Smarc

User Manual

SM-B71

SMARC Rel. 2.0 compliant module with the
Xilinx® Zynq® Ultrascale+™ MPSoC

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REVISION HISTORY

Revision	Date	Note	Rif
1.0	29 October 2019	First official release	LG
1.1	7 October 2020	Safety policy chapter added (par. 1.7) Power Consumption paragraph updated (par. 2.3.1) VDD_RTC Power rail meaning updated (par. 2.3.2) SMARC connector's table pin S144 corrected (par. 3.2.1) S113 pin assignment in par. 3.2.3 corrected	SB

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For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at https://www.seco.com (registration required).

Our team is ready to assist.

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Chapter 1.
INTRODUCTION

- Warranty
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1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/eu/support/online-rma.html (Online RMA). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit https://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210

- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "Contact us" then "Online RMA" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SM-B71 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The SM-B71 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a SM-B71 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SM-B71 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the SM-B71 Module shall be:

- used exclusively on SMARC 2.0 Compliant Carrier boards that impose limited power source up to 25W Max;
- installed inside a Fire Enclosure compliant with all applicable EN62368-1 requirements (alternatively, it must be performed an analysis for the reduction of the likelihood of ignition in single fault condition according clause 6.4.1 of the standard);
- used along with CPU Heatspreader/heatsinks designed according to the mechanical characteristics indicated in par. 2.4

The manufacturer which include an SM-B71 module in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition.
- provide an instructional safeguard against thermal injuries, according to clause 9.4.2 of the above mentioned standard. This instructional safeguard must be placed both on end-user product's User Manual and on the products itself (Danger Label).

1.8 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DDR4	DDR, 4th Generation
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer

	(PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SGMII	Serial Gigabit Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
USB	Universal Serial Bus

1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://esd.cs.ucr.edu/webres/can20.pdf
CSI	http://www.mipi.org/specifications/camera-interface
Display Port	https://www.displayport.org/
Gigabit Ethernet	https://standards.ieee.org/standard/802_3-2018.html
I2C	https://www.nxp.com/docs/en/user-guide/UM10204.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/lit/an/snla165/snla165.pdf and http://www.ti.com/lit/pdf/SNLA187
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-64
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SMARC Design Guide 2.0	https://sget.org/wp-content/uploads/2018/09/SMARC_DG_V2.pdf
SMARC Hardware Specification 2.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
USB 2.0 and USB OTG	https://www.usb.org/document-library/usb-20-specification
Xilinx® Zinq® UltraScale+™ MPSoCs	https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram

2.1 Introduction

The SM-B71 is a SMARC Rel. 2.0 compliant module with the Xilinx® Zynq® Ultrascale+™ MPSoC. Delivering flexibile ARM + FPGA Heterogeneous processing in a standard form factor, this solution is able to merge wide scalability, from cost effective Dual-Core to high performance Quad-Core ARM® Cortex®-A53 MPSoCs with GPU/VCU, and extreme flexibility (up to 256k FPGA logic cells). It also features dedicated Real-Time ARM® Cortex®-R5 processors, along with LVDS and DP video interfaces up to 4K resolution and high-speed interfaces. ®®The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express

Presented in the SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 314-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in SM-B71 module.

2.2 Technical Specifications

Processors

Xilinx® Zynq® Ultrascale+™ ZU2CG, ZU3CG, ZU4CG or ZU5CG MPSoCs:
Dual-core ARM® Cortex®-A53 MPCore Application Processing Unit +Dual-core ARM® Cortex®-R5 Real-Time Processing Unit

Xilinx® Zynq® Ultrascale+™ ZU2EG, ZU3EG, ZU4EG, ZU5EG, ZU4EV or ZU5EV MPSoCs:
Quad-core ARM® Cortex®-A53 MPCore Application Processing Unit +Dual-core ARM® Cortex®-R5 Real-Time Processing Unit

Memory

Soldered Down DDR4-2400 memory:

- Up to 8GB for Processing System Unit, 64-bit interface
- Up to 2GB for Programmable Logic, 6-bit interface

Graphics

Only on EG and EV MPSOcs:

- Integrated ARM Mali-400 MP2 Graphics Processing Unit
- Multicore 2D/3D acceleration at 667MHz
- OpenGL ES 1.1 / 2.0, OpenVG 1.0 / 1.1

On EV MPSoCs only, H.264/H.265 integrated video codec

Video Interfaces

DP interface
18/24-bit Dual Channel LVDS interface

Video Resolution

DP, resolution up to 4096x2160 @ 60Hz
LVDS, resolution dependent on the IP implemented in the programmable logic

Mass Storage

1x S-ATA Gen3 Channel
Optional eMMC 4.51 Drive soldered on-board
SD 4-bit interface
QuadSPI Flash

PCI Express

PCI-e x4 Gen3 interface

Networking

Up to 2x Gigabit Ethernet interface
Optional WiFi + BT LE module onboard

USB

1 x USB 2.0 OTG port
2 x USB 2.0 Host ports
2 x USB 3.0 Host ports

Audio

Dependent on the IP implemented in the programmable logic

Serial ports

2x UART Tx/Rx/RTS/CTS
2x UART Tx/Rx
2x CAN Bus

Other Interfaces

1x 4-lanes + 1x 2-lanes CSI camera interfaces
2x I2C Bus
2x SPI interfaces
12 x GPI/Os
Boot select signals
Power Management Signals

Power supply voltage: +3 ÷ +5.25 V_{DC}

RTC voltage: 3.3V

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **.

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 4.1

2.3 Electrical Specifications

According to SMARC specifications, the SM-B71 module can be supplied with an external voltage in the range +3V ÷ +5.25V_{DC}.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_{DC} power rail.

2.3.1 Power Consumption

The power consumption of the module depends strongly on the IP programmed on the internal FPGA, which can implement many different features.

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. Electrical voltage in the range +3V ÷ +5.25VDC directly coming from the card edge connector.

+3.3V_S: +3.3 switched voltage, derived internally.

+3.3V_ALW: +3.3 always voltage, derived internally.

+1.8V_S: +1.8 switched voltage, derived internally.

+1.8V_ALW: +1.8 always voltage, derived internally.

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card connector for supplying the RTC clock on the Zynq® Ultrascale+™ processor when the +3.3V_ALW Power rail is not available

Switched voltages are power rails active only when the board is in ACPI's S0 (Working) State;

Always voltages, instead, are power rails active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) Power States.

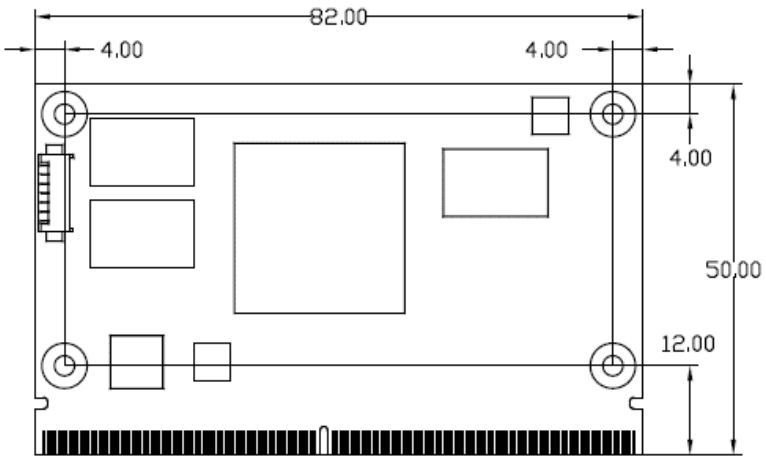
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97” x 3.23”) including the pin numbering and edge finger pattern.

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of SM-B71 will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector’s height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Supported Operating Systems

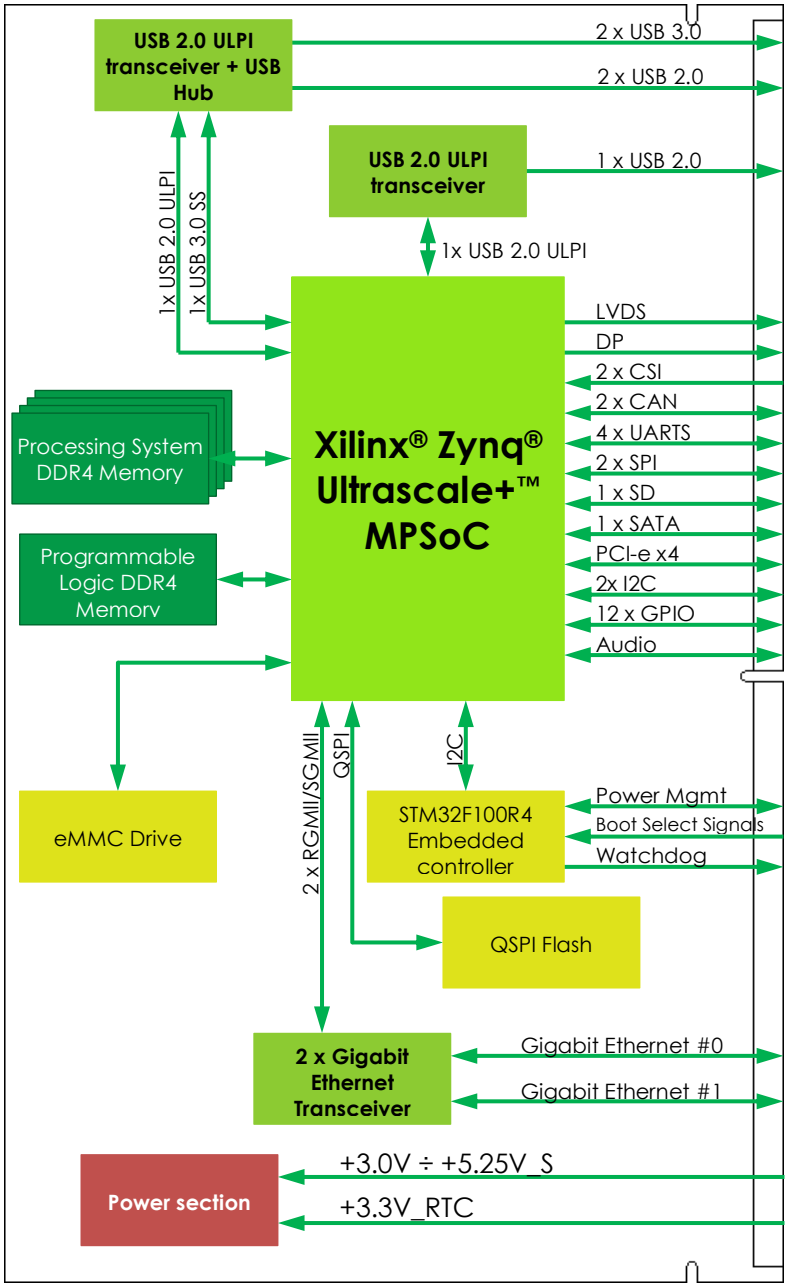
SM-B71 module supports the following operating systems:

- Linux

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC’s.

For further details, please visit https://www.seco.com.

2.6 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description

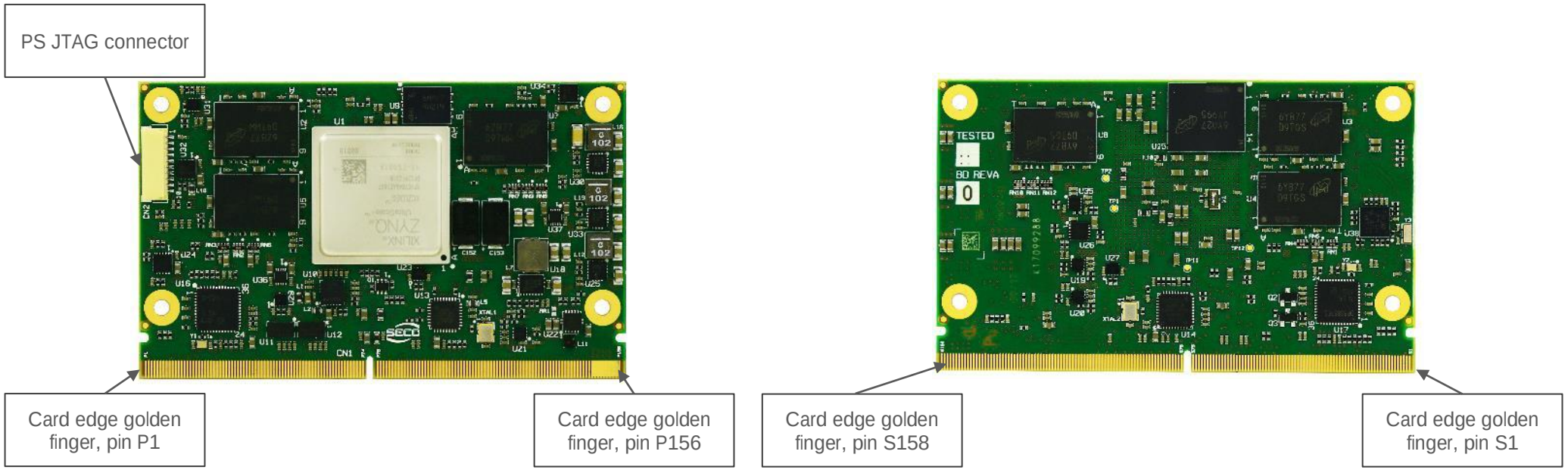
3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

An additional connector, CN2, is available for JTAG programming of the Zynq® Ultrascale+™ processor (more specifically, it is used for chip-level JTAG functions, Arm processor code downloads and run-time control operations, PL configuration, and PL debug).

TOP SIDE

BOTTOM SIDE



3.2 Connectors description

3.2.1 SMARC Connector

According to SMARC Rel 2.0 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC Rel 2.0 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals implemented.

For accurate signals description, please consult the following paragraphs.

SMARC Golden Finger Connector - CN4							
TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C_CAM1_CK	I/O	CAMERA
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C_CAM1_DAT	I/O	CAMERA
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	N.C.		
CAMERA	I	CSI1_CK-	P4	S5	I2C_CAM0_CK	I/O	CAMERA
		N.C.	P5	S6	CAM_MCK	O	CAMERA
		N.C	P6	S7	I2C_CAM0_DAT	I/O	CAMERA
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA
		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		
CAMERA	I	CSI1_RX3+	P16	S17	GBE1_MDI0+	I/O	GBE

CAMERA	I	CSI1_RX3-	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	GBE
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	O	GBE
GBE	O	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	I/O	GBE
GBE	I/O	GBE0_MDI2-	P23	S24	GBE1_MDI2-	I/O	GBE
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3+	I/O	GBE
GBE	I/O	GBE0_MDI1-	P26	S27	GBE1_MDI3-	I/O	GBE
GBE	I/O	GBE0_MDI1+	P27	S28	N.C.		
		N.C.	P28	S29	PCIE_D_TX+	O	PCI_e
GBE	I/O	GBE0_MDI0-	P29	S30	PCIE_D_TX-	O	PCI_e
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
SPI_INTERFACE	O	SPI0_CS1#	P31	S32	PCIE_D_RX+	I	PCI_e
		GND	P32	S33	PCIE_D_RX-	I	PCI_e
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	AUDIO_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	ESPI_ALERT0#	I	SPI_INTERFACE
SPI_INTERFACE	O	SPI0_CS0#	P43	S44	ESPI_ALERT1#	I	SPI_INTERFACE
SPI_INTERFACE	O	SPI0_CK	P44	S45	N.C.		
SPI_INTERFACE	I	SPI0_DIN	P45	S46	N.C.		
SPI_INTERFACE	O	SPI0_DO	P46	S47	GND		

		GND	P47	S48	I2C_GP_CK	I/O	I2C
SATA	O	SATA_TX+	P48	S49	I2C_GP_DAT	I/O	I2C
SATA	O	SATA_TX-	P49	S50	I2S2_LRCK	I/O	AUDIO
		GND	P50	S51	I2S2_SDOUT	O	AUDIO
SATA	I	SATA_RX+	P51	S52	I2S2_SDIN	I	AUDIO
SATA	I	SATA_RX-	P52	S53	I2S2_CK	I/O	AUDIO
		GND	P53	S54	N.C.		
SPI_INTERFACE	O	ESPI_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
SPI_INTERFACE	O	ESPI_CS1#	P55	S56	ESPI_IO_2	I/O	SPI_INTERFACE
SPI_INTERFACE	O	ESPI_CK	P56	S57	ESPI_IO_3	I/O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_1	P57	S58	ESPI_RESET#	O	SPI_INTERFACE
SPI_INTERFACE	I/O	ESPI_IO_0	P58	S59	N.C.		
		GND	P59	S60	N.C.		
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	USB3_SSTX+	O	USB
USB	I/O	USB0_EN_OC#	P62	S63	USB3_SSTX-	O	USB
USB	I	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	USB3_SSRX+	I	USB
USB	I/O	USB1+	P65	S66	USB3_SSRX-	I	USB
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
		STM32_RST#	P72	S73	GND		
		N.C.	P73	S74	USB2_SSRX+	I	USB
USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCI_e
USB	I/O	USB4_EN_OC#	P76	S77	PCIE_C_RST#	O	PCI_e

		SWDIO	P77	S78	PCIE_C_RX+	I	PCI_e
		SWCLK	P78	S79	PCIE_C_RX-	I	PCI_e
		GND	P79	S80	GND		
PCI_e	O	PCIE_C_REFCK+	P80	S81	PCIE_C_TX+	O	PCI_e
PCI_e	O	PCIE_C_REFCK-	P81	S82	PCIE_C_TX-	O	PCI_e
		GND	P82	S83	GND		
		N.C.	P83	S84	PCIE_B_REFCK+	O	PCI_e
		N.C.	P84	S85	PCIE_B_REFCK-	O	PCI_e
		GND	P85	S86	GND		
PCI_e	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCI_e
PCI_e	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCI_e
		GND	P88	S89	GND		
PCI_e	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCI_e
PCI_e	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCI_e
		GND	P91	S92	GND		
CAMERA	I/O	CSI2_RX2+	P92	S93	DP0_LANE0+	O	DP++
CAMERA	I/O	CSI2_RX2-	P93	S94	DP0_LANE0-	O	DP++
		GND	P94	S95	N.C.		
CAMERA	I/O	CSI2_RX1+	P95	S96	DP0_LANE1+	O	DP++
CAMERA	I/O	CSI2_RX1-	P96	S97	DP0_LANE1-	O	DP++
		GND	P97	S98	DP0_HPD	I	DP++
CAMERA	I/O	CSI2_RX0+	P98	S99	DP0_LANE2+	O	DP++
CAMERA	I/O	CSI2_RX0-	P99	S100	DP0_LANE2-	O	DP++
		GND	P100	S101	GND		
CAMERA	I/O	CSI2_CK+	P101	S102	DP0_LANE3+	O	DP++
CAMERA	I/O	CSI2_CK-	P102	S103	DP0_LANE3-	O	DP++
		GND	P103	S104	N.C.		
GENERAL PURPOSE	I	DP1_HPD	P104	S105	DP0_AUX+	I/O	DP++
GENERAL PURPOSE	I/O	HDMI_CTRL_CK	P105	S106	DP0_AUX-	I/O	DP++
GENERAL PURPOSE	I/O	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT

GENERAL PURPOSE	I	DP1_AUX_SEL	P107	S108	LVDS1_CK+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO4 / HDA_RST#	P112	S113	eDP1_HPD	I	GENERAL PURPOSE
GPIO	I/O	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6 / TACHIN	P114	S115	LVDS1_1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	N.C.		
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_1-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_2-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_3+	O	PRIMARY_DISPLAY

ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	N.C.		
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	eDP0_HPD	I	GENERAL PURPOSE
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
CAN	O	CAN1_TX	P145	S146	PCIE_WAKE#	I	PCI_e
CAN	I	CAN1_RX	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

3.2.1.1 LCD Display Support Signals

The panel control signals are:

LCD0_VDD_EN: Panel #0 VDD enable signal. Set high to enable. +1.8V_S electrical level Output.

LCD0_BKLT_EN: Panel #0 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_S electrical level Output

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #0 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_S electrical level Output

LCD1_VDD_EN: Panel #1 VDD enable signal. Set high to enable. +1.8V_S electrical level Output

LCD1_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_S electrical level Output.

LCD1_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_S electrical level Output.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_S electrical level Bidirectional

I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_S electrical level Output

3.2.1.2 Primary Display (LVDS Flat Panel) signals

LVDS interface is available on card edge connector only if the corresponding IP has been programmed in the PL of Xilinx® Zynq® Ultrascale+™ processor.

Supported resolutions depend on the programmed IP

LVDS0_0+ / LVDS0_0- : LVDS Channel #0 differential data pair #0

LVDS0_1+/ LVDS0_1-: LVDS Channel #0 differential data pair #1

LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2

LVDS0_3+/ LVDS0_3-: LVDS Channel #0 differential data pair #3

LVDS0_CK+/ LVDS0_CK-: LVDS Channel #0 differential Clock

LVDS1_0+/LVDS1_0-: LVDS Channel #1 differential data pair #0.

LVDS1_1+/LVDS1_1-: LVDS Channel #1 differential data pair #1.

LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2.

LVDS1_3+/LVDS1_3-: LVDS Channel #1 differential data pair #3.

LVDS1_CK+/LVDS1_CK-: LVDS Channel #1 differential Clock.

3.2.1.3 Secondary Display (DP++ interface) signals

The Xilinx® Zynq® Ultrascale+™ processor offers a Display Port Controller, which provides a DP standard interface for DP 1.2 compliant displays.

The signals are:

DP0_LANE3+/DP0_LANE3-: Display Port differential pair #3.

DP0_LANE2+/DP0_LANE2-: Display Port differential pair #2.

DP0_LANE1+/DP0_LANE1-: Display Port differential pair #1

DP0_LANE0+/DP0_LANE0-: Display Port differential pair #0

DP0_AUX+/DP0_AUX-: Display Port auxiliary channel differential pair.

DP0_HPD. DisplayPort Hot Plug Detect Input signal. +1.8V_S electrical level signal, active high with 100kΩ pull-down resistor.

Please be aware that Xilinx® Zynq® Ultrascale+™ processor supports only the DP interface, not DP++. The DP0_AUX_SEL signal, necessary to manage the switching between HDMI/DVI and DP mode, is therefore not managed on the module

3.2.1.4 Serial Cameras

According to SMARC specifications, there are two MIPI-CSI2 interfaces available. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair
CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0
CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair
CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0
CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1
CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2
CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3
I2C_CAM0_CK: . CSI Port #0 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_S
I2C_CAM0_DAT: . CSI Port #0 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_S
I2C_CAM1_CK: : CSI Port #1 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_S
I2C_CAM1_DAT: CSI Port #1 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_S
CAM_MCK: Master clock Output for CSI Port #0 and/or #1 support, electrical level 1.8V_S

A third CSI camera interface is implemented on SMARC card edge connector, on pins originally intended for HDMI connection. This interface is not compliant to SMARC specifications, it has been implemented to maximize the number of Zynq® processor's pins available on the card edge connector. See also par. 3.2.1.19

and 3.2.3.

CSI2_CK+/CSI2_CK-: 3-lane CSI Input Clock Differential Pair

CSI2_RX0+/CSI2_RX0- 3-lane CSI Input Differential Pair 0

CSI2_RX1+/CSI2_RX1-: 3-lane CSI Input Differential Pair 1

CSI2_RX2+/CSI2_RX2-: 3-lane CSI Input Differential Pair 2

3.2.1.5 SDI/O interface signals

The Xilinx® Zynq® Ultrascale+™ processor offer two SD 3.0 / SDIO3.0 / eMMC 4.51 interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC and external SDI/O interface).

The SDIO0 signals of the processor are used for the onboard eMMC storage of the SM-B71 module.

The SDIO1 interface of the processor is externally accessible through the edge connector of the module. Supporting 4-bit mode as per the SMARC specification.

The edge accessible SDIO1 signals are as follows:

SDIO_WP: Write Protect bidirectional signal, electrical level +3.3V_S. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_S, used to send command from Host (Zynq® Ultrascale+™ processor) to the connected card, and to send the response from the card to the Host.

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_S with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), 50 MHz maximum frequency for SD/SDIO High Speed Mode.

SDIO_PWR_EN: SDIO Power Enable output, active low signal, electrical level +3.3V_S. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SDIO data bus. Signals for 4-bit SD/SDIO/MMC communication mode.

3.2.1.6 SPI interface signals

Managed by the Zynq® Ultrascale+™ processor's SPI Controller, the signals related to SPI0 are as follows:

SPI0_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_S

SPI0_CS1#: SPI secondary Chip select, active low output signal. Electrical level +1.8V_S. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device

SPI0_CK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_S

SPI0_DIN: SPI0 Master Data Input, electrical level +1.8V_S. Input to the processor from SPI devices embedded on the Carrier Board

SPI0_DO: SPI0 Master Data Output, electrical level +1.8V_S. Output from the processor to SPI devices embedded on the Carrier Board

Managed by the Zynq® Ultrascale+™ processor's QuadSPI Controller, the signals related to QuadSPI are as follows:

ESPI_CK: QuadSPI Master Clock Output. Electrical level +1.8V_S. The reference timing signal for all the serial input and output operations

ESPI_CS0#: QuadSPI Master Chip Select Output #0. Electrical level +1.8V_S. Driven low by the processor to select the QuadSPI slave device on the carrier board. On the same bus there is a second QuadSPI slave device (flash storage), mounted on the module, connected to a dedicated chip select signal

ESPI_CS1#: QuadSPI Master Chip Select Output #1. Electrical level +1.8V_S. This signal must be used only in case there are two QSPI devices on the carrier board, and the first chip select signal (ESPI_CS0#) has already been used. It must not be used in case there is only one QSPI device

ESPI_IO_[0:3]: QuadSPI Master Data Bidirectional . Electrical level +1.8V_S. Data transfer between the master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO).

ESPI_RESET#: QuadSPI Reset. Output. Electrical level +1.8V_S. Reset the QuadSPI interface for both master and slaves.

ESPI_ALERT0#: Alert signal driven by the slave QuadSPI slave device #0. Input. Electrical level +1.8V_S

ESPI_ALERT1#: Alert signal driven by the slave QuadSPI slave device #1. Input. Electrical level +1.8V_S

3.2.1.7 Audio interface signals

By programming a dedicated IP on the FPGA, it is possible to have two I2S Audio interfaces, here are following the signals related to them:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_S

I2S0_LRCK: Left& Right audio interface #0 synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

I2S0_SDOUT: Digital audio interface #0 Output. Output from the module to the Carrier board, electrical level +1.8V_S

I2S0_SDIN: Digital audio interface #0 Input. Input from the module to the Carrier board, electrical level +1.8V_S

I2S0_CK: Digital audio interface #0 clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

I2S2_LRCK: Left& Right audio interface #2 synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

I2S2_SDOUT: Digital audio interface #2 Output. Output from the module to the Carrier board, electrical level +1.8V_S

I2S2_SDIN: Digital audio interface #2 Input. Input from the module to the Carrier board, electrical level +1.8V_S

I2S2_CK: Digital audio interface #2 clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

All these signals can be connected, on the Carrier Board, to as many I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.1.8 IC2 Interface

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_S

3.2.1.9 Asynchronous Serial Ports (UART) interface signals

Four UART interfaces are available.

SER0_TX: UART #0 Interface, Serial data Transmit (output) line, +1.8V_S electrical level

SER0_RX: UART #0 Interface, Serial data Receive (input) line, +1.8V_S electrical level

SER0_RTS#: UART #0 Interface, Handshake signal, Request to Send (output) line, +1.8V_S electrical level

SER0_CTS#: UART #0 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_S electrical level

SER1_TX: UART #1 Interface, Serial data Transmit (output) line, +1.8V_S electrical level

SER1_RX: UART #1 Interface, Serial data Receive (input) line, +1.8V_S electrical level

SER2_TX: UART #2 Interface, Serial data Transmit (output) line, +1.8V_S electrical level

SER2_RX: UART #2 Interface, Serial data Receive (input) line, +1.8V_S electrical level

SER2_RTS#: UART #2 Interface, Handshake signal, Request to Send (output) line, +1.8V_S electrical level

SER2_CTS#: UART #2 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_S electrical level.

SER3_RX: UART #3 Interface, Serial data Receive (input) line, +1.8V_S electrical level

SER3_TX: UART #3 Interface, Serial data Transmit (output) line, +1.8V_S electrical level

A fourth UART interface is present only when the module is without the optional onboard WLAN combo module:

Please consider that interface is at +1.8V_S electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_S level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

3.2.1.10 CAN interface signals

Two CAN interfaces, directly managed by the Xilinx® Zynq® Ultrascale+™ processor, are available on SMARC card edge connector.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_S electrical voltage level signal.

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_S electrical voltage level signal.

CAN1_TX: CAN Transmit Output for CAN Bus Channel 1. +1.8V_S electrical voltage level signal.

CAN1_RX: CAN Receive Input for CAN Bus Channel 1. +1.8V_S electrical voltage level signal.

Please consider that it is not possible to connect the SMARC CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.1.11 USB interface signals

The module has 5x USB ports consisting of 1x USB 2.0 OTG port from the Xilinx® Zynq® Ultrascale+™ processor's USB 2.0 controller through an USB 2.0 ULPI transceiver.

2x USB 3.0 ports and 2x USB 2.0 are implemented by using an USB 2.0 ULP transceiver plus an USB 3.0 Hub controller.

USB 2.0 controller Core #1 is capable of OTG (On-The-Go) capabilities, capable to work in High Speed (HS), Full Speed (FS) and Low Speed (LS) in Host mode, and HS/FS in peripheral mode. It is carried out directly to the golden finger connector

To allow OTG functionality, the following signal must be driven as an open collector signal by external circuitry placed on the carrier board:

USB0_OTG_ID: USB OTG Input, electrical level +3.3V_S. When USB Port #0 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low). It must be tied to GND when USB Port #0 has to be set to work in Host mode. When not driven, USB Port#0 will work in Client mode.

USB0_VBUS_DET: USB Host power detection signal, Input Signal, electrical level

USB0+/ USB0-: Universal Serial Bus Port #0 differential pair.

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for over current operation information.

USB1+/ USB1-: Universal Serial Bus Port #1 differential pair

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port #2 differential pair.

USB2_SSTX+/ USB2_SSTX-: USB Port #2 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB Port #2 Superspeed Receive differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port #3 differential pair.

USB3_SSTX+/ USB3_SSTX-: USB Port #3 Superspeed Transmit differential pair.

USB3_SSRX+/ USB3_SSRX-: USB Port #3 Superspeed Receive differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for OC operation information.

USB4+/ USB4-: Universal Serial Bus Port #4 differential pair

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for OC operation information.

USB5_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_S electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.0 Specification for OC operation information.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

3.2.1.12 PCI Express interface signals

The Xilinx® Zynq® Ultrascale+™ processor offers a single PCI-e controller, able to manage a single PCI-e x1, PCI-e x2 or PCI-e x4 link.

PCI express Gen 3.0 (8Gbps) is supported.

Here following the signals involved in PCI express management

PCIE_A_RX+/PCIE_A_RX-: PCI Express lane #0, Transmitting Output Differential pair
PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Receiving Input Differential pair
PCIE_A_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_S electrical level.

PCIE_B_RX+/PCIE_B_RX-: PCI Express lane #1, Transmitting Output Differential pair
PCIE_B_TX+/PCIE_B_TX-: PCI Express lane #1, Receiving Input Differential pair
PCIE_B_REFCK+/PCIE_B_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair
PCIE_B_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_S electrical level.

PCIE_C_RX+/PCIE_C_RX-: PCI Express lane #1, Transmitting Output Differential pair
PCIE_C_TX+/PCIE_C_TX-: PCI Express lane #1, Receiving Input Differential pair
PCIE_C_REFCK+/PCIE_C_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair
PCIE_C_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_S electrical level.

PCIE_D_RX+/PCIE_D_RX-: PCI Express lane #1, Transmitting Output Differential pair
PCIE_D_TX+/PCIE_D_TX-: PCI Express lane #1, Receiving Input Differential pair
PCIE_D_REFCK+/PCIE_D_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair

PCIE_WAKE#: PCIe wake up Input Signal, interrupt to Host. Active Low, +3.3V_S electrical level with a 10kΩ pull-up resistor.

3.2.1.13 SATA interface signals

The Xilinx® Zynq® Ultrascale+™ processor offers a SATA Host Controller, compliant to SATA 3.1 specifications, able to manage up to two external devices.

1.5, 3.0 and 6.0 Gb/s data rates are supported.

According to SMARC specifications, only one SATA interface is available on the Card edge connector, with the following signals:

SATA_RX+/SATA_RX-: SATA Channel Transmitting Output Differential pair

SATA_TX+/SATA_TX-: SATA Channel Receiving Input Differential pair

3.2.1.14 Gigabit Ethernet signals

Up to two Gigabit Ethernet interfaces can realized on SM-B71 module

The first one is implemented by using a Texas Instruments DP83867CR Gigabit Ethernet transceiver, which is interfaced to Xilinx® Zynq® Ultrascale+™ processor through an RGMII interface.

Here following the signals involved in Gigabit Ethernet #0 management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair 0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair 1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair 2

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair 3

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_S electrical level

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_S electrical level

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_S electrical level

The second Gigabit Ethernet interface is optional (factory configuration), and can be implemented by using a Texas Instruments Gigabit Ethernet transceiver interfaced to Xilinx® Zynq® Ultrascale+™ processor through an SGMII interface.

Here following the signals involved in Gigabit Ethernet #1 management

GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair 0

GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair 1

GBE1_MDI2+/GBE1_MDI2-: Media Dependent Interface (MDI) Transmit differential pair 2

GBE1_MDI3+/GBE1_MDI3-: Media Dependent Interface (MDI) Transmit differential pair 3

GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_S electrical level

GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_S electrical level

GBE1_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_S electrical level

3.2.1.15 Watchdog

WDT_TIME_OUT#: Watchdog timer Output, managed by the on-board Embedded Controller. +1.8V_S electrical level

3.2.1.16 Miscellaneous signals

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_S electrical level. Can be used as Camera #0 power enable active low output.

GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_S electrical level. Can be used as Camera #1 power enable active low output.

GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_S electrical level. Can be used as Camera #0 reset active low output.
GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_S electrical level. Can be used as Camera #1 reset active low output.
GPIO4 / HDA_RST#: General Purpose I/O #4, +1.8V_S electrical level. Can be used as Audio reset active low output.
GPIO5 / PWM_OUT: General Purpose I/O #5, +1.8V_S electrical level. Can be used as a generic PWM output (i.e. for FAN management)
GPIO6 / TACHIN: General Purpose I/O #6, +1.8V_S electrical level. Can be used as a FAN Tachometer Input, when paired with GPIO5 signal
GPIO7: General Purpose I/O #7, +1.8V_S electrical level
GPIO8: General Purpose I/O #8, +1.8V_S electrical level
GPIO9: General Purpose I/O #9, +1.8V_S electrical level
GPIO10: General Purpose I/O #10, +1.8V_S electrical level
GPIO11: General Purpose I/O #11, +1.8V_S electrical level

3.2.1.17 Management pins

According to the SMARC specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board, 3.3V_ALW electrical level
CARRIER_PWR_ON: Power On command to the Carrier Board. Output, +1.8V_AL electrical level with a 100kΩ pull-down resistor.
CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_ALW electrical level with a 100kΩ pull-down resistor.
RESET_OUT#: General Purpose Reset. Output, +1.8V_ALW electrical level with a 100kΩ pull-down resistor.
RESET_IN#: General Purpose Reset. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
POWER_BTN#: Power Button. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
SLEEP#: Sleep indicator from Carrier board. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
LID#: LID Switch. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
BATLOW#: Battery Low indication signal from the Carrier Board. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
I2C_PM_CK: Power Management I2C Clock, +1.8V_S electrical level
I2C_PM_DAT: Power Management I2C Data, +1.8V_S electrical level
CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, 3.3V_ALW electrical level with a 10kΩ pull-up resistor.
TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. 3.3V_S electrical level with a 10kΩ pull-up resistor
SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_ALW electrical level with a 4k7Ω pull-up resistor

3.2.1.18 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_S electrical level with a 10kΩ pull-up resistor.

BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_S electrical level with a 10kΩ pull-up resistor.

BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_S electrical level with a 10kΩ pull-up resistor.

FORCE_RECOV#: Force recovery Mode. Input, +1.8V_S electrical level.

3.2.1.19 Non-standard signals

The following signals are named according to SMARC specifications, however they are not managed to implement the functionality included into the standard. This means that they can be reprogrammed to realise generic functionalities. Please check also following paragraph 3.2.3.

DP1_HPD: General Purpose Signal, +1.8V_S electrical level.

HDMI_CTRL_CK: General Purpose Signal, +1.8V_S electrical level.

HDMI_CTRL_DAT: General Purpose Signal, +1.8V_S electrical level.

DP1_AUX_SEL: General Purpose Signal, +1.8V_S electrical level

eDP0_HPD: General Purpose Signal, +3.3V_S electrical level

eDP1_HPD: General Purpose Signal, +3.3V_S electrical level

STM32_RST#: Embedded controller's Reset Input Signal, active low, +3.3V_ALW electrical level

SWDIO: Serial Wire/JTAG Debug Port for Embedded controller, SWDIO or TMS signal, +3.3V_ALW electrical level

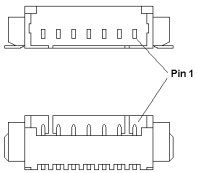
SWCLK: Serial Wire/JTAG Debug Port for Embedded controller, SWCLK or TCK signal, +3.3V_ALW electrical level

3.2.2 JTAG Connector

Besides to SMARC card edge connector, there is also a dedicated connector (CN2) for reprogramming of PS FPGA, carrying out JTAG signals.

JTAG connector – CN2			
Pin	**Signal**	**Pin**	**Signal**
1	1.8V_S	5	PS_JTAG_TDI
2	PS_SRST_B	6	PS_JTAG_TCK
3	PS_JTAG_TMS	7	GND
4	PS_JTAG_TDO		

The connector is a10-pin single line SMT connector, type MOLEX 53261-0771 or equivalent, with pinout shown in the table on the left.



Mating connector: MOLEX 51021-0700 receptacle with MOLEX 50079-8000 female crimp terminals.

PS_SRST_B: Zynq® Ultrascale+™ Processing System (PS) System Reset Input, active low, +1.8V_S electrical level with a 10kΩ pull-up resistor.

PS_JTAG_TMS: Zynq® Ultrascale+™ PS JTAG mode select, +1.8V_S electrical level with a 4k7Ω pull-up resistor.

PS_JTAG_TDO: Zynq® Ultrascale+™ PS JTAG data output, +1.8V_S electrical level with a 4k7Ω pull-up resistor.

PS_JTAG_TDI: Zynq® Ultrascale+™ PS JTAG data input, +1.8V_S electrical level with a 4k7Ω pull-up resistor.

PS_JTAG_TCK: Zynq® Ultrascale+™ PS JTAG data clock, +1.8V_S electrical level with a 4k7Ω pull-up resistor.

3.2.3 Reprogrammable pins

Since Xilinx® Zynq® Ultrascale+™ processor can be used for a wide range of applications, it is given the possibility of reprogramming its interfaces, realizing a custom module in SMARC form factor.

For this reason, in the following table is given the match between the processor pins and the SMARC card edge connector's pins, so that skilled programmers can use SM-B71 module in non-standard ways.

SMARC pins not listed in this table have a fixed functionality which cannot be changed.

Please be aware that SECO cannot support the users on applications different from SMARC standard.

SMARC Pin	SMARC I/F	ZU Pin	ZU Bank	ZU I/F	ZU bank level	I/O standard type	Note (PU, PD, Impedance) :
P1	SMB_ALERT_1V8#	AC17	500	SMB_ALERT_1V8#	1.8V		PU
P3	CSI1_CK+	J5	65	CSI1_CLK_P	1.2V	MIPI D-PHY	100 Ohm
P4	CSI1_CK-	J4	65	CSI1_CLK_N	1.2V	MIPI D-PHY	100 Ohm
P7	CSI1_RX0+	J6	65	CSI1_DATA0_P	1.2V	MIPI D-PHY	100 Ohm
P8	CSI1_RX0-	H6	65	CSI1_DATA0_N	1.2V	MIPI D-PHY	100 Ohm
P10	CSI1_RX1+	J7	65	CSI1_DATA1_P	1.2V	MIPI D-PHY	100 Ohm
P11	CSI1_RX1-	H7	65	CSI1_DATA1_N	1.2V	MIPI D-PHY	100 Ohm
P13	CSI1_RX2+	K8	65	CSI1_DATA2_P	1.2V	MIPI D-PHY	100 Ohm
P14	CSI1_RX2-	K7	65	CSI1_DATA2_N	1.2V	MIPI D-PHY	100 Ohm
P16	CSI1_RX3+	K9	65	CSI1_DATA3_P	1.2V	MIPI D-PHY	100 Ohm
P17	CSI1_RX3-	J9	65	CSI1_DATA3_N	1.2V	MIPI D-PHY	100 Ohm
P31	SPI0_CS1#	AF17	500	MIO8_SPI1_CS1#	1.8V	LVCMOS	PU
P43	SPI0_CS0#	AC16	500	MIO9_SPI1_CS0#	1.8V	LVCMOS	PU
P44	SPI0_CK	AF16	500	MIO_6_SPI_CLK	1.8V	LVCMOS	PU
P45	SPI0_DIN	AD17	500	MIO10_SPI1_MISO	1.8V	LVCMOS	PU
P46	SPI0_DO	AE17	500	MIO11_SPI1_MOSI	1.8V	LVCMOS	PU

P48	SATA_TX+	C25	505	MGTRTX_S_P2*	SATA spec.	SATA spec.	*Muxed with SGMII
P49	SATA_TX-	C26	505	MGTRTX_S_N2*	SATA spec.	SATA spec.	*Muxed with SGMII
P51	SATA_RX+	B27	505	MGTRRX_S_P2*	SATA spec.	SATA spec.	*Muxed with SGMII
P52	SATA_RX-	B28	505	MGTRRX_S_N2*	SATA spec.	SATA spec.	*Muxed with SGMII
P54	ESPI_CS0#	W12	24	ESPI_CS0#	1.8V	LVCMOS	
P55	ESPI_CS1#	Y13	24	ESPI_CS1#	1.8V	LVCMOS	
P56	ESPI_CK	AB15	24	ESPI_CK	1.8V	LVCMOS	
P57	ESPI_IO0	Y14	24	ESPI_IO1	1.8V	LVCMOS	
P58	ESPI_IO1	W13	24	ESPI_IO0	1.8V	LVCMOS	
P62	USB0_EN_OC#	AH11	44	USB0_EN_OC#	3.3V	LVCMOS	
P67	USB1_EN_OC#	AH12	44	USB1_EN_OC#	3.3V	LVCMOS	
P71	USB2_EN_OC#	AG11	44	USB2_EN_OC#	3.3V	NA	
P74	USB3_EN_OC#	AF11	44	USB3_EN_OC#	3.3V	LVCMOS	
P76	USB4_EN_OC#	AH10	44	USB4_EN_OC#	3.3V	LVCMOS	
P80	PCIE_C_REFCK+	D7	66	PCIE_C_REFCLK+	1.8V	LVCMOS	
P81	PCIE_C_REFCK-	D6	66	PCIE_C_REFCLK-	1.8V	LVCMOS	
P86	PCIE_A_RX+	Y2	224	MGTHRX_P0	PCI-e spec.	PCI-e spec.	
P87	PCIE_A_RX-	Y1	224	MGTHRX_N0	PCI-e spec.	PCI-e spec.	
P89	PCIE_A_TX+	W4	224	MGTHTX_P0	PCI-e spec.	PCI-e spec.	
P90	PCIE_A_TX-	W3	224	MGTHTX_N0	PCI-e spec.	PCI-e spec.	
P92	HDMI_D2+	T8	65	CSI2_DATA2_N	1.2V	MIPI D-PHY	100 Ohm
P93	HDMI_D2-	R8	65	CSI2_DATA2_P	1.2V	MIPI D-PHY	100 Ohm
P95	HDMI_D1+	V8	65	CSI2_DATA1_P	1.2V	MIPI D-PHY	100 Ohm
P96	HDMI_D1-	U8	65	CSI2_DATA1_N	1.2V	MIPI D-PHY	100 Ohm
P98	HDMI_D0+	V9	65	CSI2_DATA0_P	1.2V	MIPI D-PHY	100 Ohm
P99	HDMI_D0-	U9	65	CSI2_DATA0_N	1.2V	MIPI D-PHY	100 Ohm
P101	HDMI_CK+	W8	65	CSI2_CLK_P	1.2V	MIPI D-PHY	100 Ohm
P102	HDMI_CK-	Y8	65	CSI2_CLK_N	1.2V	MIPI D-PHY	100 Ohm
P104	DP1_HPD	J14	26	DP1_HPD	1.8V	LVCMOS	
P105	HDMI_CTRL_CK	F2	66	HDMI_CTRL_CK	1.8V	LVCMOS	

P106	HDMI_CTRL_DAT	E2	66	HDMI_CTRL_DAT	1.8V	LVCMOS	
P107	DP1_AUX_SEL	K14	26	DP1_AUX_SEL	1.8V	LVCMOS	
P108	GPIO0	F11	25	GPIO0	1.8V	LVCMOS	
P109	GPIO1	F12	25	GPIO1	1.8V	LVCMOS	
P110	GPIO2	F10	25	GPIO2	1.8V	LVCMOS	
P111	GPIO3	G11	25	GPIO3	1.8V	LVCMOS	
P112	GPIO4	H12	25	GPIO4	1.8V	LVCMOS	
P113	GPIO5	J12	25	GPIO5	1.8V	LVCMOS	
P114	GPIO6	G10	25	GPIO6	1.8V	LVCMOS	
P115	GPIO7	H11	25	GPIO7	1.8V	LVCMOS	
P116	GPIO8	K12	25	GPIO8	1.8V	LVCMOS	
P117	GPIO9	K13	25	GPIO9	1.8V	LVCMOS	
P118	GPIO10	J10	25	GPIO10	1.8V	LVCMOS	
P119	GPIO11	J11	25	GPIO11	1.8V	LVCMOS	
P121	I2C_PM_CK	AB19	500	MIO24_I2C1_SCL	1.8V	LVCMOS	
P122	I2C_PM_DAT	AB21	500	MIO25_I2C1_SDA	1.8V	LVCMOS	
P129	SER0_TX	A14	26	SER0_TX	1.8V	LVCMOS	
P130	SER0_RX	B14	26	SER0_RX	1.8V	LVCMOS	
P131	SER0_RTS	A15	26	SER0_RTS#	1.8V	LVCMOS	
P132	SER0_CTS	B15	26	SER0_CTS#	1.8V	LVCMOS	
P134	SER1_TX	L14	26	UART0_TX	1.8V	LVCMOS	
P135	SER1_RX	L13	26	UART0_RX	1.8V	LVCMOS	
P136	SER2_TX	D14	26	SER2_TX	1.8V	LVCMOS	
P137	SER2_RX	D15	26	SER2_RX	1.8V	LVCMOS	
P138	SER2_RTS#	C13	26	SER2_RTS#	1.8V	LVCMOS	
P139	SER2_CTS#	C14	26	SER2_CTS#	1.8V	LVCMOS	
P140	SER3_TX	K18	501	UART1_TX	3.3V	LVCMOS	
P141	SER3_RX	J19	501	UART1_RX	3.3V	LVCMOS	
P143	CAN0_TX	B20	502	CAN0_TX	1.8V	LVCMOS	
P144	CAN0_RX	F20	502	CAN0_RX	1.8V	LVCMOS	

P145	CAN1_TX	AF13	24	CAN1_TX	1.8V	LVCMOS	
P146	CAN1_RX	AE13	24	CAN1_RX	1.8V	LVCMOS	
S1	I2C_CAM1_SCL	B11	25	I2C_CAM1_CLK	1.8V	LVCMOS	
S2	I2C_CAM1_SDA	B10	25	I2C_CAM1_SDA	1.8V	LVCMOS	
S5	I2C_CAM0_SCL	A12	25	I2C_CAM0_CLK	1.8V	LVCMOS	
S6	CAM_MCK	AD15	24	CAM_MCK	1.8V	LVCMOS	
S7	I2C_CAM0_SDA	A10	25	I2C_CAM0_SDA	1.8V	LVCMOS	
S8	CSI0_CK+	L7	65	CSI0_CLK_P	1.2V	MIPI D-PHY	100 Ohm
S9	CSI0_CK-	L6	65	CSI0_CLK_N	1.2V	MIPI D-PHY	100 Ohm
S11	CSI0_RX0+	M6	65	CSI0_DATA0_P	1.2V	MIPI D-PHY	100 Ohm
S12	CSI0_RX0-	L5	65	CSI0_DATA0_N	1.2V	MIPI D-PHY	100 Ohm
S14	CSI0_RX1+	N7	65	CSI0_DATA1_P	1.2V	MIPI D-PHY	100 Ohm
S15	CSI0_RX1-	N6	65	CSI0_DATA1_N	1.2V	MIPI D-PHY	100 Ohm
S29	PCIE_D_TX+	N4	224	MGTHTX_P3	PCI-e spec.	PCI-e spec.	
S30	PCIE_D_TX-	N3	224	MGTHTX_N3	PCI-e spec.	PCI-e spec.	
S32	PCIE_D_RX+	P2	224	MGTHRX_P3	PCI-e spec.	PCI-e spec.	
S33	PCIE_D_RX-	P1	224	MGTHRX_N3	PCI-e spec.	PCI-e spec.	
S38	AUDIO_MCK	E15	26	AUDIO_MCK	1.8V	LVCMOS	
S39	I2S0_LRCK	F15	26	I2S0_LRCK	1.8V	LVCMOS	
S40	I2S0_SDOUT	F13	26	I2S0_SDOUT	1.8V	LVCMOS	
S41	I2S0_SDIN	G13	26	I2S0_SDIN	1.8V	LVCMOS	
S42	I2S0_CK	E13	26	I2S0_CK	1.8V	LVCMOS	
S43	ESPI_ALERT0#	AA12	24	ESPI_ALERT0#	1.8V	LVCMOS	
S44	ESPI_ALERT1#	Y12	24	ESPI_ALERT1#	1.8V	LVCMOS	
S48	I2C_GP_CK	D12	25	I2C0_SCL	1.8V	LVCMOS	PU
S49	I2C_GP_DAT	A11	25	I2C0_SDA	1.8V	LVCMOS	PU
S50	I2S2_LRCK	B6	66	I2S2_LRCK	1.8V	LVCMOS	
S51	I2S2_SDOUT	C6	66	I2S2_SDOUT	1.8V	LVCMOS	
S52	I2S2_SDIN	A5	66	I2S2_SDIN	1.8V	LVCMOS	
S53	I2S2_CK	B5	66	I2S2_CK	1.8V	LVCMOS	

S55	USB5_EN_OC#	AG10	44	USB5_EN_OC#	3.3V	LVCMOS	
S56	ESPI_IO2	W14	24	ESPI_IO2	1.8V	LVCMOS	
S57	ESPI_IO3	AB14	24	ESPI_IO3	1.8V	LVCMOS	
S58	ESPI_RESET#	W11	24	ESPI_RESET#	1.8V	LVCMOS	
S76	PCIE_B_RST#	AB9	44	PCIE_B_RST#	3.3V	LVCMOS	
S77	PCIE_C_RST#	AB10	44	PCIE_C_RST#	3.3V	LVCMOS	
S78	PCIE_C_RX+	T2	224	MGTHRX_P2	PCI-e spec.	PCI-e spec.	
S79	PCIE_C_RX-	T1	224	MGTHRX_N2	PCI-e spec.	PCI-e spec.	
S81	PCIE_C_TX+	R4	224	MGTHTX_P2	PCI-e spec.	PCI-e spec.	
S82	PCIE_C_TX-	R3	224	MGTHTX_N2	PCI-e spec.	PCI-e spec.	
S84	PCIE_B_REFCK+	V6	224	GTH1_CLK_S_P	PCI-e spec.	PCI-e spec.	
S85	PCIE_B_REFCK-	V5	224	GTH1_CLK_S_N	PCI-e spec.	PCI-e spec.	
S87	PCIE_B_RX+	V2	224	MGTHRX_P1	PCI-e spec.	PCI-e spec.	
S88	PCIE_B_RX-	V1	224	MGTHRX_N1	PCI-e spec.	PCI-e spec.	
S90	PCIE_B_TX+	U4	224	MGTHTX_P1	PCI-e spec.	PCI-e spec.	
S91	PCIE_B_TX-	U3	224	MGTHTX_N1	PCI-e spec.	PCI-e spec.	
S107	LCD1_BKLT_EN	AG13	24	LCD1_BLKT_EN	1.8V	LVCMOS	
S108	LVDS1_CK+	E5	66	LVDS1_CK+	1.8V	LVDS	100 Ohm
S109	LVDS1_CK-	D5	66	LVDS1_CK-	1.8V	LVDS	100 Ohm
S111	LVDS1_0+	G6	66	LVDS1_0+	1.8V	LVDS	100 Ohm
S112	LVDS1_0-	F6	66	LVDS1_0-	1.8V	LVDS	100 Ohm
S113	eDP1_HPD	AA11	44	eDP1_HPD	3.3V	LVCMOS	
S114	LVDS1_1+	F7	66	LVDS1_1+	1.8V	LVDS	100 Ohm
S115	LVDS1_1-	G8	66	LVDS1_1-	1.8V	LVDS	100 Ohm
S116	LCD1_VDD_EN	AG14	24	LCD1_VDD_EN	1.8V	LVCMOS	
S117	LVDS1_2+	F8	66	LVDS1_2+	1.8V	LVDS	100 Ohm
S118	LVDS1_2-	E8	66	LVDS1_2-	1.8V	LVDS	100 Ohm
S120	LVDS1_3+	E9	66	LVDS1_3+	1.8V	LVDS	100 Ohm
S121	LVDS1_3-	D9	66	LVDS1_3-	1.8V	LVDS	100 Ohm
S122	LCD1_BKLT_PWM	AE15	24	LCD1_BKLT_PWM	1.8V	LVCMOS	

S125	LVDS0_0+	C12	66	LVDS0_0+	1.8V	LVDS	100 Ohm
S126	LVDS0_0-	B1	66	LVDS0_0-	1.8V	LVDS	100 Ohm
S127	LCD0_BKLT_EN	AH13	24	LCD0_BKLT_EN	1.8V	LVCMOS	
S128	LVDS0_1+	A2	66	LVDS0_1+	1.8V	LVDS	100 Ohm
S129	LVDS0_1-	A1	66	LVDS0_1-	1.8V	LVDS	100 Ohm
S131	LVDS0_2+	B3	66	LVDS0_2+	1.8V	LVDS	100 Ohm
S132	LVDS0_2-	A3	66	LVDS0_2-	1.8V	LVDS	100 Ohm
S133	LCD0_VDD_EN	AH14	24	LCD0_VDD_EN	1.8V	LVCMOS	
S134	LVDS0_CK+	D4	66	LVDS0_CK+	1.8V	LVDS	100 Ohm
S135	LVDS0_CK-	C4	66	LVDS0_CK-	1.8V	LVDS	100 Ohm
S137	LVDS0_3+	B4	66	LVDS0_3+	1.8V	LVDS	100 Ohm
S138	LVDS0_3-	A4	66	LVDS0_3-	1.8V	LVDS	100 Ohm
S139	I2C_LCD_CK	C11	25	I2C_LCD_SCL	1.8V	LVCMOS	
S140	I2C_LCD_DAT	D11	25	I2C_LCD_SDA	1.8V	LVCMOS	
S141	LCD0_BKLT_PWM	AE14	24	LCD0_BKLT_PWM	1.8V	LVCMOS	
S144	eDP0_HPD	AA10	44	eDP0_HPD	3.3V	LVCMOS	
S157	TEST#	AE12	44	TEST#	3.3V	LVCMOS	PU

Pin connected to PS

Pin connected to PL

Pin connected to GTH

Pin connected to GTR

Chapter 4.
Appendices

- Thermal Design

4.1 Thermal Design

Highly integrated modules like SM-B71 offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SM-B71 indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SM-B71 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
RB71-DISS-1-PK	SMARC HEAT SPREADER: SM-B71 Heat Spreader (PASSIVE) - Packaged
RB71-DISS-2-PK	SMARC HEAT SINK: SM-B71 Heat Sink (PASSIVE) - Packaged

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