Smarc

User Manual

SM-B69

SMARC® Rel. 2.1 compliant module with the Intel® Atom™ X Series, Intel® Celeron® J / N Series and Intel® Pentium® N Series (formerly Apollo Lake) Processors

SECO

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REVISION HISTORY

Revision	Date	Note	Rif
1.0	2nd March 2020	First official release	SB / AR
1.1	16th October 2020	Second official release - Added pull-down resistor to SDIO_PWR_EN signal (par. 3.2.1.7) - Removed JTAG signals interface from SMARC MXM Connector - Added PCIE_A_CKREQ# and PCIE_B_CKREQ# signals (par. 3.2.1.8) - Added GPIO12 and GPIO13 (par. 3.2.1.16) - Aligned module to be compliant with SMARC Rel. 2.1 standard - Updated BIOS SETUP settings (Chapter 4) - Removed Mipi-DSI interface on factory alternatives - Added optional TPM 1.2 / 2.0 on board via LPC bus - Updated Block Diagram	AR
1.2	04th February 2021	Third official release - Removed SPI1 interface (paragraph 3.2.1.8) - Updated Block Diagram	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
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- Terminology and definitions
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1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210

- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The SM-B69 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The SM-B69 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a SM-B69 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The SM-B69 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
AVC	Adavanced Video Coding, a video compression standard, also known as H.264
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CSI2	MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HEVC	High Efficiency Video Coding, a video compression standard, also known as H.265
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
JPEG/MJPEG	Joint Photographic Experts Group, standard method for lossy compression of digital images. Motion JPEG is a video compression format
LAN	Local Area Network
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance

MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
MPEG2	Standard for the generic coding of moving pictures and associated audio information
MVC	Multiview Video Coding, a stereoscopic video coding standard for video compression
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, specifies programming languages for programming different devices and API
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
OS	Operating System
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SGET	Standardization Group for Embedded Technologies
SMARC	Smart Mobility Architecture, a computer Module standard maintained by the SGET
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SOC	System-on-a-chip
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
UART	Universal Asynchronous Receiver-Transmitter, is an asynchronous serial interface where data format and transmission speed are configurable
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
VP8	Open video compression format, a traditional block-based transform coding format

VP9	Successor to VP8, customized for video greater than 1080p
WMV9	Series 9 of Windows Media Video, a video compression format inlcuding native support for interlaced video, non-square pixels, and frame interpolation

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	https://uefi.org/specifications
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
CSI	http://www.mipi.org/specifications/camera-interface
DDC	http://www.vesa.org
FasEthernet	http://standards.ieee.org/about/get/802/802.3.html
Gigabit Ethernet	https://standards.ieee.org/standard/802_3-2018.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
Intel® Atom™ Apollo Lake family	https://ark.intel.com/content/www/us/en/ark/products/codename/80644/apollo-lake.html#@Embedded
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SMARC Design Guide 2.0	https://sget.org/wp-content/uploads/2018/09/SMARC_DG_V2.pdf
SMARC Hardware Specification 2.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio

SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	https://usb.org.10-1-108-210.causewaynow.com/sites/default/files/usb_32_20191024.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram

2.1 Introduction

The SM-B69 is a SMARC Rel. 2.1 compliant module based on the Intel® Atom™, Pentium® and Celeron® family of System-on-Chips (SOCs) formerly coded as Apollo Lake, a series of Single/ Dual / Quad SOCs with 64-bit instruction set.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation, which is essential for boards with sizes so reduced as for SMARC ("Smart Mobility ARChitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

The board is also available in EXTREME configuration, with all the components mounted onboard certified for industrial temperature ranges (this configuration is not available with the Celeron® processors).

The embedded memory controller allows the integration of up to 8GB of LPDDR4 Memory directly soldered onboard, speed up to 2400MHz.

All SOCs embed an Intel® HD Graphics 500 series controller, which offer high graphical performances, with support for Microsoft® DirectX12, OpenGL 4.3, OpenCL 2.0, OGL ES 3.0 and HW acceleration for video encoding and decoding of HEVC (H.265), H.264, MVC, VP8, VP9, JPEG/MJPEG. It is also possible the HW video decoding only of MPEG2, VC-1 and WMV9.

This embedded GPU is able to drive three independent displays, by using the interfaces available on SMARC connector: one DP, one HMDI or DP (factory alternatives) and one eDP + MIPI-DSI or Dual Channel 18/24bit LVDS (factory alternatives).

Mass Storage capabilities of the board include one external S-ATA Gen3 channel, a standard 4-bit SD interface and one optional eMMC 5.0 Drive soldered on board.

Other than the interfaces already discussed previously, on SMARC connector there are the signals necessary for the implementation of GB, up to 4 ports in USB2.0 only and up to 2 Super Speed (SS) ports (i.e. USB 3.0 compliant), 4 x PCI-Express lanes, HD and I^2S Audio interfaces, I^2C, SPI, LPC and SM buses, HS-UART and UART interfaces.

Interfacing to the board comes through a single card edge connector, whose pinout is defined by SMARC specifications Rel.2.1. For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in SM-B69 CPU module.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical Specifications

Processors

Intel® Atom X Series, Intel® Celeron® J / N Series and Intel® Pentium® N Series (formerly code name Apollo Lake) Processors:

- Intel® Atom™ x5-E3930 Dual Core @1.3 GHz (Burst 1.8GHz), 2MB L2 Cache, 6.5W TDP
- Intel® Atom™ x5-E3940 Quad Core @1.6 GHz (Burst 1.8GHz), 2MB L2 Cache, 9.5W TDP
- Intel® Atom™ x7-E3950 Quad Core @1.6 GHz (Burst 2.0GHz), 2MB L2 Cache, 12W TDP
- Intel® Pentium® N4200 Quad Core @1.1GHz (Burst 2.5GHz), 2MB L2 Cache, 6W TDP
- Intel® Celeron® N3350 Dual Core @1.1GHz (Burst 2.4GHz), 2MB L2 Cache, 6W TDP
- Intel® Celeron® J3455, Quad Core @1.5GHz (Burst 2.3GHz), 2MB L2Cache, 10W TDP
- Intel® Celeron® J3355, Dual Core @2.0GHz (Burst 2.5GHz), 2MB L2Cache, 10W TDP

Memory

Single-/Dual-/Quad- Channel Soldered Down LPDDR4-2400 memory, up to 8GB

Graphics

Integrated Intel® HD Graphics 500 series controller with up to 18 Execution Units
Three Independent displays supported
HW decoding of HEVC (H.265), H.264, MVC, VP8, VP9, MPEG2, VC-1, WMV9, JPEG/MJPEG formats
HW encoding of HEVC (H.265), H.264, MVC, VP8, VP9 and JPEG/MPEG format

Video Interfaces

eDP interface or Dual Channel 18/24bit LVDS interface
HDMI or DP++ interface
DP++ interface
2 x CSI interfaces

Video Resolution

HDMI, eDP, resolution up to 3840x2160 (4K) @ 60Hz
DP++, resolution up to 4096x2160 @ 60Hz
LVDS, resolution up to 1920x1200 @ 60Hz

Mass Storage

Optional eMMC 5.0 drive soldered on-board
1 x external S-ATA Gen3 Channel
SD interface

PCI Express

4 x PCI-e Root Ports

Networking

Up to 2 x Gigabit Ethernet interfaces
Intel® I210 or I211 Controller (MAC + PHY)

USB

6 x USB 2.0 Host Ports
2 x USB 3.0 Host Ports

Audio

HD Audio interface
I2S Audio interface

Serial ports

2x 2-wire HS-UARTs
2x 4-wire UARTs

Other Interfaces

Up to 14 x GPI/Os
I2C Bus
SM Bus
1x SPI interface
FAN Management
Optional TPM 1.2 / 2.0
Power Management Signals

Power supply voltage: +5V$_{DC}$ and +3.3V_RTC

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97" x 3.23")

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.*
Please also check paragraph 5.1

2.3 Electrical Specifications

According to SMARC specifications, the SM-B69 module needs to be supplied only with an external +5V_{DC} power supply.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout). All remaining voltages needed for board's working are generated internally from +5V_{DC} power rail.

2.3.1 Power Consumption

SM-B69 module, like all SMARC modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source. Anyway, it has been possible to measure power consumption directly on VDD_IN power rail (5V_{DC}) that supplies the board. Power consumption must be intended as average value (30 seconds acquisition).

Status	Configuration				
	Intel Pentium N4200 4GB LPDDR4 32GB eMMC LVDS and HDMI 2xLAN controller i210	Intel Celeron N3350 2GB LPDDR4 32GB eMMC LVDS and HDMI 2xLAN controller i210	Intel Atom E3950 8GB LPDDR4 32GB eMMC LVDS and HDMI 2xLAN controller i210	Intel Atom E3940 4GB LPDDR4 32GB eMMC DP and eDP 2xLAN controller i210	Intel Atom E3930 2GB LPDDR4 8GB eMMC DP 1xLAN controller i210
Idle – (Win10) – power saving configuration	2.65W	2.69W	3.15W	2.59W	2.33W
OS Boot – (Win10)	3.69W	2.88W	3.63W	3.27W	2.6W
Video reproduction@1080p, power saving configuration	5.57W	3.91W	4.20W	4.15W	4.13W
Video reproduction 4K, power saving configuration	7.67W	5.68W	5.16W	7.23W	5.04W
7.09W	9.02W	7.12W	17.71W	12W	7.09W
Intel TAT (without power limit)	22.43W	14.28W	22.84W	15.88W	11W

Independently by the SOC mounted onboard, the following power consumptions are common to all boards:

Battery Backup power consumption: 4.7µA
Soft-Off State power consumption: TBM
Suspend State power consumption: TBM

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector. Also named 5V_DSW.
VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the I.MX 8M
+3.3V_DSW: +3.3 Always-on voltage, derived internally from 5V_DSW
+3.3V_RUN: +3.3 Switched voltage, derived internally from +3.3V_DSW
+3.3V_ALW: +3.3 Switched voltage, derived internally from +3.3V_DSW
+1.8V_ALW: +1.8 Always-on voltage, derived internally from 5V_DSW
+1.8V_RUN: +1.8 switched voltage, derived internally from +1.8V_ALW
+1.8V_DSW: +1.8 Always-on voltage, derived internally from +3.3V_DSW

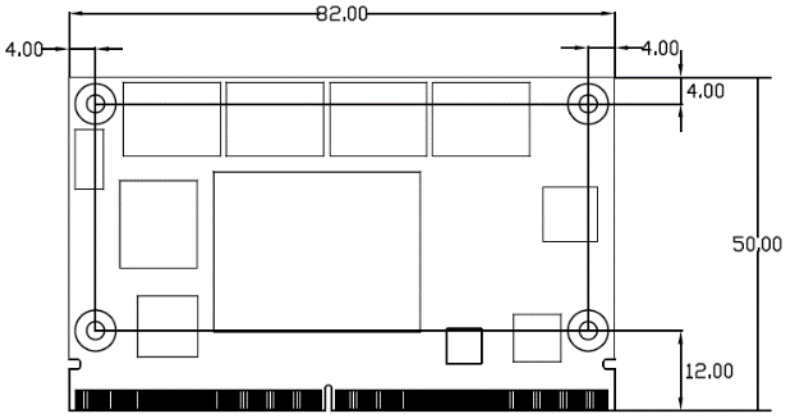
2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97” x 3.23”) including the pin numbering and edge finger pattern.

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of SM-B69 will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector’s height, if there is the need to place components on the carrier board in the zone below the SMARC module.



2.5 Supported Operating Systems

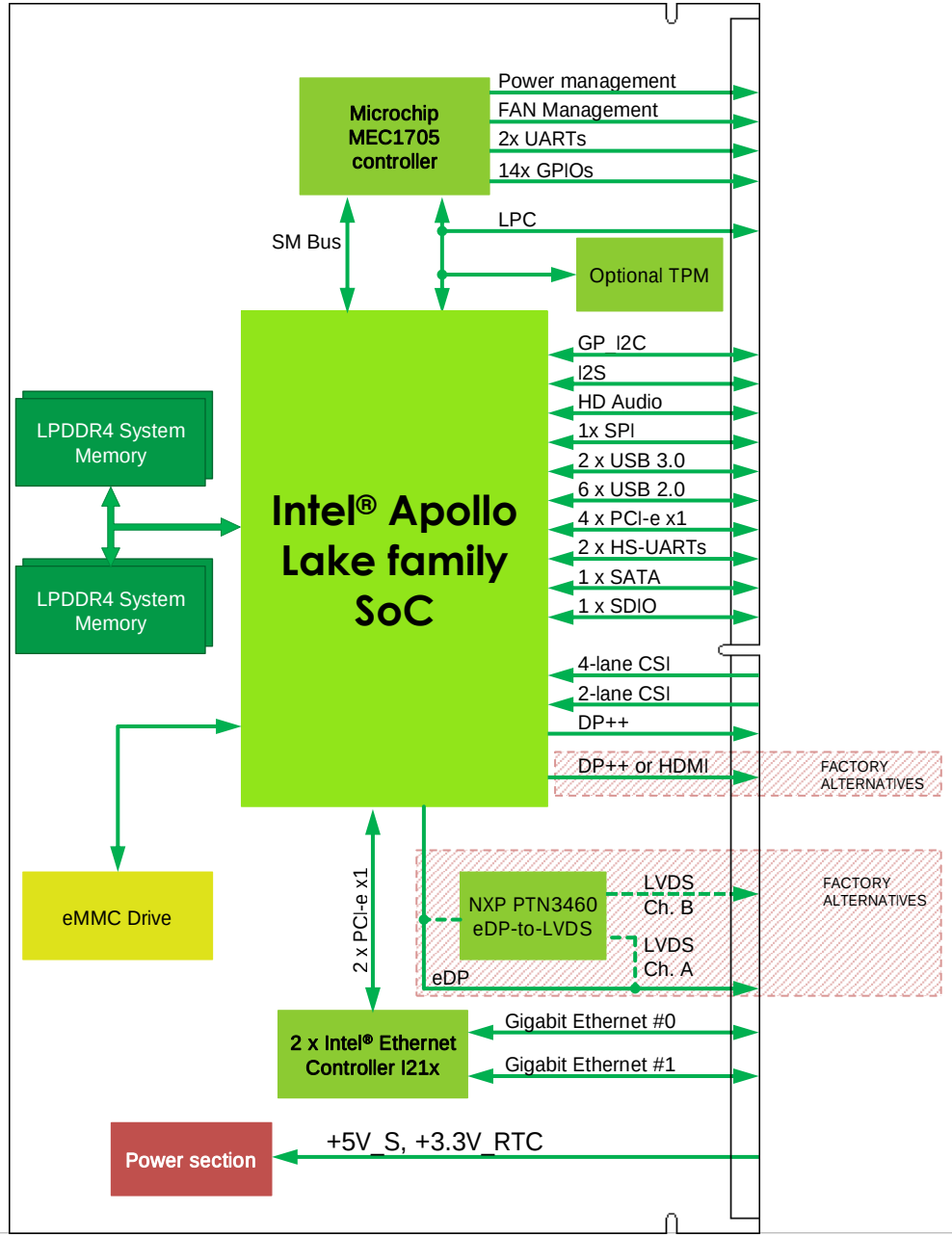
SM-B69 module supports the following operating systems:

- Microsoft® Windows 10 Enterprise (64 bit)
- Microsoft® Windows 10 IoT Core
- Linux
- Yocto

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC’s.

For further details, please visit https://www.seco.com.

2.6 Block Diagram



Chapter 3.
CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

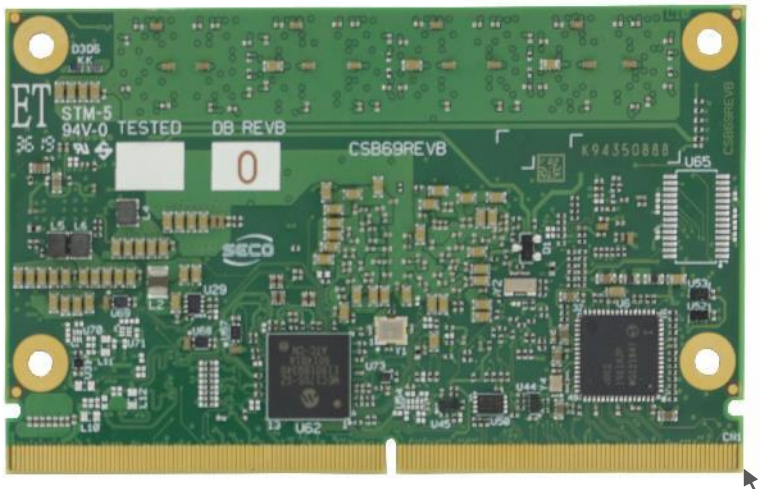
According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

TOP SIDE

Card edge golden finger, pin P1

Card edge golden finger, pin P156

BOTTOM SIDE



Card edge golden finger, pin S158

Card edge golden finger, pin S1

3.2 Connectors description

3.2.1 SMARC Connector

According to SMARC Rel 2.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC Rel 2.1 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

For accurate signals description, please consult the following paragraphs.

SMARC Golden Finger Connector - CN4							
TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C_CAM1_CK	I/O	CAMERA
MANAGEMENT	I	SMB_ALERT_1V8#	P1	S2	I2C_CAM1_DAT	I/O	CAMERA
		GND	P2	S3	GND		
CAMERA	I	CSI1_CK+	P3	S4	RSVD		
CAMERA	I	CSI1_CK-	P4	S5	I2C_CAM0_CK	I/O	CAMERA
GBE	I	GBE1_SD+	P5	S6	CAM_MCK	O	CAMERA
GBE	I	GBE0_SD+	P6	S7	I2C_CAM0_DAT	I/O	CAMERA
CAMERA	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CAMERA
CAMERA	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CAMERA
		GND	P9	S10	GND		
CAMERA	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CAMERA
CAMERA	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CAMERA
		GND	P12	S13	GND		
CAMERA	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CAMERA
CAMERA	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CAMERA
		GND	P15	S16	GND		
CAMERA	I	CSI1_RX3+	P16	S17	GBE1_MDI0+		

CAMERA	I	CSI1_RX3-	P17	S18	GBE1_MDI0-		
		GND	P18	S19	GBE1_LINK100#		
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+		
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-		
GBE	O	GBE0_LINK100#	P21	S22	GBE1_LINK1000#		
GBE	O	GBE0_LINK1000#	P22	S23	GBE1_MDI2+		
GBE	I/O	GBE0_MDI2-	P23	S24	GBE1_MDI2-		
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3+		
GBE	I/O	GBE0_MDI1-	P26	S27	GBE1_MDI3-		
GBE	I/O	GBE0_MDI1+	P27	S28	N.C.		
		N.C.	P28	S29	PCIE_D_TX+		
GBE	I/O	GBE0_MDI0-	P29	S30	PCIE_D_TX-		
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#		
		N.C.	P31	S32	PCIE_D_RX+		
		GND	P32	S33	PCIE_D_RX-		
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	N.C.		
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	AUDIO_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	N.C.		
SPI_INTERFACE	O	SPI0_CS0#	P43	S44	N.C.		
SPI_INTERFACE	O	SPI0_CK	P44	S45	N.C.		
SPI_INTERFACE	I	SPI0_DIN	P45	S46	N.C.		
SPI_INTERFACE	O	SPI0_DO	P46	S47	GND		

		GND	P47	S48	I2C_GP_CK	I/O	I2C
S-ATA	I	SATA_TX+	P48	S49	I2C_GP_DAT	I/O	I2C
S-ATA	I	SATA_TX-	P49	S50	HDA_SYNC	I/O	AUDIO
		GND	P50	S51	HDA_SDO	O	AUDIO
S-ATA	O	SATA_RX+	P51	S52	HDA_SDI	I	AUDIO
S-ATA	O	SATA_RX-	P52	S53	HDA_CK	I/O	AUDIO
		GND	P53	S54	SATA_ACT#	I	S-ATA
		N.C.	P54	S55	USB5_EN_OC#	I/O	USB
		N.C.	P55	S56	N.C.		
		N.C.	P56	S57	N.C.		
		N.C.	P57	S58	N.C.		
		N.C.	P58	S59	USB5+	I/O	USB
		GND	P59	S60	USB-	I/O	USB
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	USB3_SSTX+	O	USB
USB	I/O	USB0_EN_OC#	P62	S63	USB3_SSTX-	O	USB
USB	O	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	USB3_SSRX+	I	USB
USB	I/O	USB1+	P65	S66	USB3_SSRX-	I	USB
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
		RSVD	P72	S73	GND		
		RSVD	P73	S74	USB2_SSRX+	I	USB
USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCI_e
USB	I/O	USB4_EN_OC#	P76	S77	PCIE_C_RST#	O	PCI_e

PCI_e	I/O	PCIE_B_CKREQ#	P77	S78	PCIE_C_RX+	I	PCI_e
PCI_e	I/O	PCIE_A_CKREQ#	P78	S79	PCIE_C_RX-	I	PCI_e
		GND	P79	S80	GND		
PCI_e	O	PCIE_C_REFCK+	P80	S81	PCIE_C_TX+	O	PCI_e
PCI_e	O	PCIE_C_REFCK-	P81	S82	PCIE_C_TX-	O	PCI_e
		GND	P82	S83	GND		
PCI_e	O	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	O	PCI_e
PCI_e	O	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	O	PCI_e
		GND	P85	S86	GND		
PCI_e	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCI_e
PCI_e	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCI_e
		GND	P88	S89	GND		
PCI_e	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCI_e
PCI_e	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCI_e
		GND	P91	S92	GND		
DISPLAY	O	HDMI_D2+	P92	S93	DP0_LANE0+	O	DISPLAY
DISPLAY	O	HDMI_D2-	P93	S94	DP0_LANE0-	O	DISPLAY
		GND	P94	S95	DP0_AUX_SEL	I	DISPLAY
DISPLAY	O	HDMI_D1+	P95	S96	DP0_LANE1+	O	DISPLAY
DISPLAY	O	HDMI_D1-	P96	S97	DP0_LANE1-	O	DISPLAY
		GND	P97	S98	DP0_HPD	I	DISPLAY
DISPLAY	O	HDMI_D0+	P98	S99	DP0_LANE2+	O	DISPLAY
DISPLAY	O	HDMI_D0-	P99	S100	DP0_LANE2-	O	DISPLAY
		GND	P100	S101	GND		
DISPLAY	O	HDMI_CK+	P101	S102	DP0_LANE3+	O	DISPLAY
DISPLAY	O	HDMI_CK-	P102	S103	DP0_LANE3-	O	DISPLAY
		GND	P103	S104	N.C.		
DISPLAY	I	HDMI_HPD	P104	S105	DP0_AUX+	I/O	DISPLAY
DISPLAY	I/O	HDMI_CTRL_CK	P105	S106	DP0_AUX-	I/O	DISPLAY
DISPLAY	I/O	HDMI_CTRL_DAT	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT

DISPLAY	I	DP1_AUX_SEL	P107	S108	LVDS1_CK+	O	DISPLAY
GPIO	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK-	O	DISPLAY
GPIO	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+	O	DISPLAY
GPIO	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0-	O	DISPLAY
GPIO	I/O	GPIO4 / HDA_RST#	P112	S113	eDP1_HPD	I	DISPLAY
GPIO	I/O	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+	O	DISPLAY
GPIO	I/O	GPIO6 / TACHIN	P114	S115	LVDS1_1-	O	DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+	O	DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2-	O	DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+	O	DISPLAY
		GND	P120	S121	LVDS1_3-	O	DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_0+ / eDP0_TX0+	O	DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_0- / eDP0_TX0-	O	DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT
MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_1+ / eDP0_TX1+	O	DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_1- / eDP0_TX1-	O	DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_2+ / eDP0_TX2+	O	DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_2- / eDP0_TX2-	O	DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+ / eDP0_AUX+	O	DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK- / eDP0_AUX-	O	DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_3+ / eDP0_TX3+	O	DISPLAY

ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_3- / eDP0_TX3-	O	DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
		N.C.	P143	S144	eDP0_HPD	I	DISPLAY
		N.C.	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
		N.C.	P145	S146	PCIE_WAKE#	I	PCI_e
		N.C.	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT
		VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
		VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
		VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
		VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
		VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
		VDD_IN	P156	S157	TEST#	I	MANAGEMENT
				S158	GND		

3.2.1.1 LCD Display Support Signals

The Intel® family of SOCs formerly coded as Apollo Lake offers signal for direct driving of panels and its display's backlight: enabling signals for both panels (LCD0_VDD_EN and LCD1_VDD_EN) and both backlights (LCD0_BKLT_EN and LCD1_BKLT_EN), Backlight Brightness Control signals (LCD0_BKLT_PWM and LCD1_BKLT_PWM). These signals have an electrical of +1.8V_RUN, so they will be adapted/level shifted by the carrier board for external use.

There are also the signals necessary for driving I2C Data and Clock lines of LCD EDID EEPROM.

The panel control signals are:

LCD0_VDD_EN: Panel #0 Panel enable signal. Set high to enable. +1.8V_RUN electrical level Output.

LCD0_BKLT_EN: Panel #0 Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #0 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

LCD1_VDD_EN: Panel #1 Panel Power signal enable signal. Set high to enable. +1.8V_RUN electrical level Output

LCD1_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

LCD1_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM.

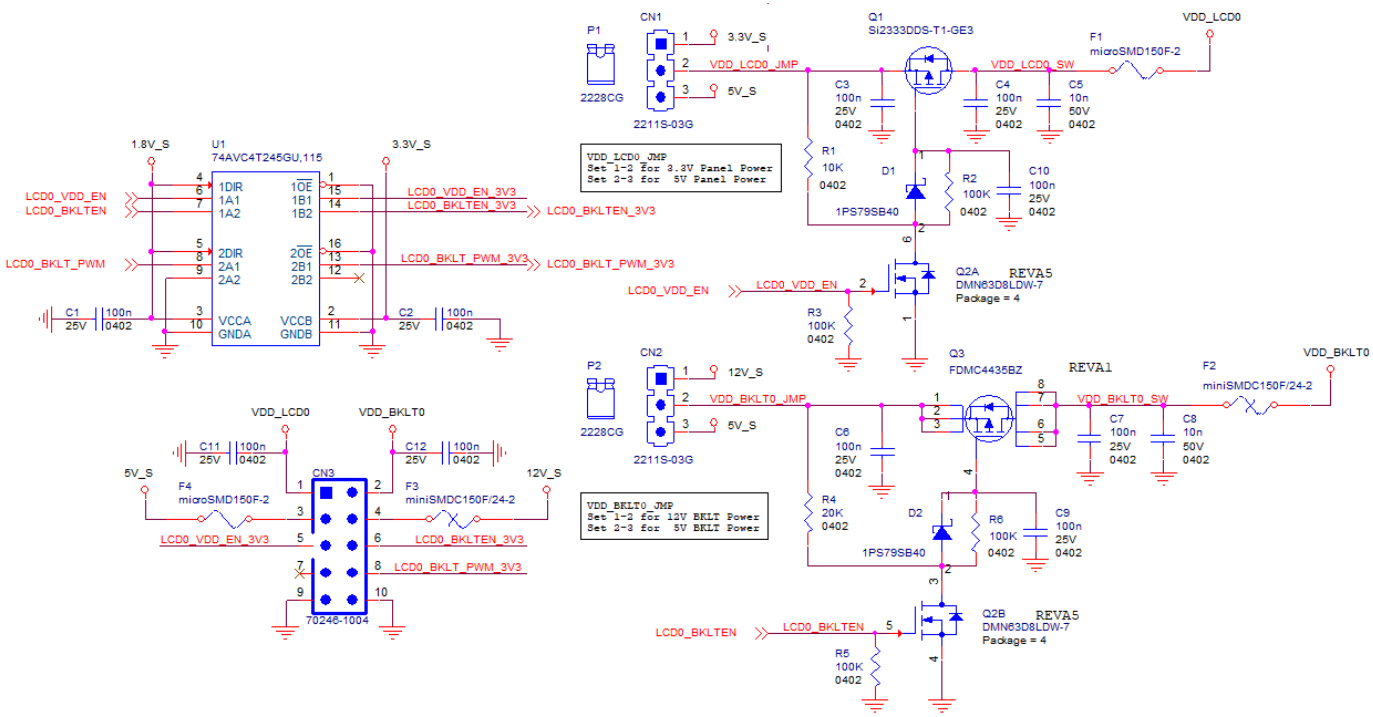
I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM.

Please refer to the following schematics as an example of implementation for LCD and backlight support signals driving connection + voltage level shifters on the carrier board.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design



3.2.1.2 eDP / Dual Channel LVDS (factory alternatives)

The Intel® family of SOCs formerly coded as Apollo Lake offers a wide range of single and multi-purpose Digital Display Interfaces, which allow the implementation of embedded Display Port (eDP) interface or Dual Channel LVDS, HDMI or Display Port (DP), and two Camera Serial Inputs (CSI)

The LVDS interface, which is frequently used in many application fields, is not directly supported by the SOC.

For this reason, considering that LVDS dual channel interfaces can be factory alternative on the same pins with eDP interface, on SM-B69 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode). Such an interface is derived from the SOCs' dedicated eDP Interface.

!

Please remember that LVDS interface is not native for the Intel® family of SOCs formerly coded as Apollo Lake, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS or eDP interface.

Please take care of specifying if it is necessary LVDS interface or eDP, before placing an order of SM-B69 module.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for Channel #0 are LVDS:

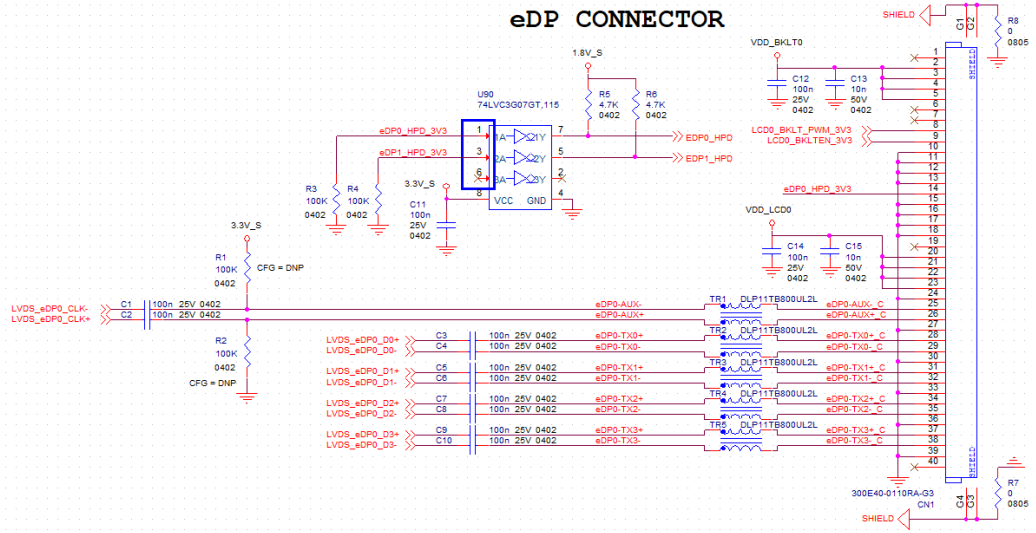
LVDS0_0+/LVDS0_0-: LVDS Channel #0 differential data pair #0.
LVDS0_1+/LVDS0_1-: LVDS Channel #0 differential data pair #1.
LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2.
LVDS0_3+/LVDS0_3-: LVDS Channel #0 differential data pair #3.
LVDS0_CK+/LVDS0_CK-: LVDS Channel #0 differential Clock.

OR the signals for Channel #0 are eDP:

eDP0_TX0+/ eDP0_TX0-: eDP Channel #0 differential data pair #0.
eDP0_TX1+/ eDP0_TX1-: eDP Channel #0 differential data pair #1.
eDP0_TX2+/ eDP0_TX2-: eDP Channel #0 differential data pair #2.
eDP0_TX3+/ eDP0_TX3-: eDP Channel #0 differential data pair #3.
eDP0_AUX+/ eDP0_AUX-: eDP Channel #0 differential Clock.

eDP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_S electrical level from carrier board with a 100kΩ pull-down resistor

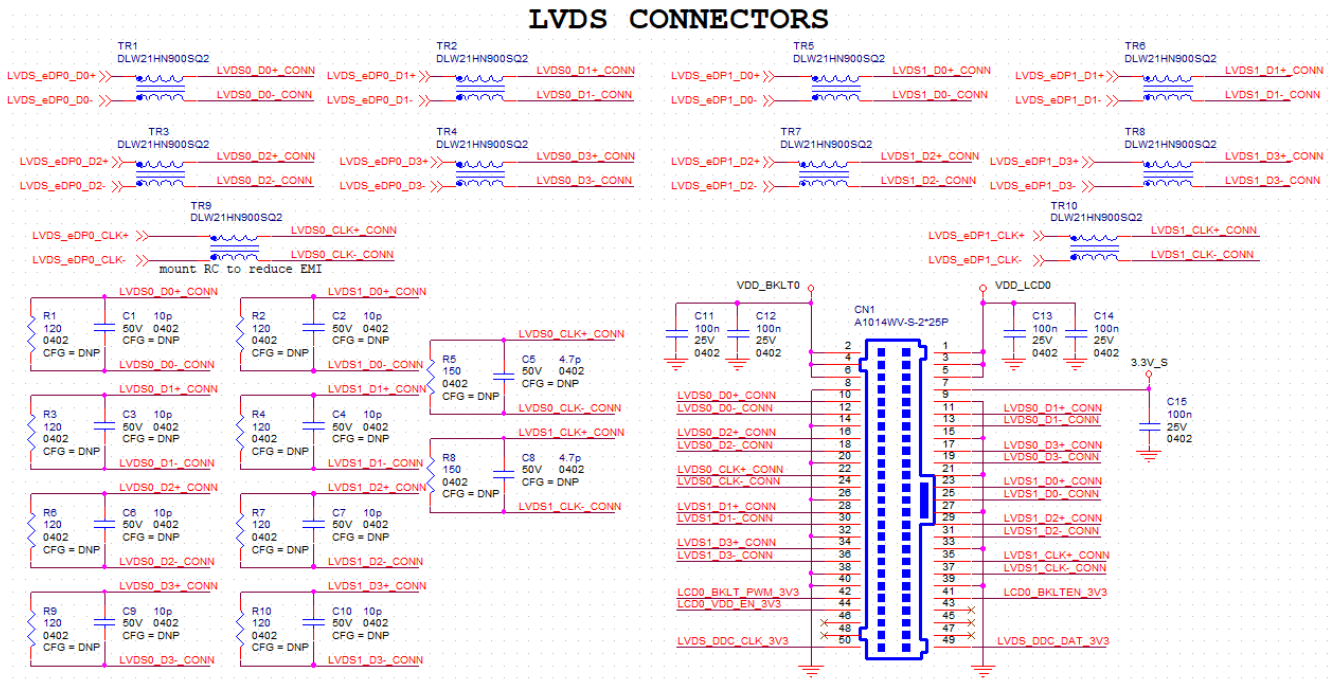
Please refer to the following schematics as an example of connection of eDP interface on the carrier board. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation.



The signals for Channel #1 are LVDS, when this interface is selected in factory board configuration, otherwise these pins will be not connected.

LVDS1_1+ / LVDS1_0- : LVDS Channel #1 differential data pair #0
LVDS1_1+/ LVDS1_1-: LVDS Channel #1 differential data pair #1
LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2
LVDS1_3+/ LVDS1_3-: LVDS Channel #1 differential data pair #3
LVDS1_CK+/ LVDS1_CK-: LVDS Channel #1 differential Clock

Please refer to the following schematics as an example of connection of LVDS interface on the carrier board, with EMI filtering section included.



3.2.1.3 HDMI / DP++ (factory alternatives) interface signals

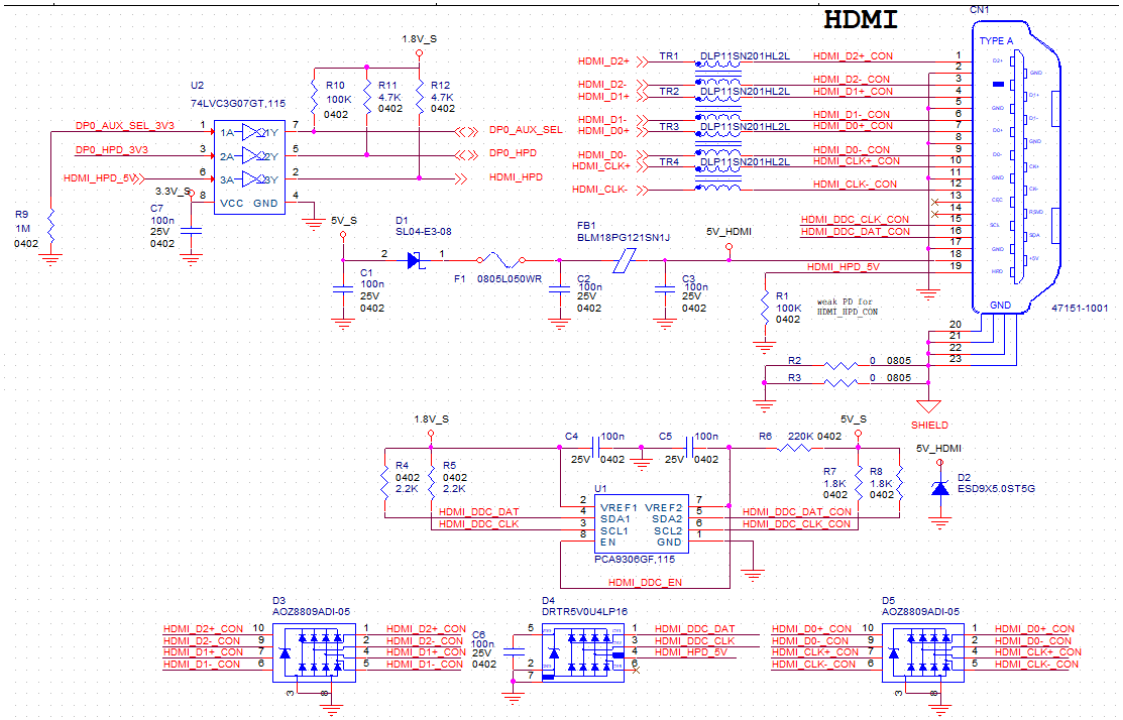
As described in the previous paragraph, the Intel® family of SOCs formerly coded as Apollo Lake offers a native multimode Digital Display Interface, configurable as a factory alternative to work as Display Port (DP) with a resolution up to 4096 x 2160 @60Hz or HDMI v1.4 with a resolution up to 3840 x 2160 @30Hz.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for the Channel are HDMI:

HDMI_D0+/HDMI_D0-: HDMI Output Differential Pair #0
HDMI_D1+/HDMI_D1-: HDMI Output Differential Pair #1
HDMI_D2+/HDMI_D2-: HDMI Output Differential Pair #2
HDMI_CK+/HDMI_CK-: HDMI Differential Clock

HDMI_HPD: Hot Plug Detect, Active high Input signal of +1.8V_S electrical level from carrier board with a 100kΩ pull-down resistor
HDMI_CTRL_CK: DDC Clock line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor
HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor



Please refer to the above schematics as an example of connection of HDMI interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression, as well as common mode choke inductors for EMI purpose. Voltage level shifters are necessary on Control data/Clock signals, as well as for Hot Plug Detect signal.

OR the signals for the Channel are eDP:

DP1_LANE0+/ DP1_LANE0-: DP Channel #1 Output Differential Pair #0

DP1_LANE1+/ DP1_LANE1-: DP Channel #1 Output Differential Pair #1

DP1_LANE2+/ DP1_LANE2-: DP Channel #1 Output Differential Pair #2

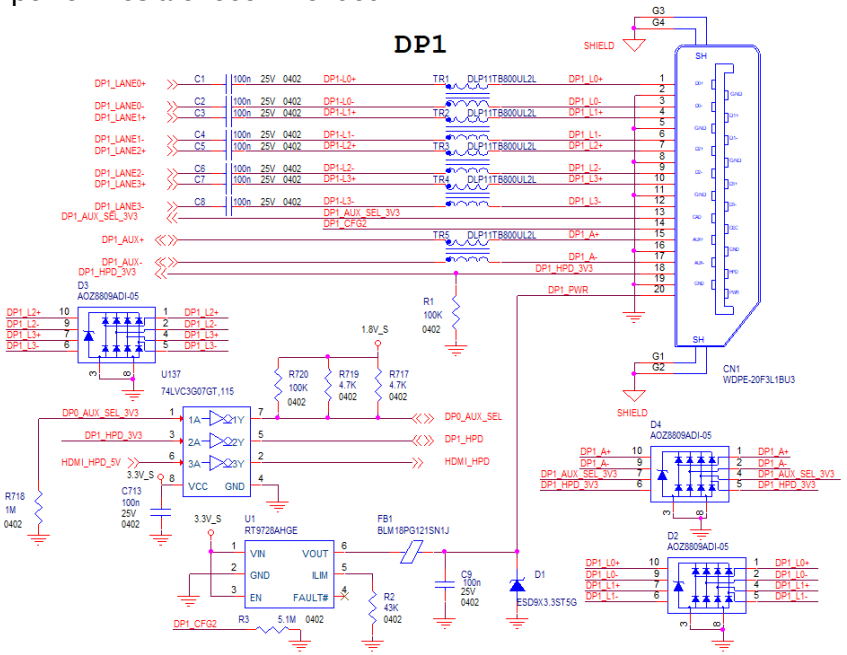
DP1_LANE3+/ DP1_LANE3-: DP Channel #1 Output Differential Pair #3

DP1_AUX+: DDC Clock line for DP Channel #1. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

DP1_AUX-: DDC Data line for DP Channel #1. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

DP1++_AUX_SEL: Select input signal to switch between I2C Clock/Data for HDMI (low level) and Display Port Auxiliary Channel for DP/HDMI (high level)

Please refer to the following schematics as an example of connection of DP interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation. Switch with settable current limit on power lines are recommended.



3.2.1.4 DP++ interface signals

As described in the previous paragraph, the Intel® family of SOCs formerly coded as Apollo Lake offers a native Display Port (DP) interface, with a resolution up to 4096 x 2160 @60Hz

The signals related to DP++ are as follows:

DP0_LANE0+/ DP0_LANE0-: DP Channel #0 differential data pair #0.

DP0_LANE1+/ DP0_LANE1-: DP Channel #0 differential data pair #1.

DP0_LANE2+/ DP0_LANE2-: DP Channel #0 differential data pair #2.

DP0_LANE3+/ DP0_LANE3-: DP Channel #0 differential data pair #3.

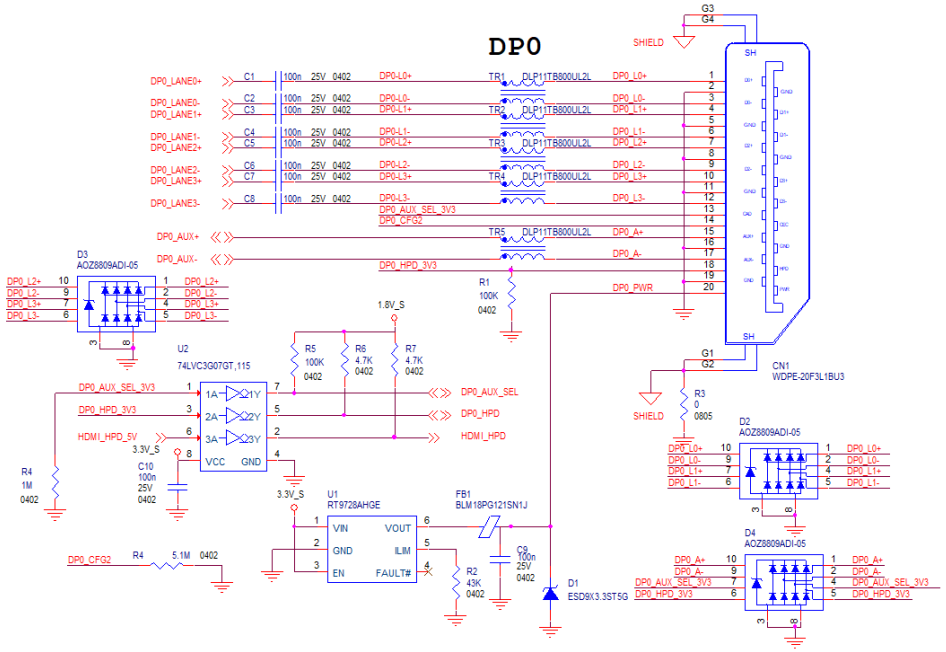
DP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_S electrical level from carrier board with a 100kΩ pull-down resistor

DP0_AUX+: DDC Clock line for DP Channel #0. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

DP0_AUX-: DDC Data line for DP Channel #0. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

DP0++_AUX_SEL: Select input signal to switch between I2C Clock/Data for HDMI (low level) and Display Port Auxiliary Channel for DP/HDMI (high level)

Please refer to the following schematics as an example of connection of DP interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression. Hot Plug Detect signal must be buffered to prevent back feeding of power from the display to the module as well as level translation. Switch with settable current limit on power lines are recommended.



3.2.1.5 Serial Cameras

The Intel® family of SOCs formerly coded as Apollo Lake contains a processing subsystems (PS) which is an advanced Image Signal Processor (ISP) and the Input Subsystems (IS) composed by two MIPI – CSI2 controllers, supporting imaging sensors connected to it.

There are two MIPI-CSI2 interfaces available. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair

CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0

CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair

CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0

CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1

CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2

CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

I2C_CAM0_CK: I2C control interface clock signal to configure the camera sensor for MIPI-CSI #0. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

I2C_CAM0_DAT: I2C control interface data signal to configure the camera sensor for MIPI-CSI #0. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

I2C_CAM1_CK: I2C control interface clock signal to configure the camera sensor for MIPI-CSI #1. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

I2C_CAM1_DAT: I2C control interface data signal to configure the camera sensor for MIPI-CSI #1. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN.

CAM_MCK: master clock output for CSI camera support from the SMARC carrier board.

3.2.1.6 SATA interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers two S-ATA interfaces, but one of them is internally multiplexed with USB 3.0 and used for this purpose.

The interfaces are Gen3 compliant, with support of 1.5Gbps, 3.0 Gbps and 6.0 Gbps data rates

Here following the signals related to SATA interface:

SATA_TX+/SATA_TX-: Serial ATA Channel #1 Transmit differential pair

SATA_RX+/SATA_RX-: Serial ATA Channel #1 Receive differential pair

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_RUN voltage

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to a SATA M 7p connector or switched for an M.2 SSD Slot, which allow plugging M.2 Socket 2 Key B Solid State Drives. Please refer to the following schematics as an example of connection of SATA interface on the carrier board to selected connector.

3.2.1.7 SDI/O interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers one SD Card controller, able to support SD Card 3.0 interface.

Such an SD controller complies with SD Host Controller Standard Specification version 3.01.

The SD port is externally accessible through the SD Card Slot connector, can work in 1-bit and 4-bit mode operation with data rate up to 104MB/s

The signals related to SDIO are as follows:

SDIO_WP: Write Protect input, electrical level +3.3V_RUN with 10kΩ pull-up resistor. It is used to communicate the status of Write Protect switch of the external SD card. Since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal must be tied to GND, otherwise the OS will always consider the card as protected from writing.

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_RUN, used to send command from Host (Intel processor) to the connected card, and to send the response from the card to the Host.

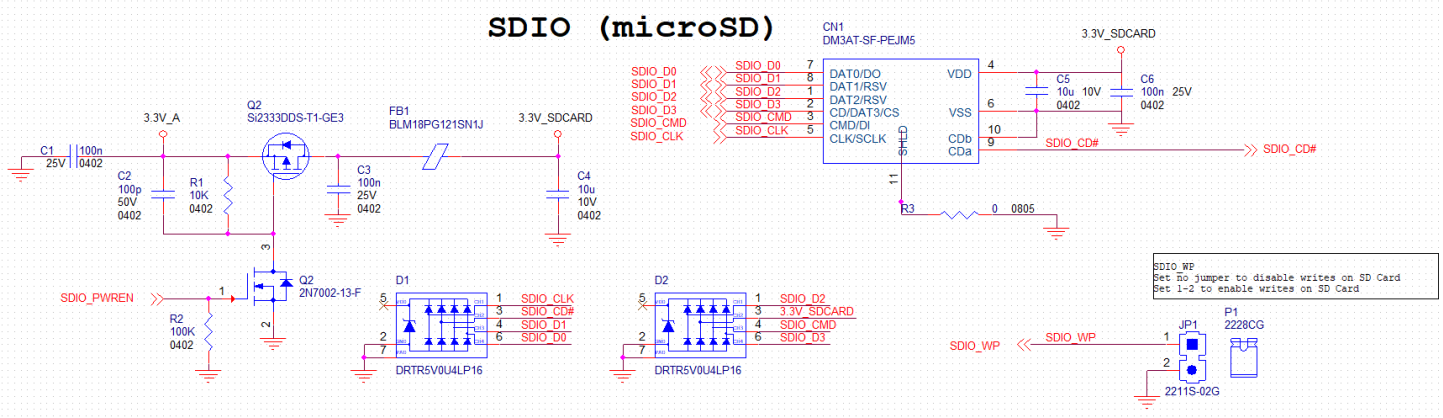
SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), 50 MHz maximum frequency for SD/SDIO High Speed Mode.

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +3.3V_RUN with 10kΩ pull-down resistor. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SD Card data bus. SDIO_D0 signal is used for all communication modes. SDIO_[D1÷D3] signals are required for 4-bit communication mode.

Please refer to the following schematics as an example of connection of SDIO interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression.



3.2.1.8 SPI interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of EEPROMs and Serial Flash devices.

SPI interface supports master mode only can support speed up to 25Mbps.

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI channel #0 primary Chip select, active low output signal. Electrical level +1.8V_RUN

SPI0_CK: SPI channel #0 Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_RUN

SPI0_DIN: SPI0 channel #0 Master Data Input, electrical level +1.8V_RUN.

SPI0_DO: SPI0 channel #0 Master Data Output, electrical level +1.8V_RUN.

3.2.1.9 Audio interface signals

The Intel® family of SOCs formerly coded as Apollo Lake supports I2S audio format, thanks to native support offered by the processor to this audio codec standard.

Here are following the signals related to I2S Audio interface:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

All these signals have to be connected, on the Carrier Board, to an I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

The Intel® family of SOCs formerly coded as Apollo Lake supports also HD audio format, thanks to native support offered by the processor to this audio codec standard.

Here are following the signals related to HD Audio interface:

HDA_SYNC: Synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

HDA_SDO: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

HDA_SDI: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

HDA_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

HDA_RST#: Digital Audio Reset. This signal is multiplexed with GPIO4. This pin has to be defined via BIOS so that GPIO4/HDA_RST# is in HDA_RST# modality.

All these signals have to be connected, on the Carrier Board, to an HD Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.1.10 I2C Interface

The Intel® family of SOCs formerly coded as Apollo Lake supports GPIO I2C interface.

Here are following the signals related to I2C Audio interface:

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

3.2.1.11 Asynchronous Serial Ports (UART) interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers in its Low Power Sub System (LPSS) two high speed UART, with a maximum speed of 115,200 kb/s or 3.6864Mb/s depending on Industry standards.

In addition, two additional UART are offered and managed by the Embedded controller MEC1705 from Microchip

SER0_TX: UART #0 Interface, Serial data Transmit (output) line, 1.8V_DSW electrical level. It is managed by Microchip MEC1705 controller.

SER0_RX: UART #0 Interface, Serial data Receive (input) line, 1.8V_DSW electrical level. It is managed by Microchip MEC1705 controller.

SER0_RTS#: UART #0 Interface, Handshake signal, Request to Send (output) line, 1.8V_DSW electrical level

SER0_CTS#: UART #0 Interface, Handshake signal, Clear to Send (Input) line, 1.8V_DSW electrical level

SER1_TX: HS-UART #0 Interface, Serial data Transmit (output) line, 1.8V_DSW electrical level. It is directly managed by Intel processor.

SER1_RX: HS-UART #0 Interface, Serial data Receive (input) line, 1.8V_DSW electrical level. It is directly managed by Intel processor.

SER2_TX: UART #1 Interface, Serial data Transmit (output) line, 1.8V_DSW electrical level. It is managed by Microchip MEC1705 controller.

SER2_RX: UART #1 Interface, Serial data Receive (input) line, 1.8V_DSW electrical level. It is managed by Microchip MEC1705 controller.

SER2_RTS#: UART #1 Interface, Handshake signal, Request to Send (output) line, 1.8V_DSW electrical level.

SER2_CTS#: UART #1 Interface, Handshake signal, Clear to Send (Input) line, 1.8V_DSW electrical level.

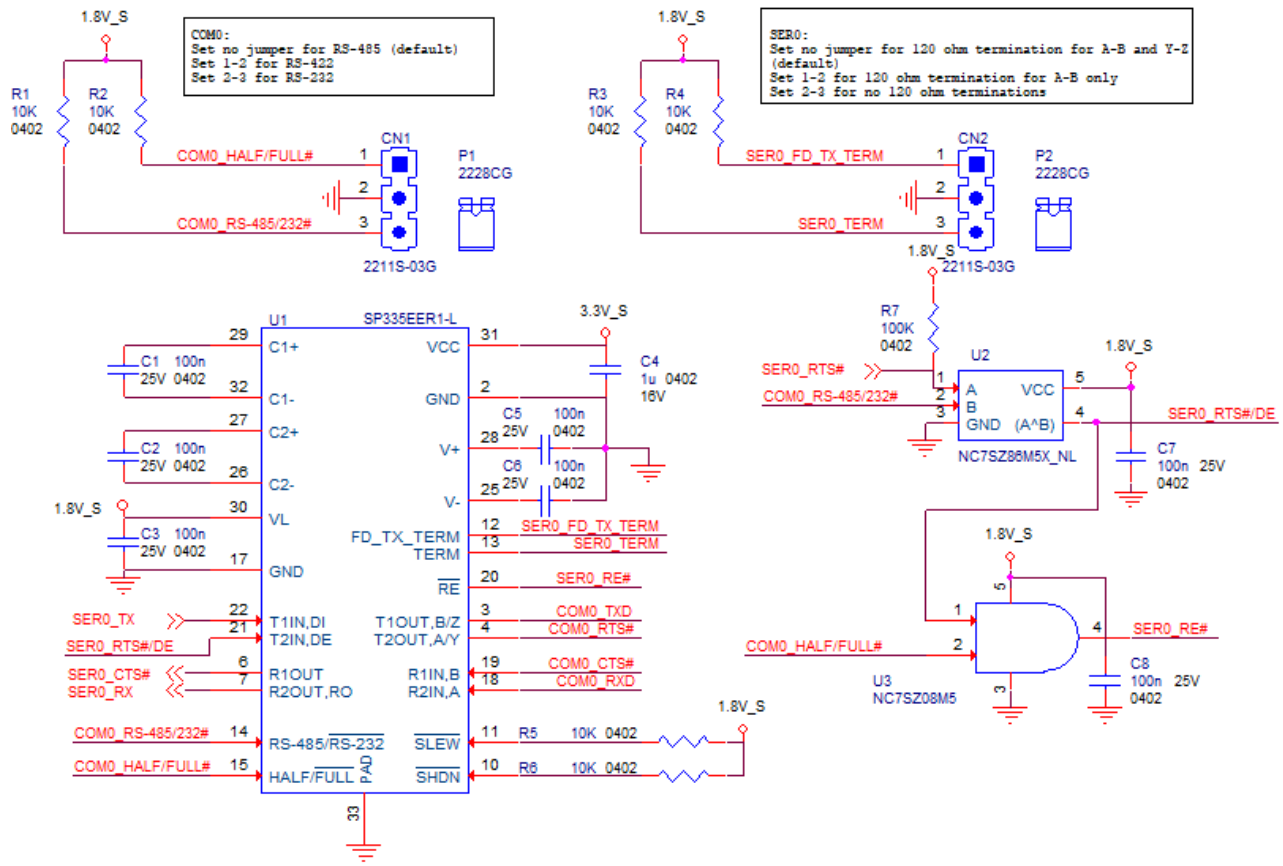
SER3_RX: HS-UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level. It is directly managed by Intel processor.

SER3_TX: HS-UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level. It is directly managed by Intel processor.

Please consider that interface is at +1.8V_DSW electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_DSW level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

In the following schematic here is an example of UART interface on the carrier board, with a multiprotocol transceiver allowing to support RS485/RS-422/RS-232 serial interfaces.

SER #0


COM0:
Set no jumper for RS-485 (default)
Set 1-2 for RS-422
Set 2-3 for RS-232
SER0:
Set no jumper for 120 ohm termination for A-B and Y-Z (default)
Set 1-2 for 120 ohm termination for A-B only
Set 2-3 for no 120 ohm terminations
1.8V_S
R1 10K 0402
R2 10K 0402
R3 10K 0402
R4 10K 0402
CN1
CN2
P1 2228CG
P2 2228CG
2211S-03G
COM0_HALF/FULL#
COM0_RS-485/232#
SER0_FD_TX_TERM
SER0_TERM
U1
SP335EER1-L
3.3V_S
C1 100n 25V 0402
C2 100n 25V 0402
C3 100n 25V 0402
C4 1u 0402 16V
C5 100n 25V 0402
C6 100n 25V 0402
C1+
C1-
C2+
C2-
VL
GND
VCC
V+
V-
FD_TX_TERM
TERM
RE
T1IN,DI
T2IN,DE
R1OUT
R2OUT,RO
T1OUT,B/Z
T2OUT,A/Y
R1IN,B
R2IN,A
RS-485/RS-232
HALF/FULL
SLEW
SHDN
SER0_TX
SER0_RTS#/DE
SER0_CTS#
SER0_RX
SER0_RE#
COM0_TXD
COM0_RTS#
COM0_CTS#
COM0_RXD
R5 10K 0402
R6 10K 0402
R7 100K 0402
U2
NC7SZ86M5X_NL
C7 100n 25V 0402
C8 100n 25V 0402
U3
NC7SZ08M5

3.2.1.12 USB interface signals

The Intel® family of SOCs formerly coded as Apollo Lake offers an xHCI controller, which is able to manage up to 6 Superspeed ports (i.e. USB 3.0 compliant) and up to 8 ports in USB 2.0 mode only, one of them also capable of OTG.

In SM-B69, there are up to 4 ports in USB2.0 only and up to 2 Super Speed (SS) ports (i.e. USB 3.0 compliant). One of USB 2.0 port has also OTG capabilities.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus 2.0 Port #0 differential pair (directly managed by Intel processor)

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for over current operation information.

USB0_VBUS_DET: USB Voltage Bus detection from Carrier Board. Input, electrical level +5V.

USB0_OTG_ID: USB OTG Input, electrical level +3.3V_ALW. When USB Port #0 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low). It must be tied to GND when USB Port #0 has to be set to work in Host mode. When not driven, USB Port#0 will work in Client mode.

USB1+/ USB1-: Universal Serial Bus Port 2.0 #2 differential pair.

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port 2.0 #1 differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port 2.0 #5 differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB4+/USB4-: Universal Serial Bus Port 2.0 #4 differential pair.

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

USB5+/USB5-: Universal Serial Bus Port 2.0 #3 differential pair.

USB5_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC 2.1 Specification for OC operation information.

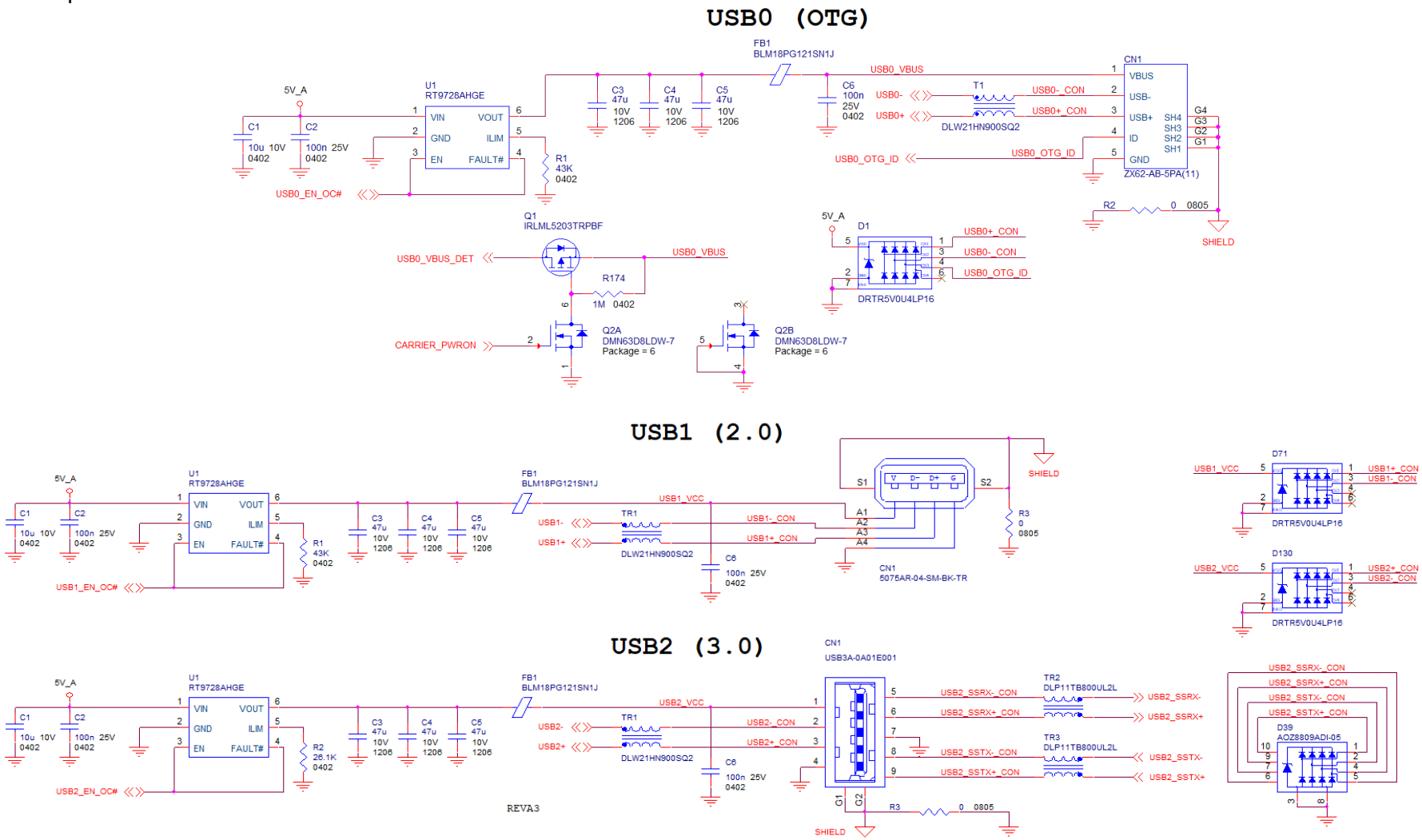
USB2_SSTX+/ USB2_SSTX-: USB 3.0 Port #1 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB 3.0 Port #1 Superspeed Receive differential pair.

USB3_SSTX+/ USB3_SSTX-: USB 3.0 Port #5 Superspeed Transmit differential pair.

USB3_SSRX+/ USB3_SSRX-: USB 3.0 Port #5 Superspeed Receive differential pair.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. Switch with settable current limit on power lines are recommended.



3.2.1.13 PCI Express interface signals

The SM-B69 module can offer externally four PCI Express lane, which are directly managed by the Intel® family of SOCs formerly coded as Apollo Lake.

PCI express Gen 2.0 (5Gbps) is supported.

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_A_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_ALW electrical level. it can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_A_CKREQ#: PCI Express Port A clock request signal, used from a PCI-e device to request the need for PCI Express Reference Clock. Bidirectional signal, +3.3V_RUN electrical level with a 20k pull-up resistor.

PCIE_B_RX+/ PCIE_B_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE_B_TX+/PCIE_B_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE_B_REFCK+/ PCIE_B_REFCK-: PCI Express Reference Clock for lane #1, Differential Pair

PCIE_B_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_ALW electrical level. it can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board. This signal is shared

PCIE_B_CKREQ#: PCI Express Port B clock request signal, used from a PCI-e device to request the need for PCI Express Reference Clock. Bidirectional signal, +3.3V_RUN electrical level with a 20k pull-up resistor.

PCIE_C_RX+/ PCIE_C_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE_C_TX+/PCIE_C_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE_C_REFCK+/ PCIE_C_REFCK-: PCI Express Reference Clock for lane #2, Differential Pair

PCIE_C_RST#: Reset Signal that is sent from SMARC Module to a PCI-e device available on the carrier board. Active Low, +3.3V_ALW electrical level. it can be used directly to drive externally a single RESET Signal. In case Reset signal is needed for multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_D_RX+/ PCIE_D_RX-: PCI Express lane #3, Receiving Input Differential pair

PCIE_D_TX+/PCIE_D_TX-: PCI Express lane #3, Transmitting Output Differential pair

PCIE_WAKE#: PCIe wake up interrupt to host input signal. Active low, +3.3V_ALW electrical level with a 10k pull-up resistor.

In the following table are shown the possible groupings allowed of the PCI-e lanes:

Allowed groupings	Lane #0	Lane #1	Lane #2	Lane #3
1 PCI-e x 4 port	√			
2 PCI- e x2	√		√	
1 PCI-e x 2 + 2 PCI-e x1	√		√	√
4 PCI-e x1	√	√	√	√

Please also be aware that this grouping cannot be changed dynamically, it is a fixed feature of the BIOS.
The customer in phase of order must select what grouping to have for PCI-e lanes.

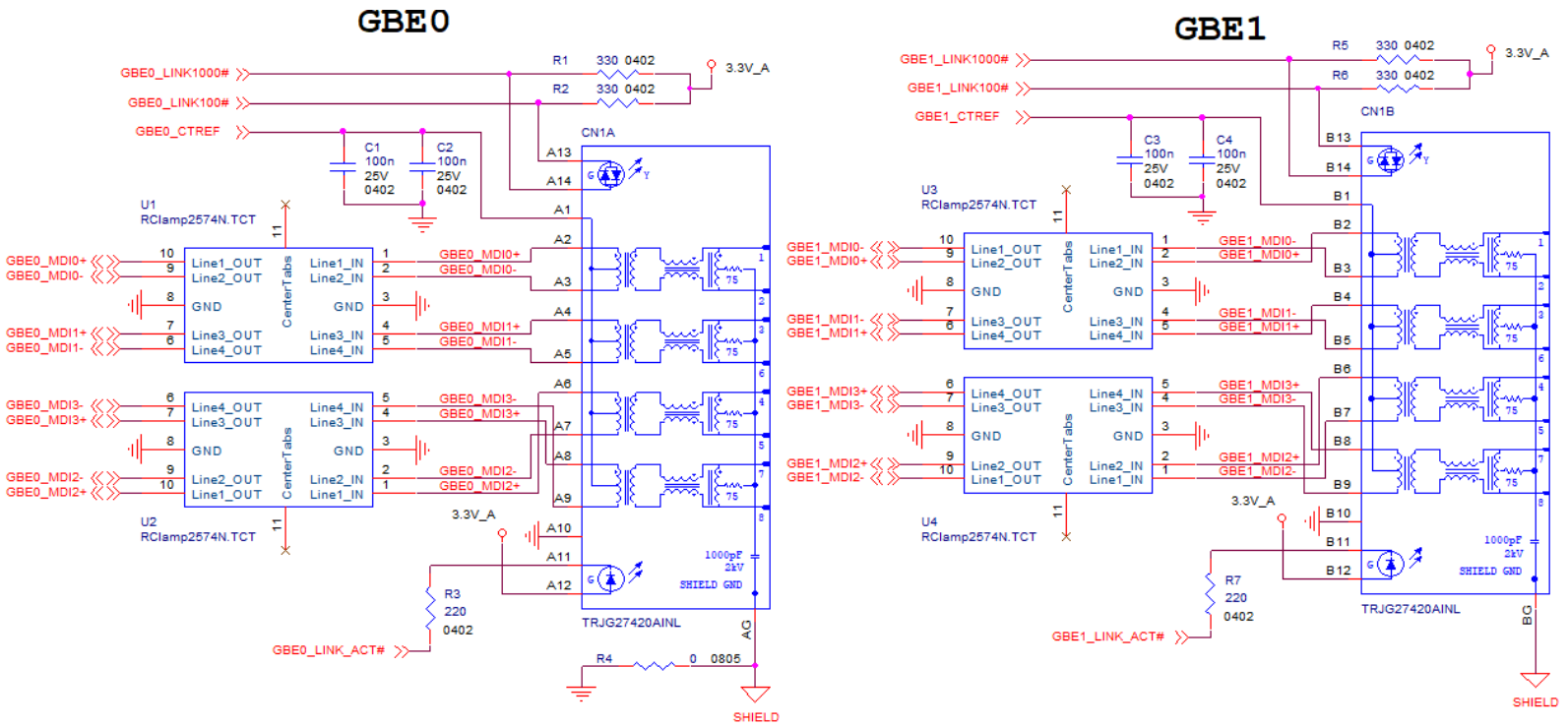
3.2.1.14 Gigabit Ethernet signals

Gigabit Ethernet interface is realized on SM-B69 module by using an Intel I210 Ethernet contoller, which is interfaced to Intel processor through a PCI interface.
Here following the signals involved in Gigabit Ethernet #0 management:
GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair
GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair
GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair
GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair
GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level
GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level
GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level
GBE0_SDP: Software defined pin, directly managed by Intel® Ethernet Controller I210 for Gigabit Ethernet #0
Here following the signals involved in Gigabit Ethernet #1 management:
GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair
GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair
GBE1_MDI2+/GBE1_MDI2-: Media Dependent Interface (MDI) Transmit differential pair
GBE1_MDI3+/GBE1_MDI3-: Media Dependent Interface (MDI) Transmit differential pair
GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level
GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_SDP: Software defined pin, directly managed by Intel® Ethernet Controller I210 for Gigabit Ethernet #1

Please refer to the following schematics as an example of connection of Ethernet interface on the carrier board, with TVS diodes specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I210x Gigabit Ethernet controller, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on SMARC connector



Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary, for both Gigabit Ethernet interfaces

3.2.1.15 Watchdog

WDT_TIME_OU: Watchdog timer Output. +1.8V_DSW electrical level

3.2.1.16 GPIO signals

The Embedded controller MEC1705 GPIO interface provides general purpose input monitoring and output control, as well as many other features for the GPIO described on datasheet.

The signals involved in GPIO management are:

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_DSW electrical level

GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_DSW electrical level

GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_DSW electrical level

GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_DSW electrical level

GPIO4 / HDA_RST#: General Purpose I/O #4, +1.8V_DSW electrical level

GPIO5 / PWM_OUT: General Purpose I/O #5, +1.8V_DSW electrical level

GPIO6 / TACHIN: General Purpose I/O #6, +1.8V_DSW electrical level

GPIO7: General Purpose I/O #7, +1.8V_DSW electrical level

GPIO8: General Purpose I/O #8, +1.8V_DSW electrical level

GPIO9: General Purpose I/O #9, +1.8V_DSW electrical level

GPIO10: General Purpose I/O #10, +1.8V_DSW electrical level

GPIO11: General Purpose I/O #11, +1.8V_DSW electrical level

GPIO12: General Purpose I/O #12, +1.8V_DSW electrical level

GPIO13: General Purpose I/O #13, +1.8V_DSW electrical level

3.2.1.17 Management pins

A set of signals are used by SM-B69 to communicate with carrier board for power management and indication status. Please refer to SMARC hardware specifications ver. 2.1 for more detailed informations.

The signals involved are:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board, active low signal from a voltage detection circuit

CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output is set to +1.8V_ALW electrical level with a 10k pull-down resistor

CARRIER_STBY#: Stand By command to the Carrier Board. Output, active low signal, is set to +1.8V_ALW electrical level with a 10k pull-down resistor

RESET_OUT#: General Purpose Reset. Output, active low signal, +1.8V_RUN electrical level

RESET_IN#: General Purpose Reset. Input, active low signal, +3.3_ALW electrical level with a 10k pull-up resistor

POWER_BTN#: Power Button. Input, active low signal, +3.3_ALW electrical level with a 10k pull-up resistor

SLEEP#: Sleep indicator from Carrier board. Input, active low signal, +3.3_ALW electrical level with a 10k pull-up resistor

LID#: LID Switch. Input, active low signal, +3.3_ALW electrical level with a 10k pull-up resistor

BATLOW#: Battery Low indication signal from the Carrier Board. Input, active low signal, +1.8V_DSW electrical level with a 10k pull-up resistor

I2C_PM_CK: Power Management I2C Clock. It is managed by Microchip MEC1705 controller. +1.8V_DSW electrical level with a 2k2 pull-up resistor

I2C_PM_DAT: Power Management I2C Data. It is managed by Microchip MEC1705 controller. +1.8V_DSW electrical level with a 2k2 pull-up resistor

CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, active low signal, +3.3V_DSW electrical level with a 10k pull-up resistor

CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, active low signal, +3.3V_DSW electrical level with a 2k2 pull-up resistor

TEST#: Signals used to invoke from Carrier Board specific test function(s). Input, active low signal, +3.3V_DSW electrical level with a 10k pull-up resistor. At the moment, this function is not implemented and reserved for its use in the future.

SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, active low signal, +1.8V_DSW electrical level with a 2k2 pull-up resistor

3.2.1.18 Boot Select

The following signals are active low and driven by open/ground circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_DSW electrical level with a 10k pull-up resistor

BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_DSW electrical level with a 10k pull-up resistor

BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_DSW electrical level with a 10k pull-up resistor

FORCE_RECOV#: Force recovery Mode. Input, +3.3_ALW electrical level with a 10k pull-up resistor

Chapter 4.
BIOS SETUP

- Aptio setup Utility
- Main setup menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu

4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. “Aptio Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
+ / -	+ and - keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F2>	Previous Values
<F3>	<F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted
<F4>	<F4> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub-screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Date / System Time

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Intel® I210 Gigabit Network Connection - MAC Address #1 *Other Network Connections - MAC Address #x*	See submenu	Configures settings for Boot Phase
Trusted Computing	See submenu	Trusted Computing Settings
ACPI Settings	See submenu	System ACPI parameters
Serial Port Console Redirection	See submenu	Serial Port Console Redirection
CPU Configuration	See submenu	CPU Configuration Parameters
AMI Graphic Output Protocol Policy	See submenu	User Selected Monitor Output by Graphic Output protocol
Network Stack Configuration	See submenu	Network Stack Settings
CSM Configuration	See submenu	Compatibility Support Module(CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc…
NVMe Configuration	See submenu	NVMe Device Options Settings
SDIO Configuration	See submenu	SDIO Configuration Parameters
LVDS Configuration	See submenu	LVDS Configuration Parameters
Super I/O Configuration	See submenu	Super I/O Setup Configuration Utility
USB Configuration	See submenu	USB Configuration Parameters
Platform Trust technology	See submenu	Platform Trust Technology Parameters
Embedded Controller	See submenu	Embedded Controller Parameters
Thermal	See submenu	Thermal Configuration Parameters

4.3.1 Intel® I210 Gigabit Network Connection - MAC Address #1 submenu

Menu Item	Options	Description
NIC Configuration	See submenu	Enter the submenu to configure the network device port
Blink LEDs	0 / 1	Identify the physical network port by blinking the associated LED

4.3.1.1 NIC configuration submenu

Menu Item	Options	Description
Link Speed	Auto Negotiated 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	Specifies the port speed used for the selected boot protocol
Wake On LAN	Disabled / Enabled	Enables powering on the system via LAN. Note that configuring Wake on LAN in the operating system does not change the value of this setting, but does override the behaviour of Wake on LAN in OS controlled power states

4.3.2 Trusted computing submenu

Menu Item	Options	Description
Security Device Support	Enabled / Disabled	Enables or Disables BIOS support for security device. OS will not show the Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled all the following items will be available.
SHA-1 PCR Bank	Enabled / Disabled	Enables or Disables SHA-1 PCR Bank
SHA256 PCR Bank	Enabled / Disabled	Enables or Disables SHA256 PCR Bank
Pending Operation	None / TPM Clear	Schedule an Operation for the Security Device. NTE: your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	Enabled / Disabled	Enables or Disabled the Platform Hierarchy
Storage Hierarchy	Enabled / Disabled	Enables or Disabled the Storage Hierarchy
Endorsement Hierarchy	Enabled / Disabled	Enables or Disabled the Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 TCG_2	Select the TCG Spec Version support. TCG_1_2 is the compatible mode for Windows 8 / Windows 10. TCG 2 supports the new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	1.2 / 1.3	Select to tell OS to support PPI Spec Version 1.2 or 1.3. Please note that some HCK tests might not support 1.3
Device Select	Auto TPM 1.2 TPM 2.0	TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

4.3.3 ACPI Settings submenu

Menu Item	Options	Description
Enable ACPI Auto Configuration	Disabled / Enabled	Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled
Enable Hibernation	Disabled / Enabled	Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy resources	Disabled / Enabled	Enables or Disables Lock of Legacy resources

4.3.4 Serial Port Console Redirection submenu

Menu Item	Options	Description
Console redirections	Enabled / Disabled	Enables or Disables the Console redirection. When enabled the following item will appear
Console Redirection Settings	See Submenu	The settings specifies how the host and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings

4.3.4.1 *Console Redirection Settings submenu*

Menu Item	Options	Description
Terminal Type	VT100 VT100+ VT-UTF8 ANSI	Emulation: ANSI: Extended ASCII Char set. VT100: ASCII Char set. VT100+: extends VT100 to support colour, function keys, etc. VT-UTF8: uses UTF8 encoding to map Unicode chars onto 1 or more bytes
Bits per second	9600 / 19200 / 38400 / 57600 / 115200	Select Serial port Transmission Speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Data bits	7 / 8	Set Console Redirection data bits
Parity	None Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the number of 1s in the data bits is even. Odd: parity bit is 0 if the number of 1s in the data bits is odd. Mark: parity bit is always 1. Space: parity bit is always 0. Mark and Space do not allow for error detection

Stop bits	1 / 2	Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit
Flow Control	None Hardware RTS/CTS	Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses RTS# / CTS# lines to send the start / stop signals.
VT-UTF8 Combo Key Support	Enabled / Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Recorder Mode	Enabled / Disabled	When this mode is enabled, only text will be sent. This is to capture Terminal data.
Resolution 100x31	Enabled / Disabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	80x24 / 80x25	On Legacy OS, the number of Columns and Rows supported redirection
Putty Keypad	VT100 / Intel Linux / XTERMR6 / SCO / ESCN /VT400	Select FunctionKey and KeyPad on Putty
Redirection after BIOS POST	Always Enabled BootLoader	When BootLoader is selected, then Legacy Console redirection is disabled before booting to Legacy OS. When 'Always Enabled' is selected, then Legacy Console redirection is enabled for Legacy OS. Default setting for this option is set to 'Always Enabled'

4.3.5 CPU Configuration submenu

Menu Item	Options	Description
Detailed CPU Information		Shows board's specific SoC information
CPU Power Management	See Submenu	CPU Power Management options
Active Processor Cores	Disabled / Enabled	Number of Cores to enable in each processor package
Core 0 Core 1 Core 2 Core 3	Disabled / Enabled	Core #x Enable / Disable. Only available when “Active Processor Cores” is enabled
Intel Virtualization Technology	Disabled / Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
VT-d	Disabled / Enabled	Enables or disables CPU VT-d
Bi-directional PROCHOT	Disabled / Enabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor
Thermal Monitor	Disabled / Enabled	Enables or disables the Thermal Monitor
Monitor Mwait	Disabled / Enabled /	Enables or disables Monitor Mwait

	Auto	
P-STATE Coordination	HW_ALL / SW_ALL / SW_ANY	Change P-STATE Coordination type
DTS	Disabled / Enabled	Enables or disables the Digital Thermal Sensor

4.3.5.1 CPU Power Management submenu

Menu Item	Options	Description
EIST	Disabled / Enabled	Enables or disables Intel® SpeedStep
Turbo mode	Disabled / Enabled	Only Available when "EIST" is enabled. Enables or disables the Turbo Mode
Boot Performance mode	Max performance Max battery	Select the performance state that the BIOS will set before OS handoff.
Power Limit 1 Enable	Disabled / Enabled	Enables or disables Power Limit 1. When Enabled, the following menu items will appear-
Power Limit 1 Clamp Mode	Disabled / Enabled	When Power Limit 1 is Enabled, enables or disables the Clamp Mode
Power Limit 1 Power	Auto / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Windows	Auto / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 10 / 12 / 14 / 16 / 20 / 24 / 28 / 32 / 40 / 48 / 56 / 64 / 80 / 96 / 112 / 128	Power Limit 1 Time Window Value in Seconds. Auto will program the Power Limit 1 Time Window based on silicon default support value

4.3.6 AMI graphic Output Protocol Policy submenu

Menu Item	Options	Description
Output Select	*List of available / connected module's video interfaces*	Sets the support for USB keyboard / mouse / storage under UEFI and DOS environment. When set to UEFI only, then it will support exclusively UEFI environment.

4.3.7 Network Stack configuration submenu

Menu Item	Options	Description
Network Stack	Enabled / Disabled	Enables or disables UEFI Network Stack. When enabled, following menu items will appear
Ipv4 PXE Support	Enabled / Disabled	Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created

Ipv4 HTTP Support	Enabled / Disabled	Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created
Ipv6 PXE Support	Enabled / Disabled	Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created
Ipv6 HTTP Support	Enabled / Disabled	Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created
PXE boot wait time	[0..5]	Wait time to press ESC key to abort the PXE boot
Media detect count	[1..50]	Number of times that the presence of media will be checked

4.3.8 CSM configuration submenu

Menu Item	Options	Description
CSM Support	Enabled / Disabled	Enables or disables the Compatibility Support Module (CSM) Support. When enabled, the following menu items will appear
GateA20 Active	Upon Request Always	Upon Request: GateA20 can be disabled using BIOS services, Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB.
INT19 Trap Response	Immediate Postponed	BIOS Reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot
Boot option filter	UEFI and Legacy Legacy only UEFI only	This option controls Legacy / UEFI ROMs priority
Network Stack	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage Hierarchy	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM
Other PCI devices	Do not launch UEFI Legacy	Determines the OpROM execution policy for devices other than Network, Storage or Video

4.3.9 NVMe configuration submenu

4.3.10 SDIO configuration submenu

Menu Item	Options	Description
SDIO Access Mode	Auto ADMA SDMA PIO	Auto Option: Access the SD Device in DMA mode if the controller supports it, otherwise in PIO Mode. DMA Option: Access the SD Device in DMA mode ADMA Option: Access the SD Device in Advanced DMA mode PIO Option: Access the SD Device in PIO mode
List of SDIO devices found	Auto Floppy Forced FDD Hard Disk	Mass storage device emulation type. 'Auto' enumerates devices less than 530Mb as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD.

4.3.11 LVDS Configuration submenu

Menu Item	Options	Description
LVDS interface	Enabled / Disabled	Enables or Disables the LVDS interface. When enabled all the following parameters will appear
Edid Mode	External / Default / Custom	Select the source (EDID, Extended Display Identification Data) to be used for the internal flat panel. Depending on the setting chosen, only some of the following option or none will appear.
EDID	640x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Only available when Edid Mode is set to "default". Select a software resolution (EDID settings) to be used for the internal flat panel.
Pixel Clock / 10000	[2500..22400]	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. Allowed range from 2500 (25MHz) to 22400 (224MHz)
Horizontal Active	[1..4095]	Horizontal Addressable Video in pixels, a.k.a. Horizontal resolution (e.g. 1024 on a 1024x768 LFP)
Horizontal Blank	[1..4095]	Horizontal Blanking in pixels, equals to Horizontal Total (Horizontal Active + Horizontal Front Porch + Horizontal Black Porch)
Vertical Active	[1..4095]	Vertical Addressable Video in pixels, a.k.a. Vertical resolution (e.g. 768 on a 1024x768 LFP)
Vertical Blank	[1..4095]	Vertical Blanking in pixels, equals to Vertical Total (Vertical Active + Vertical Front Porch + Vertical Black Porch)

Horizontal Offset	[1..1023]	Horizontal Front Porch in pixels
Horizontal Pulse	[1..1023]	Horizontal Sync Pulse Width in pixels
Vertical Offset	[1..63]	Vertical Front Porch in pixels
Vertical Pulse	[1..63]	Vertical Sync Pulse Width in pixels
Horizontal Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Vertical Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Color Mode	VESA 24bpp / JEIDA 24bpp / 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
Interface	Single Channel / Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LVDS Advanced Options	See Submenu	LVDS Advanced Options Configurations

4.3.11.1 LVDS Advanced options submenu

Menu Item	Options	Description
Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)

4.3.12 SuperI/O configuration submenu

Menu Item	Options	Description
Name of the SuperI/O found		This menu item will show the name of all the Super I/Os that are found on the carrier board. By selecting the adequate SuperI/O, it will be possible to set the serial ports and possibly other parameters as shown in the following menu items. If no Super I/O is available on the Carrier Board, this menu will not be available.
Serial Port 1 / Serial Port 2 / Serial Port 3 / Serial Port 4	Enabled / Disabled	Enable or Disable single serial port #1, #2, #3 or #4 (the number of serial ports depends on the Super I/O).
Address	0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each Serial Port, if enabled.
IRQ	3 / 4 / 5 / 6 / 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.

4.3.13 USB configuration submenu

Menu Item	Options	Description
Legacy USB Support	Enabled / Disabled / Auto	Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI hand-off	Enabled/ Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enabled/ Disabled	Enables or disables USB Mass Storage Driver Support
USB Transfer time-out	1 sec / 5 sec / 10 sec / 20 sec	Sets the time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10 sec / 20 sec / 30 sec / 40 sec	USB mass storage device Start Unit command time-out
Device power-up delay	Auto / Manual	Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor).
Device power-up delay in seconds	[1..40]	Delay range in seconds, in one second increment

4.3.14 Platform Trust technology submenu

Menu Item	Options	Description
fTPM	Enabled / Disabled	Enable/Disable fTPM

4.3.15 Embedded Controller submenu

Menu Item	Options	Description
Watchdog	Disabled / Enabled	Enables or disables the Watchdog. When enabled, the following parameters will appear.
Watchdog action	System Reset Power Button 1s Power Button 4s (Shutdown)	Action executed at the firing of the watchdog timeout.
Delay to Start (Sec.)	[0..600]	Seconds of delay before the watchdog timer starts counting.
Timeout (Sec.)	[20..599]	Watchdog Timeout.
Watchdog Event	Disabled / Enabled	High Active output watchdog event indicator
Ext. PWM Frequency (Hz)	[1..65535]	Sets External PWM Frequency in Hertz
Ext. PWM DC (%)	[0..100]	Sets external PWM Duty Cycle (%)
Ext. Tacho Configuration	3-Wire 4-Wire	Sets External Tachometric FAN Type
LID_BTN# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configures the LID_BTN# signal as always open or closed, no matter the pin level, or configures the pin polarity: High = Open (Normal), Low = Open (Inverted)
LID_BTN# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	Configures LID_BTN# wake capability (when not forced to Open or Closed). According to the pin configuration, when the LID is open it can cause a system wake from a sleep state.
SMB_ALERT# wake	Disabled / Enabled	Enables or disables SMBUS Alert Wake from Suspend State.
Int. LAN wake	Disabled / Enabled	Enable wake for internal LAN
External PCIE wake	Disabled / Enabled	Enable wake from Q7 edge connector's PCIE_WAKE# pin
User Non Volatile Storage Content		Open a page showing the user Non Volatile Storage Area Contents

4.3.16 Thermal submenu

Menu Item	Options	Description
Automatic Thermal Reporting	Enabled / Disabled	Configures Critical Trip Point, Passive trip Point and Active Trip Point automatically basing on the values recommended in BWG's Thermal reporting for Thermal Management Settings. Set to Disabled for Manual Configuration.
Critical Trip Point	15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 100°C / 103°C / 110°C / 119°C / 125°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off.
Passive Trip Point	Disable / 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor.
Active Trip Point	15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 60°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 110°C	This value controls the temperature of the ACPI Active Trip Point - the point in which the OS will turn the FAN on.

4.4 Chipset menu

Menu Item	Options	Description
South Bridge		South Bridge Parameters
Uncore Configuration		Uncore Configuration Parameters
South Cluster Configuration		South Cluster Configuration Parameters

4.4.1 South Bridge submenu

Menu Item	Options	Description
Serial IRQ Mode	Quiet Mode Continuous Mode	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.
OS Selection	Windows / Android / Win7 / Intel Linux	Select the Target OS
Real Time Option	RT Disabled RT Enabled, Agent IDI1 RT Enabled, Agent Disabled	Select Real-Time Enable and IDI Agent Real-Time Traffic Mask Bits

4.4.2 Uncore Configuration submenu

Menu Item	Options	Description
GOP Brightness Level	20/40/60/80/100/120/140/160/180/200/220/240/255	Set Graphics Output Protocol (GOP) Brightness Level; value ranges from 0 to 255
DDI0 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #0 Pull-up values
DDI1 DDC Pull Type	Pull Up 1K Pull Up 2K Pull Up 5K	Sets DDI #1 Pull-up values
DDI0 Configuration Override	Disabled	Allows to override default DDI0 configuration

	DP++ (Multimode DP) HDMI / DVI	
DDI1 Configuration	Disabled DP++ (Multimode DP) HDMI / DVI	Allows to override default DDI1 configuration
Integrated Graphics Device	Enabled / Disabled	Enable the Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor, or always disable it.
Primary Display	IGD / PCIe / HG	Select which of IGD / PCIe /HG graphics device should be the Primary Display
HG Delay After Power Enable	[0..1000]	Delay in milliseconds after power enable
HG Delay After Hold Reset	[0..1000]	Delay in milliseconds after hold reset
RC6 (Render Standby)	Enabled / Disabled	Permits to enable the render standby features, which allows the on-board graphics entering in standby mode to decrease power consumption
GTT Size	2 MB / 4 MB / 8 MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	256 MB	Use this item to set the total size of Memory that must be left to the GFX Engine
DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
Cd Clock Frequency	144 MHz / 288 MHz / 384 MHz / 576 MHz / 624 MHz	Select the highest CD Clock frequency supported by the platform
GT PM Support	Enabled / Disabled	Enable / Disable GT Power Management Support
PAVP	Enabled / Disabled	Enable / Disable Protected Audio Video Playback (PAVP)
Memory Scrambler	Enabled / Disabled	Enable / Disable the Memory Scrambler Support

4.4.3 South Cluster Configuration submenu

Menu Item	Options	Description
HD Audio Configuration	See submenu	HD Audio Configuration Settings
LPSS Configuration	See submenu	Low Power Sub System Configuration Settings

PCI Express Configuration	See submenu	PCI Express Configuration Settings
SATA Drives	See submenu	SATA Devices Configuration Setup options
SCC Configuration	See submenu	Storage Control Cluster Configuration Settings
USB Configuration	See submenu	USB configuration Settings
Miscellaneous Configuration	See submenu	Miscellaneous Settings

4.4.3.1 HD Audio Configuration submenu

Menu Item	Options	Description
HD Audio Support	Enabled / Disabled	Enable / Disable HD Audio Support
HD Audio DSP	Enabled / Disabled	Enable / Disable HD Audio DSP

4.4.3.2 LPSS Configuration submenu

Menu Item	Options	Description
I2C #1 (D22:F0)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS I2C #1 Support
Set LPSS I2C #0 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #1 is not disabled. Select LPSS I2C #0 Speed
I2C #3 (D22:F2)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS I2C #3 Support
Set LPSS I2C #2 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #3 is not disabled. Select LPSS I2C #2 Speed
I2C #5 (D23:F0)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS I2C #5 Support
Set LPSS I2C #4 Speed	Standard Mode Fast Mode Fast Plus Mode	Only available when LPSS I2C #5 is not disabled. Select LPSS I2C #4 Speed

HSUART #0 (D24:F0)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS HSUART #0 Support
HSUART #2 (D24:F2)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS HSUART #2 Support
LPSS SPI #1 Support (D25:F0)	Disable PCI Mode ACPI Mode	Enable/Disable LPSS SPI #1 Support

4.4.3.3 PCI Express Configuration submenu

Menu Item	Options	Description
Compliance Mode	Enabled / Disabled	Compliance Mode Enable/Disable
PCIE Root Port 1 - Internal LAN 0 PCIE Root Port 2 - Internal LAN 1 PCIE Root Port 3 - SMARC PCIE0 PCIE Root Port 4 - SMARC PCIE1 PCIE Root Port 5 - SMARC PCIE2 PCIE Root Port 6 - SMARC PCIE3		Sets the parameters for each single PCI-e Root Port

4.4.3.3.1 *PCIE Root Port #x submenus*

Menu Item	Options	Description
PCIE Root Port 1 - Internal LAN 0 PCIE Root Port 2 - Internal LAN 1 PCIE Root Port 3 - SMARC PCIE0 PCIE Root Port 4 - SMARC PCIE1 PCIE Root Port 5 - SMARC PCIE2 PCIE Root Port 6 - SMARC PCIE3	Auto Enabled Disabled	Controls the PCI Express Root Port. Auto: disable unused root port automatically for the most optimised power saving. Enable: Always enable the PCIe root port. Disable: Always disable the PCIe root port *(all the following items will disappear)*
ASPM	Disable / L0s	PCI Express Active State Power Management Settings
PCIe Speed	Auto Gen1 Gen2	Configure PCIe Speed

4.4.3.4 SATA Drives Configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Enables or Disables the Chipset SATA controller, which supports the 2 black internal SATA ports (up to 3GB/s supported per port).
SATA Test Mode	Enabled / Disabled	Enable / Disable SATA Test Modes
SATA Speed	Gen1 Gen2 Gen3	Select SATA Speed
Port 0 Port 1	Enabled / Disabled	Enable / Disable SATA Port #x

4.4.3.5 SCC Configuration submenu

Menu Item	Options	Description
SCC SD Card Support	Enabled / Disabled	Enable or Disable SCC SD Card Support
SCC eMMC Support	Enabled / Disabled	Enable or Disable SCC eMMC Card Support

4.4.3.6 USB Configuration submenu

Menu Item	Options	Description
xHCI Pre-Boot Driver	Enable / Disable	Enables or Disable the support for XHCI Pre-boot driver
xHCI Mode	Enable / Disable	Once Disabled, the xHCI Controller would be function disabled, none of the USB devices will be detectable and usable during the boot and in the OS. Do not disable it unless for debug purposes
USB VBUS	Off / ON	VBUS should be ON in HOST mode. It should be OFF in OTG device mode
USB Port Disable Override	Enable / Disable	Allows enabling or disabling selectively each single USB port from reporting a device connection to the controller.
USB Port #0 USB Port #1 USB Port #2 USB Port #3 USB Port #4 USB Port #5 USB 3 Port #0	Enable / Disable	Only available when "USB Port Disable Override" is Enabled. Allows enabling or disabling the single USB Port #x. Once disabled, any USB device connected to the corresponding port will not be detected by the BIOS neither by the OS

USB 3 Port #1 USB 3 Port #5		
XDCI Support	Disable PCI Mode	Enables or Disables the XDCI (USB Device)
XDCI Disable Compliance Mode	FALSE / TRUE	Options to disable XHCI Link Compliance Mode. Default is FALSE to not disable Compliance Mode. Set TRUE to disable Compliance Mode

4.4.3.7 Miscellaneous Configuration submenu

Menu Item	Options	Description
State After G3	Always ON Always OFF Last State	Specify what state to go to when power is re-applied after a power failure (G3 state). In S0 State, the System will boot directly as soon as power is applied. IN S5 State, the System keeps in power-off state until power button is pressed
Wake On Lan	Enabled / Disabled	Enable or disable the Wake On LAN Feature
BIOS Lock	Enabled / Disabled	Enables or disables the SC BIOS Lock enable feature. It is required that it is enabled to ensure SMM protection of flash
Flash Protection Range Registers	Enabled / Disabled	Enable Flash Protection Range registers
Reset Power Cycle Duration	1-2 seconds 2-3 seconds 3-4 seconds 4-5 seconds	The value in this register determines the minimum time a platform will stay in reset during a host partition reset with power cycle or a global reset

4.5 Security menu

Menu Item	Options	Description
Setup Administrator Password		Set Setup Administrator Password
User Password		Set User Password
Secure Boot	See Submenu	Customizable Secure Boot Settings

4.5.1 Secure Boot submenu

Menu Item	Options	
Attempt Secure Boot	Enabled / Disabled	Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled.
Secure Boot Mode	Standard / Customized	Set UEFI Secure Boot Mode to STANDARD Mode or CUSTOM mode. This change will be effective after save. And after reset, the mode will return to Standard
Key management	See submenu	Enable expert users to modify Secure Boot Policy variables without full authentication

4.5.1.1 Key Management submenu

Menu Item	Options	
Provision Factory Default keys	Enabled / Disabled	Provision factory default keys on next re-boot only when System in Setup Mode
Install Factory Default Keys		Force System to User Mode. Configure NVRAM to contain OEM- defined factory default Secure Boot keys
Enroll Efi Image	*File System Image*	Allow the selected image to run in Secure Boot mode. Enrol SHA256 Hash Certificates of the Image into Authorized Signature Database (db)
Restore DB defaults		Restore DB variable to factory defaults
Platform key Key Exchange Keys Authorized Signatures Forbidden Signatures Authorized Timestamps OS Recovery Signatures	Set New Var Append Key	Enrol factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER encoded) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHA256,384,512 2. Authenticated UEFI variables 3. EFI PE/COFF Image (SHA256), Key Source: Factory, External, Mixed

4.6 Boot menu

Menu Item	Options	Description
Setup Prompt Timeout	0 .. 65535	Number of seconds to wait for setup activation key. 655535 means indefinite waiting.
Bootup NumLock State	On / Off	Select the Keyboard NumLock State at boot
Quiet Boot	Enabled / Disabled	Enables or Disables Quiet Boot options
New Boot Option Policy	Default Place First Place Last	Controls the placement of newly detected UEFI boot options
Boot Mode Select	LEGACY UEFI	Select the boot mode between Legacy and UEFI
Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8	Hard Disk0 Hard Disk1 eMMC CD/DVD SD USB Device Network Other Device Disabled	Select the system boot order
UEFI EMMC Drive BBS Priorities	*List of UEFI bootable drives*	Specifies the Boot Device priority sequence from available UEFI EMMC Drives
UEFI Other Drive BBS Priorities	*List of other UEFI drives*	Specifies the Boot Device priority sequence from available UEFI Other Drives

4.7 Save & Exit menu

Menu Item	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset the system without saving any changes.
Save Changes		Save the changes done so far to any of the setup options.
Discard Changes		Discard the changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options
List of EFI boot options		
Launch EFI Shell from filesystem device		Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices

Chapter 5.
Appendices

- Thermal Design

5.1 Thermal Design

Highly integrated modules like SM-B69 offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SM-B69 indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SM B69 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
RB69-DISS-1-PK	SMARC HEAT SPREADER: SM-B69 Heat Spreader (PASSIVE) - Packaged
RB69-DISS-2-PK	SMARC HEAT SINK: SM-B69 Heat Sink (PASSIVE) - Packaged

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

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