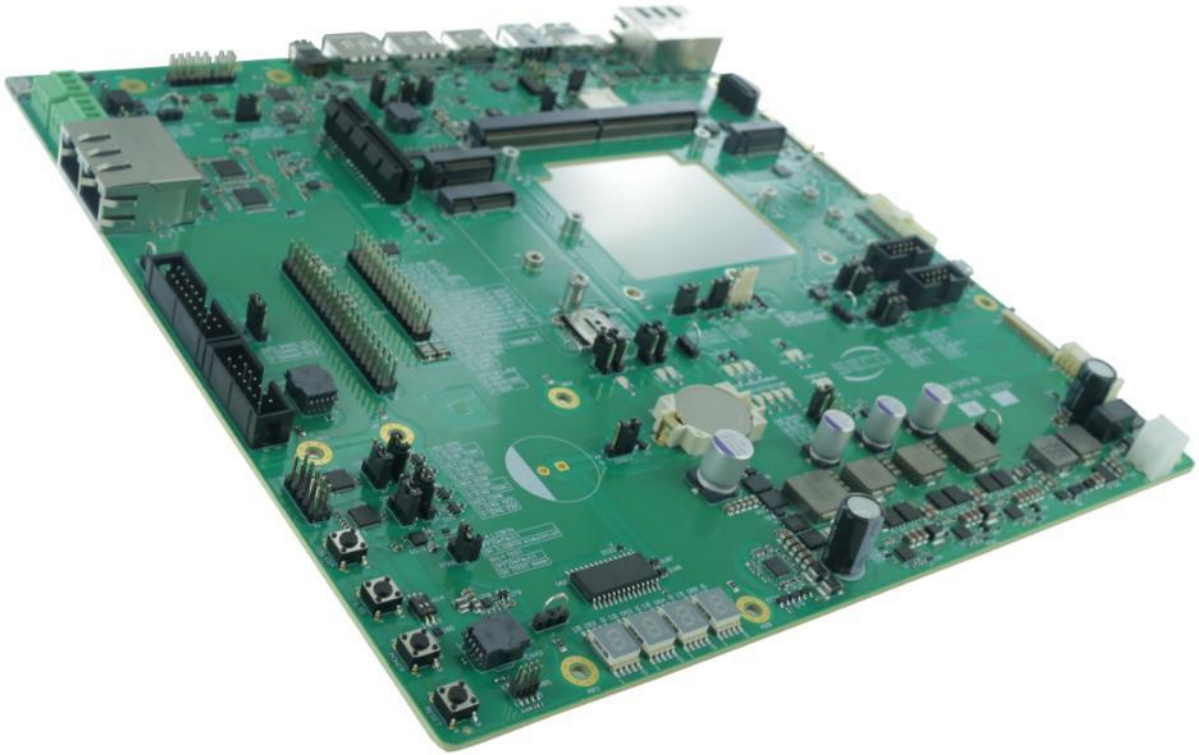
Smarc

User Manual



CSM-B79

Carrier Board for SMARC® Rel. 2.0 / 2.1 compliant modules

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	30th August 2021	First official release	AR
1.1	22nd September 2021	Updated SMARC MXM Connector on pins S78-S79-S81-S82	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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INTRODUCTION

- Warranty
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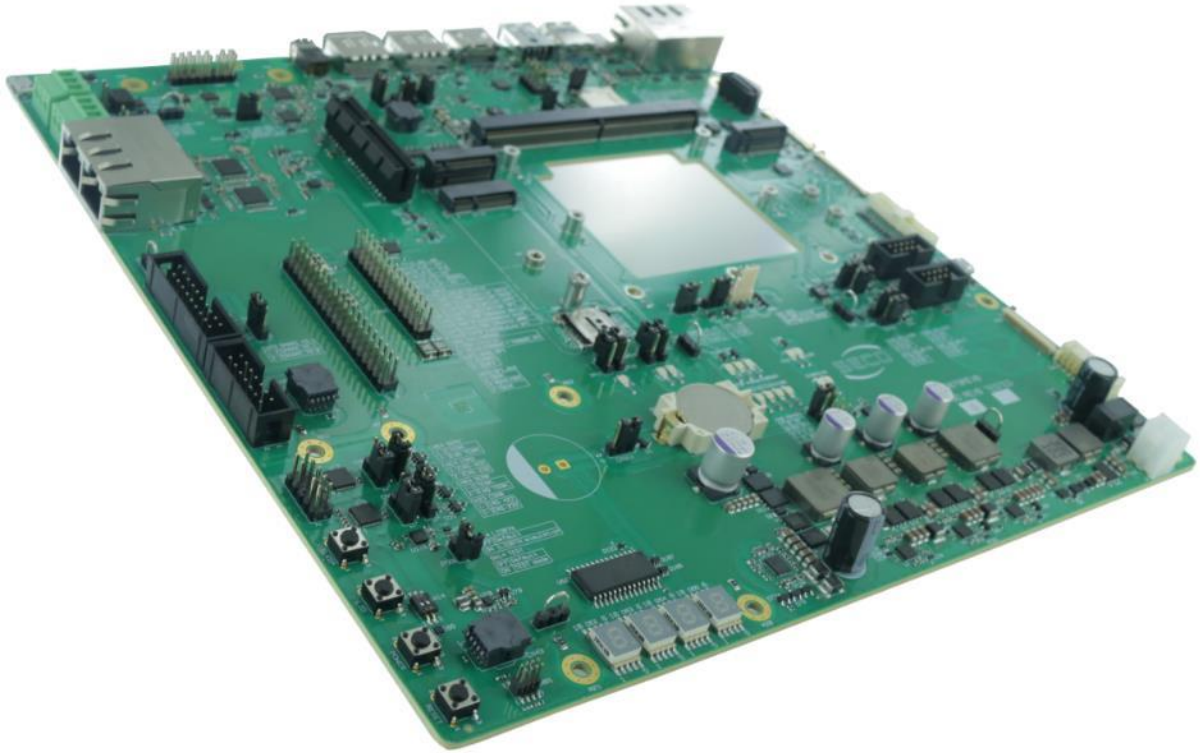


1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210

- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The CSM-B79 board uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!**
>
> Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.
>
> Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The CSM-B79 board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!**
>
> Whenever handling a CSM-B79 board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The CSM-B79 board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the CSM-B79 Carrier Board shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the board never exceeds 100 W, even in worst-case fault);
- used inside an enclosure provided with the symbol IEC 60417-5041(element 1a according to clause 9.5.2 of the IEC 62368-1) on the external part;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes a CSM-B79 Carrier Board in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- prescribe temperature and humidity range for operating, transport and storage conditions;
- prescribe to perform maintenance on the board only when it is off and has already cooled down;
- prescribe that the connections from or to the board have to be compliant to ES1 requirements;
- the board in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
AVC	Advanced Video Coding, a video compression standard, also known as H.264
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
DP	Display Port, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HEVC	High Efficiency Video Coding, a video compression standard, also known as H.265
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
JPEG/MJPEG	Joint Photographic Experts Group, standard method for lossy compression of digital images. Motion JPEG is a video compression format
LAN	Local Area Network
LPDDR4	Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of

	the MMC. They are devices that incorporate the flash memories on a single BGA chip.
MPEG2	Standard for the generic coding of moving pictures and associated audio information
MVC	Multiview Video Coding, a stereoscopic video coding standard for video compression
N.A.	Not Applicable
N.C.	Not Connected
OpenCL	Open Computing Language, specifies programming languages for programming different devices and API
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OS	Operating System
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems
PWM	Pulse Width Modulation
PWR	Power
RGMII (PHY)	Reduced Gigabit Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer
SATA	Serial Advance Technology Attachment, a differential full duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SGET	Standardization Group for Embedded Technologies
SMARC	Smart Mobility Architecture, a computer Module standard maintained by the SGET
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SOC	System-on-a-chip
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
UART	Universal Asynchronous Receiver-Transmitter, is an asynchronous serial interface where data format and transmission speed are configurable
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface

USB	Universal Serial Bus
VP8	Open video compression format, a traditional block-based transform coding format
VP9	Successor to VP8, customized for video greater than 1080p
WMV9	Series 9 of Windows Media Video, a video compression format inlcuding native support for interlaced video, non-square pixels, and frame interpolation

1.9 Reference specifications

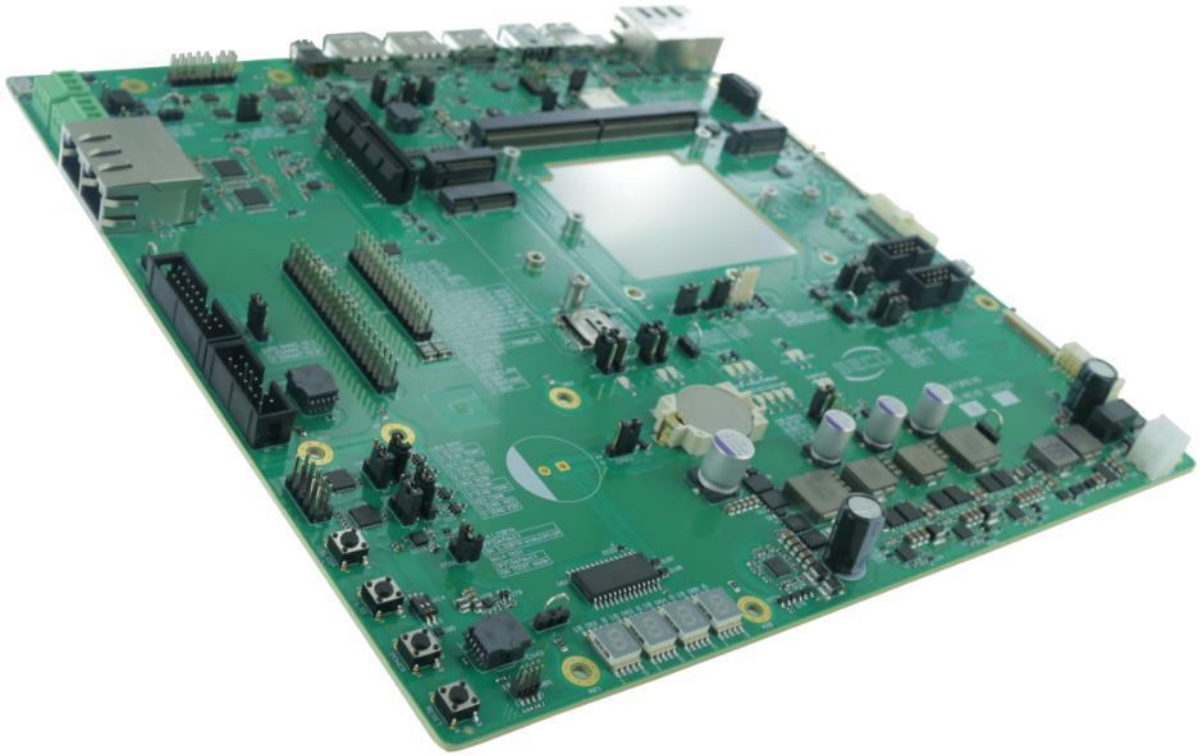
Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	https://uefi.org/specifications
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
FastEthernet	http://standards.ieee.org/about/get/802/802.3.html
Gigabit Ethernet	https://standards.ieee.org/standard/802_3-2018.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MIPI	http://www.mipi.org
MMC/eMMC	http://www.jedec.org/committees/jc-649
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SMARC Design Guide 2.1	SMARC Design Guide 2.1.1 (sget.org)
SMARC Hardware Specification 2.1.1	https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds

UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	https://usb.org.10-1-108-210.causewaynow.com/sites/default/files/usb_32_20191024.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

The CSM-B79 is a carrier board for SMARC® Rel. 2.0 / 2.1 compliant modules, designed in microATX form factor.

SMARC ("Smart Mobility Architecture") is a computer Module standard maintained by the SGET consortium.

SMARC® Modules are small form factor (82mm x 50mm), low power computer Modules that integrates all core components of a common PC architecture (CPU, RAM, Graphic, audio, etc.). All the functionalities are made available through a standardized card edge connector, from which all signals can be taken and carried to the appropriate external connector in the carrier board and/or to other internal component, to implement more functionalities other than included in the standard SMARC® bus interface.

SMARC® Modules are used on a Carrier board that utilizes a 314 pin 0.5mm pitch right-angle memory socket style connector to host the Module.

SMARC® Modules may utilize ARM, low power RISC or low power x86 CPUs / SOCs.

The list of features that are effectively available depends on the configuration of the SMARC® module used.

CSM-B79 carrier board is specially designed for being both an advanced development board, for skilled users who want to design their own carrier boards, and a good solution for mass production, for customers whose needing are satisfied by this compact and versatile Carrier Board.

All the components mounted onboard are certified for industrial temperature range.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

2.2 Technical Specifications

Supported Modules

SMARC® Rel. 2.0 / 2.1 compliant modules

Video interfaces

- LVDS/MIPI-DSI connector, interface shared with 2x eDP connectors
- Backlight control + LCD selectable voltages dedicated connector
- 2x DP++ connectors
- HDMI connector (can be used in alternative to 1x DP++)
- 2x CSI Camera input interfaces

Mass Storage interfaces

- 1x SATA 7p M connector with dedicated power connector, interface shared with M.2 Socket 2 2230 / 2242 / 2260 Key B SSD slot
- µSD Card slot

Networking

- 2x Dual RJ-45 Gigabit Ethernet connector
- M.2 Socket1 2230 Key E Slot for WiFi/BT Modules (interface shared with PCI-e x4 slot)
- M.2 Socket 2 2260 / 3042 Key B Slot for WWAN Modem Modules (interface shared with PCI-e x 4 slot), connected to on-board microSIM slot

USB

- 1 x USB 3.0 type A Socket
- 1 x USB 2.0 type A Socket
- 1 x USB OTG micro-AB Socket
- 1 x USB 3.1 Type-C Socket

PCI-e

- PCI-e x4 slot, interface shared with M.2 Slots

Audio

- TRSS Audio Jack
- Onboard I2S Audio Codec (TI TLV320AIC3204) + HD Audio Codec (Cirrus Logic CS4207)
- I2S Audio header

Serial Ports

- 2 x CAN ports
- 2 x RS-232/RS-422/RS-485 configurable serial ports on internal pin header
- 2 x Serial ports (Tx/Rx signals only, TTL level) on feature header

Other Interfaces

- eSPI pin header + Flash Socket
- SPI pin header + Flash Socket
- I2C EEPROM Socket
- 4 x 7-segment LCD displays for POST codes
- Feature pin header with 2 x Serial ports, I2C, SM Bus, Watchdog and Power Management Signals
- GPIO / FuSa header
- FAN connector
- Optional Debug USB port on micro-B connector
- Boot selection switches
- JTAG connector
- Selector for SMARC® 2.0 / 2.1 pinout compatibility

Power supply:

9 ÷ 24V_{DC} through dedicated Mini-Fit Jr 2x2 power connector

6 ÷ 17V_{DC} through 2/3/4 Cell Smart Battery Connector

RTC Coin cell battery holder

Operating temperature: -40°C ÷ +85°C *

Dimensions: 243.84 x 243.84mm (microATX)

! ** Temperature ranges indicated mean that all components available onboard are certified for working with a Tcase included in these temperature ranges. This means that it is customer's responsibility to ensure that all components' Tcases remain in the range above indicated. Please also check paragraph 4.1.*

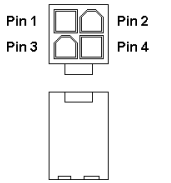
2.3 Electrical Specifications

CSM-B79 board needs to be supplied with a single voltage in the range $9V_{DC}$ .. + $24V_{DC}$. All the others voltages necessary for the working of the board and of the connected peripherals are derived from the main V_{IN} power rail.

Power IN Connector – CN3			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	VIN	4	VIN

The power connector is type Molex Mini-Fit Jr connector, type MOLEX p/n 39-28-1043 or equivalent.

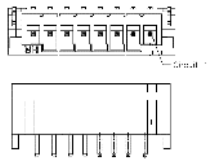
The pin-out is indicated in the table here on the left, and the mating connector is MOLEX p/n 39-01-2040 or equivalent with crimp terminals series 5556/44476.



2.3.1 Smart Battery Connector

It is possible to supply the board also by using external SMART batteries. Input voltage range, in this case, must be in the range $6..17V_{DC}$.

SMART Battery Connector – CN6	
Pin	**Signal**
1	VBAT
2	VBAT
3	N.C.
4	SMB_CLK_BAT
5	SMB_DAT_BAT
6	SAFETY
7	GND
8	GND



To do this, a 8-pin male connector is provided, type HR p/n A2001WR-S-08PD01 or equivalent, with pinout shown in the table on the left.

Mating connector: JST PHR-8 crimp housing with JST SPH-002T-P0.5L crimp terminals.

SMB_CLK_BAT: Smart Battery System Management bus bidirectional clock line, +3.3V_DSW electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_CK signal

SMB_DAT_BAT: Smart Battery System Management bus bidirectional data line, +3.3V_DSW electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_DAT signal

SAFETY: Smart Battery System Management safety input signal, used to communicate critical errors and/or safety mechanisms to prevent over-charging, over-discharging, over-temperature and other conditions that are dangerous or could adversely affect battery longevity. This signal goes directly from the battery to the on-board charger.

2.3.2 RTC Battery

For the occurrences when the System (Carrier board + SMARC® module) is not powered with an external power supply, on board there is a RTC Coin Cell Battery holder CN2, for the use of standard coin battery type CR2032 with a nominal capacity of 220mAh, to supply, with a 3V voltage, the Real Time Clock and CMOS memory mounted on the SMARC® module.

The batteries should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Never allow the batteries to become short-circuited during handling.

Batteries supplied with CSM-B79 board are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order CSM-B79 board, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

CN93 position	RTC Battery enable
1-2	Battery connected
2-3	Battery disconnected
NO jumper	Current measurement

It is possible to monitor the consumption on VDD_RTC battery by removing the jumper from CN93 connector and inserting a tester in series set as ammeter between 1-2 position.

RTC battery can be enabled/disabled using dedicated jumper on CN93, which is a 

standard pin header, P2.54mm, 1x3 pin.

2.3.3 SMARC Module's Power In Voltage selector

CN8 position	VDD_IN SMARC Voltage
1-2	3.0V
3-4	3.3V
5-6	4.25V
7-8	5V

According to SMARC® 2.1.1 specifications, SMARC® modules allow a power input voltage range of 3.0V to 5.25V for VDD_IN.

Since the modules could be designed to work only with a fixed voltage value in this range, on CSM-B79 carrier board is possible to select module's power in voltage value by placing a jumper on CN8 header, type ADIMPEX p/n LE008208-R.

2.3.4 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: SMARC® module power input voltage. Derived directly from VIN coming from Power IN Connector CN3. VDD_IN value can be set by SMARC Module's Power In Voltage selector CN8 (par.2.3.3)

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the RTC Coin Cell Battery holder CN2 for supplying the RTC clock on SMARC® module.

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI s S0 (Working) state. Examples:+3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI s S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

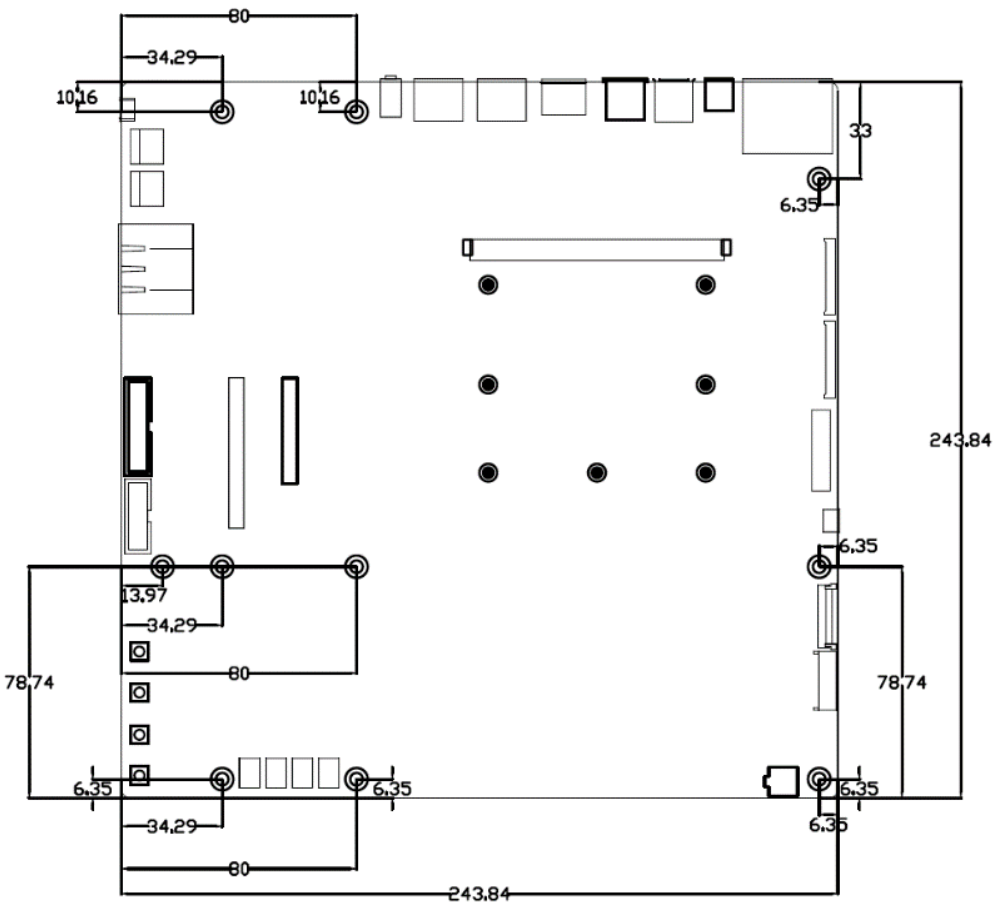
_DSW: Deep Sleep Well voltages, i.e. power rails that are derived directly from VIN coming from Power IN Connector CN3. Examples: +3.3V_DSW, +1.8V_DSW.

2.4 Mechanical Specifications

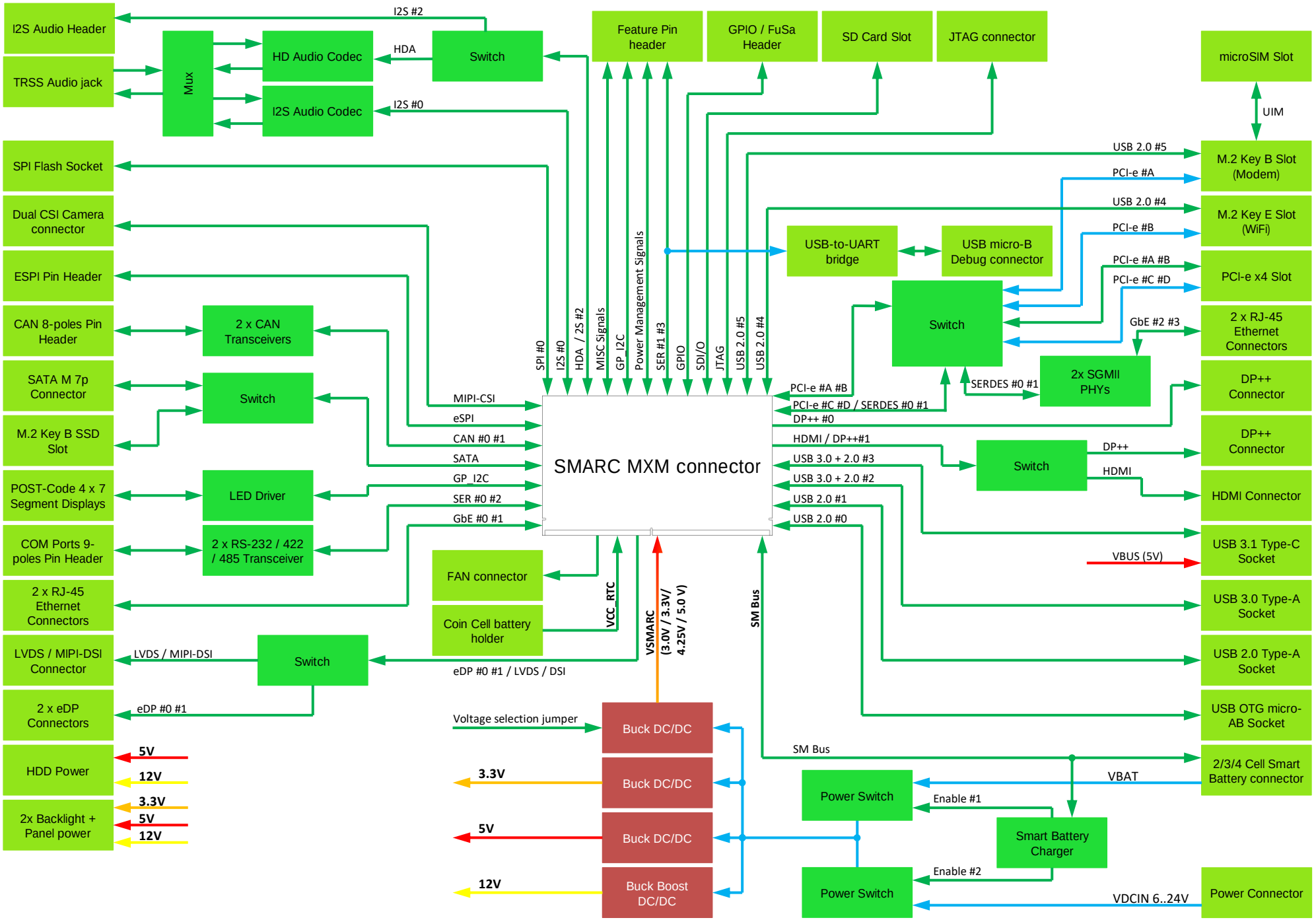
According to microATX form factor, board dimensions are 243.84 x 243.84 mm.

The printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

In order to fix the SMARC® module to the carrier board, on CSM-B79 have been soldered seven metallic spacers, height 8mm, 2.5mm diameter module.

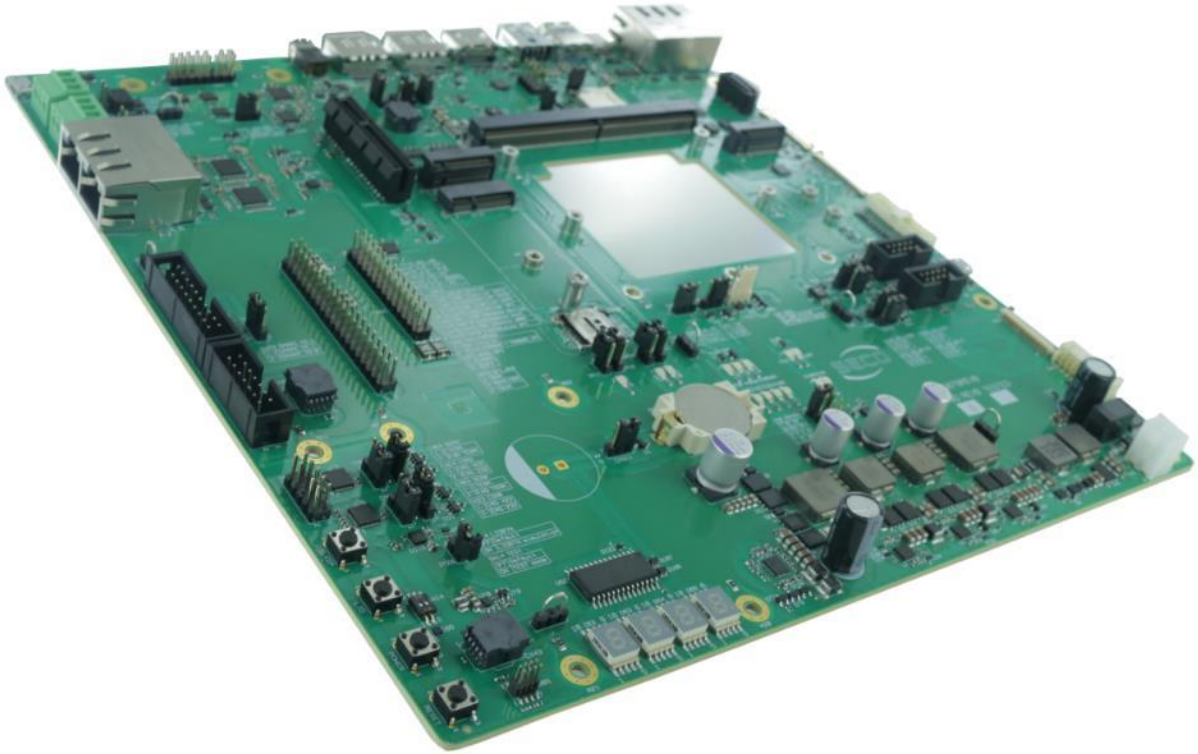


2.5 Block Diagram



Chapter 3.
CONNECTORS

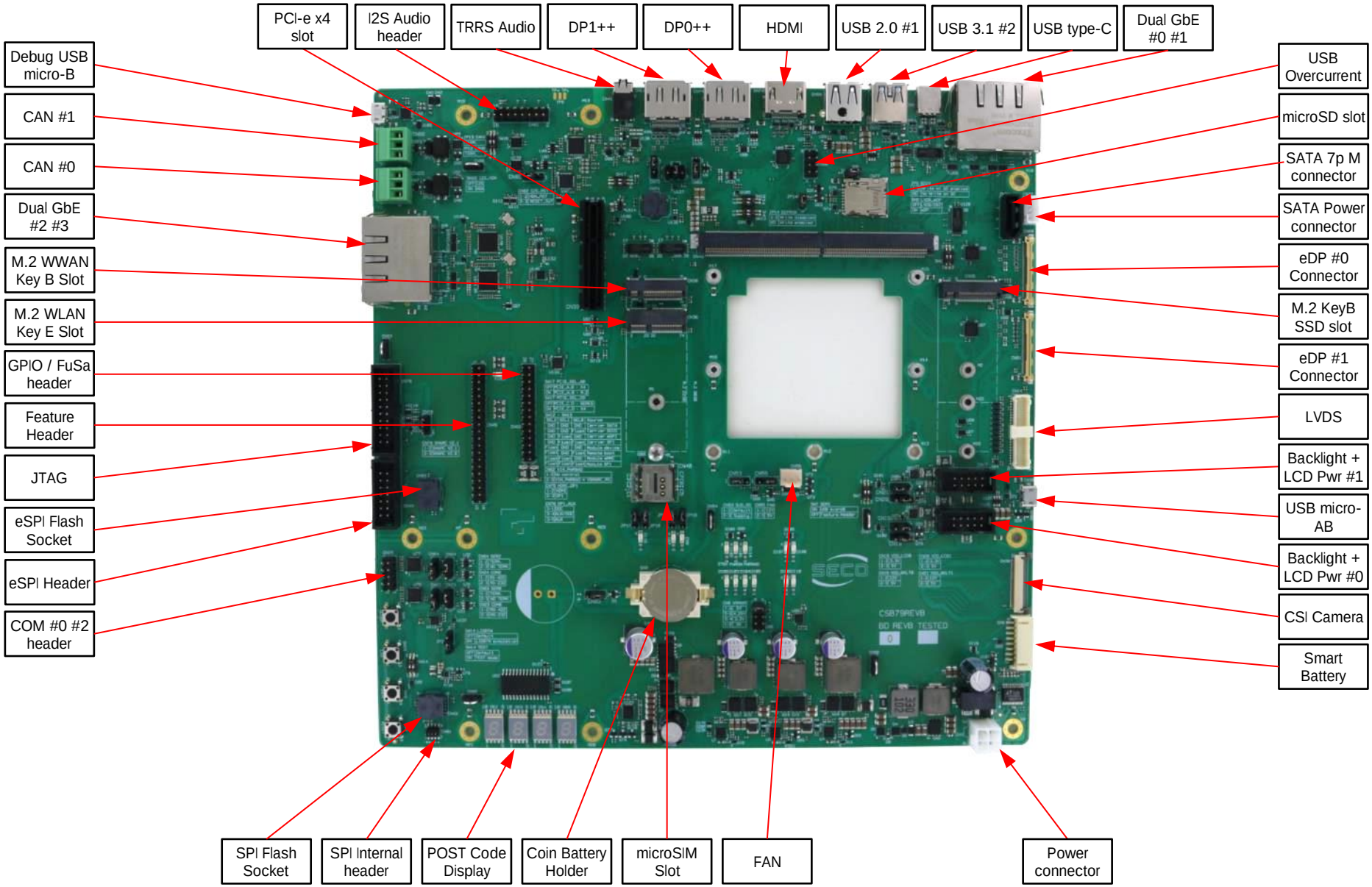
- Connectors placement
- Connectors overview
- Connectors description



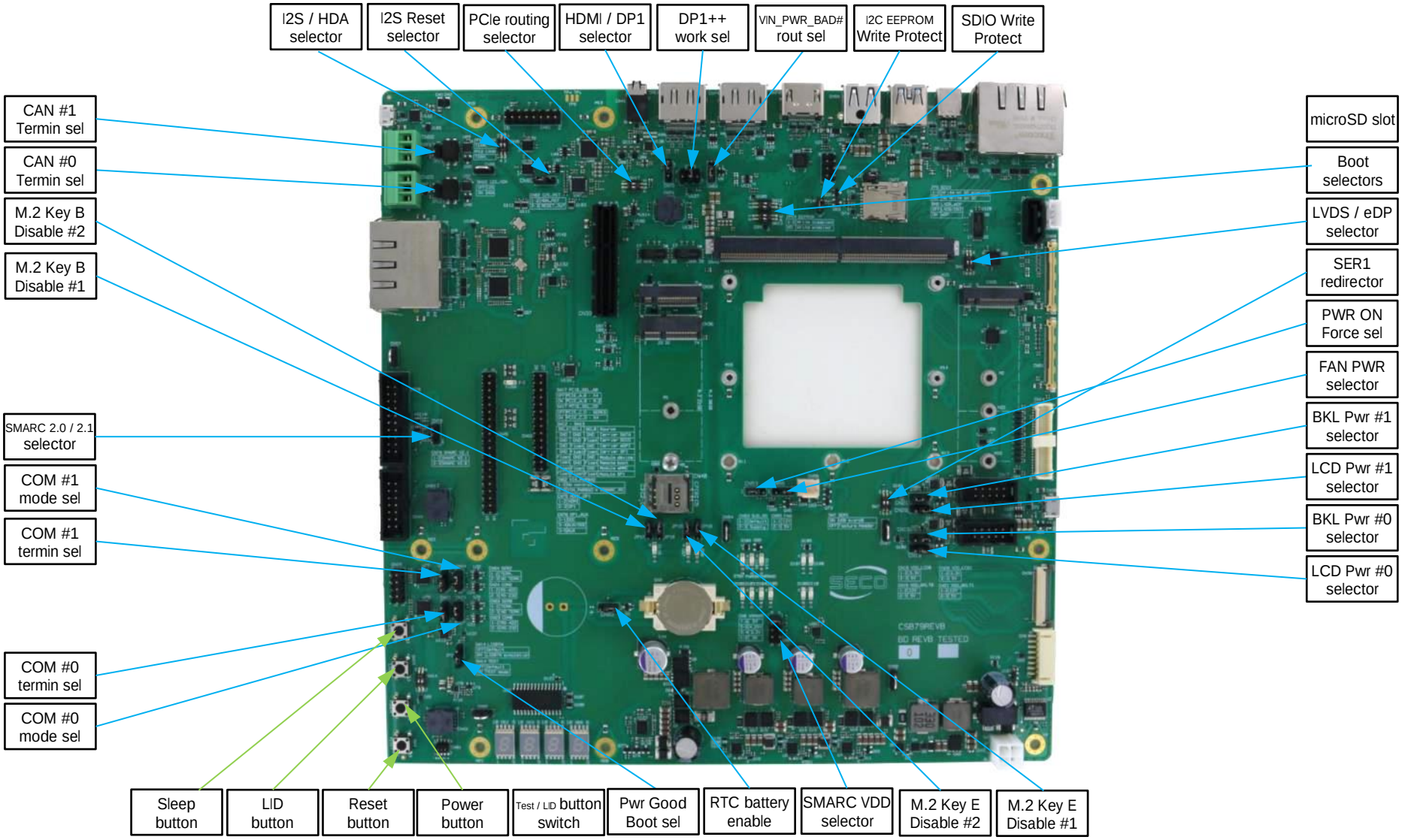
3.1 Connectors placement

On CSM-B79 carrier board, there are several connectors. Some of them are standard connectors, like Gigabit Ethernet, USB ports, and are placed on the same side of the board, so that they can be placed on a panel of a possible enclosure.

In the following picture it is possible to see the position of each connector.



JUMPER POSITION



3.2 Connectors overview

3.2.1 Connectors list

Name	Description	Name	Description
CN2	RTC Coin Cell Battery holder	CN49	SMARC MXM Connector
CN3	Power Connector	CN50	USB 2.0 #1 Type-A Slot
CN6	Smart Battery Connector	CN56	FAN Connector
CN9	USB 3.1 Type-C Socket	CN60	eDP #0 Connector
CN11	DP1++ Connector	CN61	eDP #1 Connector
CN14	LVDS / MIPI-DSI Connector	CN65	CAN #0 PCB Terminal Block
CN16	LCD Panel #0 Voltage connector	CN66	CAN #1 PCB terminal Block
CN17	LCD Panel #1 Voltage connector	CN69	eSPI Flash Socket
CN25	COM #0 #2 internal Header	CN70	JTAG Connector
CN27	Dual Gigabit Ethernet Connector (GbE #0 #1)	CN71	I2C EEPROM Socket
CN28	Dual Gigabit Ethernet Connector (GbE #2 #3)	CN72	USB 3.1 #2 type- A socket
CN30	Micro-AB USB Connector	CN73	Debug USB micro-B
CN33	PCI-e x4 slot	CN74	DP0++ Connector
CN34	SATA 7p M Connector	CN77	microSD Slot
CN35	M.2 Key B SSD Slot	CN79	HDMI Connector
CN36	M.2 WLAN Key E Slot	CN80	USB Overcurrent Header
CN37	S-ATA Power Connector	CN81	I2S Audio Header
CN38	M.2 WWAN Key B Slot	CN91	SPI Internal Header
CN39	CSI Camera Connector	CN92	GPIO / FuSa Header
CN40	microSIM Slot		
CN41	TRRS Audio jack		
CN43	SPI Flash Socket		
CN44	eSPI Header		
CN45	Feature Header		

3.2.2 Jumpers and switch list

Name	Description	Name	Description
CN8	SMARC VDD_IN Voltage selector	JP5	SDIO Write Protect
CN18	LCD #0 Power Selector	JP12	CAN #0 termination selector
CN19	BKLT #0 power selector	JP13	CAN #1 termination selector
CN20	LCD #1 Power Selector	JP14	I2C EEPROM Socket Write Protect
CN21	BKLT #1 power selector	JP15	M.2 Key E Wireless Disable #2
CN23	COM #0 mode selector	JP16	M.2 Key E Wireless Disable #1
CN24	COM #2 mode selector	JP17	M.2 Key B Wireless Disable #1
CN53	Power ON Force selector	JP18	M.2 Key B Wireless Disable #2
CN55	FAN Power Selector	JP20	Power Good controlled boot selector
CN62	VIN_PWR_BAD# routing selector	SW3	Power Button
CN63	COM #0 Termination selector	SW4	Reset Button
CN64	COM #2 Termination selector	SW5	Sleep Button
CN75	HDMI / DP1++ selector	SW6	LVDS / eDP selector
CN76	DP1++ Working mode selector	SW7	SER #1 routing selector
CN78	SMARC 2.0 / 2.1 selector	SW12 / SW13	BOOT Selectors
CN82	I2S Reset selector	SW14	Test and Lid Button debug switch
CN93	RTC Battery enable	SW15	LID Button
		SW16	I2S / HDA Codec selector
		SW17	PCIe routing selector

3.3 Connectors description

3.3.1 SMARC Connector

According to SMARC Rel. 2.1.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in SMARC® standard are implemented on MXM3 connector, due to the functionalities really implemented on CSM-B79.

Therefore, please refer to the following table for a list of effective signals reported on MXM3 connector. Please be aware that on signals' description, Input and Output (if specifically written) are referred to the SMARC® module, i.e. they are inputs and outputs of the module itself, not of the carrier board (where they are, respectively, outputs and inputs).

SMARC MXM Connector – CN49							
TOP SIDE				BOTTOM SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
				S1	I2C_CAM1_CK	I/O	CSI1 CAMERA INTERFACE
MANAGEMENT	I	SMB_ALERT#	P1	S2	I2C_CAM1_DAT	I/O	CSI1 CAMERA INTERFACE
		GND	P2	S3	GND		
CSI1 CAMERA INTERFACE	I	CSI1_CK+	P3	S4	RSVD#S4	I/O	Reserved Purpose Signal
CSI1 CAMERA INTERFACE	I	CSI1_CK-	P4	S5	I2C_CAM0_CK	I/O	CSI0 CAMERA INTERFACE
GBE	I/O	GBE1_SDP	P5	S6	CAM_MCK	O	CSI0/1 CAMERA INTERFACE
GBE	I/O	GBE0_SDP	P6	S7	I2C_CAM0_DAT	I/O	CSI0 CAMERA INTERFACE
CSI1 CAMERA INTERFACE	I	CSI1_RX0+	P7	S8	CSI0_CK+	I	CSI0 CAMERA INTERFACE
CSI1 CAMERA INTERFACE	I	CSI1_RX0-	P8	S9	CSI0_CK-	I	CSI0 CAMERA INTERFACE
		GND	P9	S10	GND		
CSI1 CAMERA INTERFACE	I	CSI1_RX1+	P10	S11	CSI0_RX0+	I	CSI0 CAMERA INTERFACE
CSI1 CAMERA INTERFACE	I	CSI1_RX1-	P11	S12	CSI0_RX0-	I	CSI0 CAMERA INTERFACE
		GND	P12	S13	GND		
CSI1 CAMERA INTERFACE	I	CSI1_RX2+	P13	S14	CSI0_RX1+	I	CSI0 CAMERA INTERFACE
CSI1 CAMERA INTERFACE	I	CSI1_RX2-	P14	S15	CSI0_RX1-	I	CSI0 CAMERA INTERFACE
		GND	P15	S16	GND		

CSI1 CAMERA INTERFACE	I	CSI1_RX3+	P16	S17	GBE1_MDI0+	I/O	GBE
CSI1 CAMERA INTERFACE	I	CSI1_RX3-	P17	S18	GBE1_MDI0-	I/O	GBE
		GND	P18	S19	GBE1_LINK100#	O	
GBE	I/O	GBE0_MDI3-	P19	S20	GBE1_MDI1+	I/O	GBE
GBE	I/O	GBE0_MDI3+	P20	S21	GBE1_MDI1-	I/O	GBE
GBE	O	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	O	
GBE	O	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	I/O	GBE
GBE	I/O	GBE0_MDI2-	P23	S24	GBE1_MDI2-	I/O	GBE
GBE	I/O	GBE0_MDI2+	P24	S25	GND		
GBE	O	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3-	I/O	GBE
GBE	I/O	GBE0_MDI1-	P26	S27	GBE1_MDI3+	I/O	GBE
GBE	I/O	GBE0_MDI1+	P27	S28	GBE1_CTREF	O	GBE
GBE	O	GBE0_CTREF	P28	S29	SERDES_0_TX+ / PCIE_D_TX+	O	SERDES / PCI-e
GBE	I/O	GBE0_MDI0-	P29	S30	SERDES_0_TX- / PCIE_D_TX-	O	SERDES / PCI-e
GBE	I/O	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	O	GBE
SPI 0 INTERFACE	O	SPI0_CS1#	P31	S32	SERDES_0_RX+ / PCIE_D_RX+	I	SERDES / PCI-e
		GND	P32	S33	SERDES_0_RX- / PCIE_D_RX-	I	SERDES / PCI-e
SDIO_CARD	I	SDIO_WP	P33	S34	GND		
SDIO_CARD	I/O	SDIO_CMD	P34	S35	USB4+	I/O	USB
SDIO_CARD	I	SDIO_CD#	P35	S36	USB4-	I/O	USB
SDIO_CARD	O	SDIO_CK	P36	S37	USB3_VBUS_DET	I	USB
SDIO_CARD	O	SDIO_PWR_EN	P37	S38	AUDIO_MCK	O	AUDIO
		GND	P38	S39	I2S0_LRCK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D0	P39	S40	I2S0_SDOUT	O	AUDIO
SDIO_CARD	I/O	SDIO_D1	P40	S41	I2S0_SDIN	I	AUDIO
SDIO_CARD	I/O	SDIO_D2	P41	S42	I2S0_CK	I/O	AUDIO
SDIO_CARD	I/O	SDIO_D3	P42	S43	ESPI_ALERT0#	I	ESPI INTERFACE
SPI 0 INTERFACE	O	SPI0_CS0#	P43	S44	ESPI_ALERT1#	I	ESPI INTERFACE
SPI 0 INTERFACE	O	SPI0_CK	P44	S45	MDIO_CLK/JTAG_TDI	O	SERDES
SPI 0 INTERFACE	I	SPI0_DIN	P45	S46	MDIO_DAT/JTAG_TDO	I/O	SERDES

SPI 0 INTERFACE	O	SPI0_DO	P46	S47	GND		
		GND	P47	S48	I2C_GP_CK	I/O	I2C
SATA	O	SATA_TX+	P48	S49	I2C_GP_DAT	I/O	I2C
SATA	O	SATA_TX-	P49	S50	I2S2_LRCK / HDA_SYNC	I/O	I2S / HD AUDIO
		GND	P50	S51	I2S2_SDOUT / HDA_SDO	O	I2S / HD AUDIO
SATA	I	SATA_RX+	P51	S52	I2S2_SDIN / HDA_SDI	I	I2S / HD AUDIO
SATA	I	SATA_RX-	P52	S53	I2S2_CK / HDA_CK	O	I2S / HD AUDIO
		GND	P53	S54	SATA_ACT#	O	SATA
SPI 1 / eSPI INTERFACE	O	SPI1_CS0#/ESPI_CS0#	P54	S55	USB5_EN_OC#	I/O	USB
SPI 1 / eSPI INTERFACE		SPI1_CS1#/ESPI_CS1#	P55	S56	ESPI_IO_2	I/O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	O	SPI1_CK / ESPI_CK	P56	S57	ESPI_IO_3	I/O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	I/O	SPI1_DIN / ESPI_IO_1	P57	S58	ESPI_RESET#	O	eSPI INTERFACE
SPI 1 / eSPI INTERFACE	I/O	SPI1_DO / ESPI_IO_0	P58	S59	USB5+	I/O	USB
		GND	P59	S60	USB5-	I/O	USB
USB	I/O	USB0+	P60	S61	GND		
USB	I/O	USB0-	P61	S62	USB3_SSTX+	O	USB
USB	I/O	USB0_EN_OC#	P62	S63	USB3_SSTX-	O	USB
USB	I	USB0_VBUS_DET	P63	S64	GND		
USB	I	USB0_OTG_ID	P64	S65	USB3_SSRX+	I	USB
USB	I/O	USB1+	P65	S66	USB3_SSRX-	I	USB
USB	I/O	USB1-	P66	S67	GND		
USB	I/O	USB1_EN_OC#	P67	S68	USB3+	I/O	USB
		GND	P68	S69	USB3-	I/O	USB
USB	I/O	USB2+	P69	S70	GND		
USB	I/O	USB2-	P70	S71	USB2_SSTX+	O	USB
USB	I/O	USB2_EN_OC#	P71	S72	USB2_SSTX-	O	USB
Reserved Purpose Signal	I/O	RSVD#P72 (JTAG_RST#)	P72	S73	GND		
Reserved Purpose Signal	I/O	RSVD#P73 (JTAG_TRST#)	P73	S74	USB2_SSRX+	I	USB
USB	I/O	USB3_EN_OC#	P74	S75	USB2_SSRX-	I	USB
PCI_e	O	PCIE_A_RST#	P75	S76	PCIE_B_RST#	O	PCI-e

USB	I/O	USB4_EN_OC#	P76	S77	PCIE_C_RST#	O	PCI-e
PCI-e	I	PCIE_B_CLKREQ# (JTAG_TMS)	P77	S78	SERDES_1_RX+ / PCIE_C_RX+	I	SERDES / PCI-e
PCI-e	I	PCIE_A_CLKREQ# (JTAG_TCK)	P78	S79	SERDES_1_RX- / PCIE_C_RX-	I	SERDES / PCI-e
		GND	P79	S80	GND		PCI-e
PCI-e	O	PCIE_C_REFCK+	P80	S81	SERDES_1_TX+ / PCIE_C_TX+	O	SERDES / PCI-e
PCI-e	O	PCIE_C_REFCK-	P81	S82	SERDES_1_TX- / PCIE_C_TX-	O	SERDES / PCI-e
		GND	P82	S83	GND		
PCI-e	O	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	O	PCI-e
PCI-e	O	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	O	PCI-e
		GND	P85	S86	GND		
PCI-e	I	PCIE_A_RX+	P86	S87	PCIE_B_RX+	I	PCI-e
PCI-e	I	PCIE_A_RX-	P87	S88	PCIE_B_RX-	I	PCI-e
		GND	P88	S89	GND		
PCI-e	O	PCIE_A_TX+	P89	S90	PCIE_B_TX+	O	PCI-e
PCI-e	O	PCIE_A_TX-	P90	S91	PCIE_B_TX-	O	PCI-e
		GND	P91	S92	GND		
HDMI/DP++ INTERFACE #1	O	HDMI_D2+ / DP1_LANE0+	P92	S93	DP0_LANE0+	O	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_D2- / DP1_LANE0-	P93	S94	DP0_LANE0-	O	DP++ INTERFACE #0
		GND	P94	S95	DP0_AUX_SEL	I	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_D1+ / DP1_LANE1+	P95	S96	DP0_LANE1+	O	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_D1- / DP1_LANE1-	P96	S97	DP0_LANE1-	O	DP++ INTERFACE #0
		GND	P97	S98	DP0_HPD	I	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_D0+ / DP1_LANE2+	P98	S99	DP0_LANE2+	O	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_D0- / DP1_LANE2-	P99	S100	DP0_LANE2-	O	DP++ INTERFACE #0
		GND	P100	S101	GND		
HDMI/DP++ INTERFACE #1	O	HDMI_CK+/ DP1_LANE3+	P101	S102	DP0_LANE3+	O	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	O	HDMI_CK- / DP1_LANE3-	P102	S103	DP0_LANE3-	O	DP++ INTERFACE #0
		GND	P103	S104	USB3_OTG_ID	I	USB
HDMI/DP++ INTERFACE #1	I	HDMI_HPD / DP1_HPD	P104	S105	DP0_AUX+	I/O	DP++ INTERFACE #0
HDMI/DP++ INTERFACE #1	I/O	HDMI_CTRL_CK/DP1_AUX+	P105	S106	DP0_AUX-	I/O	DP++ INTERFACE #0

HDMI/DP++ INTERFACE #1	I/O	HDMI_CTRL_DAT/DP1_AUX-	P106	S107	LCD1_BKLT_EN	O	LCD_SUPPORT
HDMI/DP++ INTERFACE #1	I	DP1_AUX_SEL	P107	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	O	PRIMARY_DISPLAY
GPIO / CSI 0 CAMERA	I/O	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	O	PRIMARY_DISPLAY
GPIO / CSI 1 CAMERA	I/O	GPIO1 / CAM1_PWR#	P109	S110	GND		
GPIO / CSI 0 CAMERA	I/O	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	O	PRIMARY_DISPLAY
GPIO / CSI 1 CAMERA	I/O	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	O	PRIMARY_DISPLAY
GPIO / HDA AUDIO	I/O	GPIO4 / HDA_RST#	P112	S113	eDP0_HPD	I	PRIMARY_DISPLAY
GPIO	I/O	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO6 / TACHIN	P114	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO7	P115	S116	LCD1_VDD_EN	O	LCD_SUPPORT
GPIO	I/O	GPIO8	P116	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO9	P117	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	O	PRIMARY_DISPLAY
GPIO	I/O	GPIO10	P118	S119	GND		
GPIO	I/O	GPIO11	P119	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	O	PRIMARY_DISPLAY
		GND	P120	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	O	PRIMARY_DISPLAY
MANAGEMENT	I/O	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	O	LCD_SUPPORT
MANAGEMENT	I/O	I2C_PM_DAT	P122	S123	GPIO13	I/O	GPIO
BOOT_SEL	I	BOOT_SEL0#	P123	S124	GND		
BOOT_SEL	I	BOOT_SEL1#	P124	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	O	PRIMARY_DISPLAY
BOOT_SEL	I	BOOT_SEL2#	P125	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	O	PRIMARY_DISPLAY
MANAGEMENT	O	RESET_OUT#	P126	S127	LCD0_BKLT_EN	O	LCD_SUPPORT

MANAGEMENT	I	RESET_IN#	P127	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	O	PRIMARY_DISPLAY
MANAGEMENT	I	POWER_BTN#	P128	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_TX	P129	S130	GND		
ASYNC_SERIAL	I	SER0_RX	P130	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER0_RTS#	P131	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER0_CTS#	P132	S133	LCD0_VDD_EN	O	LCD_SUPPORT
		GND	P133	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER1_TX	P134	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER1_RX	P135	S136	GND		
ASYNC_SERIAL	O	SER2_TX	P136	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	O	PRIMARY_DISPLAY
ASYNC_SERIAL	I	SER2_RX	P137	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	O	PRIMARY_DISPLAY
ASYNC_SERIAL	O	SER2_RTS#	P138	S139	I2C_LCD_CK	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER2_CTS#	P139	S140	I2C_LCD_DAT	I/O	LCD_SUPPORT
ASYNC_SERIAL	O	SER3_TX	P140	S141	LCD0_BKLT_PWM	O	LCD_SUPPORT
ASYNC_SERIAL	I	SER3_RX	P141	S142	GPIO12	I/O	GPIO
		GND	P142	S143	GND		
CAN	O	CAN0_TX	P143	S144	eDP0_HPD	I	PRIMARY_DISPLAY
CAN	I	CAN0_RX	P144	S145	WDT_TIME_OUT#	O	WATCHDOG
CAN	O	CAN1_TX	P145	S146	PCIE_WAKE#	I	PCI_e
CAN	I	CAN1_RX	P146	S147	VDD_RTC		
		VDD_IN	P147	S148	LID#	I	MANAGEMENT
		VDD_IN	P148	S149	SLEEP#	I	MANAGEMENT
		VDD_IN	P149	S150	VIN_PWR_BAD#	I	MANAGEMENT
		VDD_IN	P150	S151	CHARGING#	I	MANAGEMENT

	VDD_IN	P151	S152	CHARGER_PRSNT#	I	MANAGEMENT
	VDD_IN	P152	S153	CARRIER_STBY#	O	MANAGEMENT
	VDD_IN	P153	S154	CARRIER_PWR_ON	O	MANAGEMENT
	VDD_IN	P154	S155	FORCE_RECOV#	I	BOOT_SEL
	VDD_IN	P155	S156	BATLOW#	I	MANAGEMENT
	VDD_IN	P156	S157	TEST#	I	MANAGEMENT
			S158	GND		

3.3.2 LVDS / MIPI-DSI connector

LVDS connector – CN14			
Pin	**Signal**	**Pin**	**Signal**
2	VDD_BKLT0	1	VDD_LCD0
4	VDD_BKLT0	3	VDD_LCD0
6	VDD_BKLT0	5	VDD_LCD0
8	GND	7	3.3V_RUN
10	LVDS0_D0+_CONN	9	GND
12	LVDS0_D0-_CONN	11	LVDS0_D1+_CONN
14	GND	13	LVDS0_D1-_CONN
16	LVDS0_D2+_CONN	15	GND
18	LVDS0_D2-_CONN	17	LVDS0_D3+_CONN
20	GND	19	LVDS0_D3-_CONN
22	LVDS0_CLK+_CONN	21	GND
24	LVDS0_CLK-_CONN	23	LVDS1_D0+_CONN
26	GND	25	LVDS1_D0-_CONN
28	LVDS1_D1+_CONN	27	GND
30	LVDS1_D1-_CONN	29	LVDS1_D2+_CONN
32	GND	31	LVDS1_D2-_CONN
34	LVDS1_D3+_CONN	33	GND
36	LVDS1_D3-_CONN	35	LVDS1_CLK+_CONN
38	GND	37	LVDS1_CLK-_CONN
40	GND	39	GND
42	LCD0_BKLT_PWM_3V3	41	LCD0_BKLTEN_3V3
44	LCD0_VDD_EN_3V3	43	---
46	---	45	---
48	---	47	---
50	LVDS_DDC_CLK_3V3	49	LVDS_DDC_DAT_3V3

According to SMARC® Rel. 2.1.1 specification, the primary display interface from card edge connector can be used to implement multi-purpose Digital Display Interfaces.

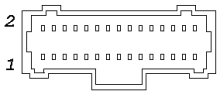
The primary display interface can support LVDS video interface, allowing the connection of displays with a colour depth of 18 or 24 bit, in single or dual channel configuration. Alternatively, the same pins can be used to support up to two Embedded Display Ports or MIPI DSI interface.

Please notice that the effective support of this kind of displays depends only by the SMARC® module used with the CSM-B79 carrier board, it is not a feature dependent from the carrier board itself.

The pin-out of this card edge connector is given according to SMARC® Rel. 2.1.1 specifications, so that the carrier board is ready for the use of any SMARC® module that follows those specifications. Please refer to the SMARC® module's User manual for the details regarding the panels supported and the availability of the LVDS / eDP / MIPI-DSI signals.

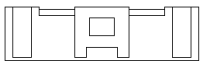
CSM-B79 board allows to interface to Single/Dual Channel 18-/24-bit displays, using the LVDS channel coming directly from the SMARC® module Single-Dual Channel 18-24-bit connector.

The LVDS interface will be available on connector CN14, type HR A1014WV-S-2x25P or equivalent (2 x 25p, male, straight, P1, low profile, polarised), with the pin-out shown in the table on the left



Mating connector: HR A1014H-2X25P with HR A1014-T female crimp terminals.

Alternative mating connector, MOLEX 501189-5010 with crimp terminals series 501334.



On the same connector, are also implemented voltage rails that can be used to supply the Backlight Unit and related LCD and signals for direct driving of display's backlight: voltages (VDD_BKLT0 and VDD_LCD0) and control signals (LCD enable signal, LCD0_VDD_EN, Backlight enable signal, LCD0_BKLTEN, and Backlight Brightness Control signal, LCD0_BKLT_PWM).

When building a cable for connection of LVDS displays, please take care of twist as tight as possible differential pairs' signal wires, in order to reduce EMI interferences. Shielded cables are also recommended.

Signal Description:

LVDS0_D[0..3]+_CONN / LVDS0_D[0..3]-_CONN: SMARC® Module LVDS Channel#0 Differential pairs

LVDS0_CLK+_CONN / LVDS0_CLK-_CONN: SMARC® Module LVDS Channel#0 Differential clock

LVDS1_D[0..3]+_CONN / LVDS1_D[0..3]-_CONN: SMARC® Module LVDS Channel#1 Differential pairs

LVDS1_CLK+_CONN / LVDS1_CLK-_CONN: SMARC® Module LVDS Channel#1 Differential clock

LVDS_DDC_DAT_3V3: Display ID Data line for Flat Panel detection and control. Signal derived by I2C_LCD_DAT from SMARC® Module through voltage level translator. Bidirectional signal, +3.3V_RUN electrical level with 2k2 pull up resistor

LVDS_DDC_CLK_3V3: Display ID Clock line for Flat Panel detection and control. Signal derived by I2C_LCD_CK from SMARC® Module through voltage level translator. Bidirectional signal, +3.3V_RUN electrical level with 2k2 pull up resistor

LCD0_VDD_EN_3V3: LVDS Panel power for LCD Enable Signal, derived by LCD0_VDD_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

LCD0_BKLTEN_3V3: LVDS Panel power for Backlight Enable Signal, derived by LCD0_BKLT_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

LCD0_BKLT_PWM_3V3: LVDS Panel Backlight Brightness Control, PWM signal derived by LCD0_BKLT_PWM from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

SW6 position	LVDS / eDP selector
ON position (1-3)	eDP1
OFF position (1-3)	LVDS1 / DSI1
ON position (2-4)	eDP0
OFF position (2-4)	LVDS0 / DSI0

In order to match the CSM-B79 Carrier Board with the primary display interfaces effectively available on the SMARC® module, it is necessary to configure properly the dual DIP switch SW6, type ADIMPEX p/n KVT04602-R, according to the left table.

In order to support Dual Channel LVDS configuration or MIPI-DSI dual channel, both DIP switches must be placed in OFF positions.

CN18 position	LCD #0 PWR selector (VDD_LCD0)
1-2	+3.3V_RUN
2-3	+5V_RUN

The LCD Voltage rail VDD_LCD0 value can be set to +3.3V_RUN or +5V_RUN by using dedicated jumper CN18, which is a standard pin header, P2.54mm, 1x3 pin.

This selectable power rail is carried both to LVDS connector CN14 and eDP0 connector CN60 (par.3.3.3).

CN19 position	BKLT #0 PWR selector (VDD_BKLT0)
1-2	+12V_RUN
2-3	+5V_RUN

The Backlight Voltage rail VDD_BKLT0 value can be set to +5V_RUN or +12V_RUN by using dedicated jumper CN19, which is another standard pin header, P2.54mm, 1x3 pin.

This selectable power rail is carried both to LVDS connector CN14 and eDP0 connector CN60 (par.3.3.3).

CN20 position	LCD #1 PWR selector (VDD_LCD1)
1-2	+3.3V_RUN
2-3	+5V_RUN

The LCD Voltage rail VDD_LCD1 value can be set to +3.3V_RUN or +5V_RUN by using dedicated jumper CN20, which is a standard pin header, P2.54mm, 1x3 pin.

This selectable power rail is carried to eDP1 connector CN61 (par.3.3.3).

CN21 position	BKLT #1 PWR selector (VDD_BKLT1)
1-2	+12V_RUN
2-3	+5V_RUN

The Backlight Voltage rail VDD_BKLT1 value can be set to +5V_RUN or +12V_RUN by using dedicated jumper CN21, which is another standard pin header, P2.54mm, 1x3 pin.

This selectable power rail is carried to eDP1 connector CN61 (par.3.3.3).

Finally, these signals (VDD_LCD0, VDD_LCD1, VDD_BKLT0, VDD_BKLT1) are also carried to dedicated LCD panels voltage connectors CN16 and CN17 (par.3.3.4).

MIPI-DSI connector – CN14			
Pin	Signal	Pin	Signal
2	VDD_BKLT0	1	VDD_LCD0
4	VDD_BKLT0	3	VDD_LCD0
6	VDD_BKLT0	5	VDD_LCD0
8	GND	7	3.3V_RUN
10	DSI0_D0+_CONN	9	GND
12	DSI0_D0-_CONN	11	DSI0_D1+_CONN
14	GND	13	DSI0_D1-_CONN
16	DSI0_D2+_CONN	15	GND
18	DSI0_D2-_CONN	17	DSI0_D3+_CONN
20	GND	19	DSI0_D3-_CONN
22	DSI0_CLK+_CONN	21	GND
24	DSI0_CLK-_CONN	23	DSI1_D0+_CONN
26	GND	25	DSI1_D0-_CONN
28	DSI1_D1+_CONN	27	GND
30	DSI1_D1-_CONN	29	DSI1_D2+_CONN
32	GND	31	DSI1_D2-_CONN
34	DSI1_D3+_CONN	33	GND
36	DSI1_D3-_CONN	35	DSI1_CLK+_CONN
38	GND	37	DSI1_CLK-_CONN
40	GND	39	GND
42	LCD0_BKLT_PWM_3V3	41	LCD0_BKLTEN_3V3
44	LCD0_VDD_EN_3V3	43	---
46	---	45	---
48	---	47	---
50	LVDS_DDC_CLK_3V3	49	LVDS_DDC_DAT_3V3

As stated above, if supported by SMARC® module, the primary display interface can be used to connect up to two MIPI DSI (Display Serial Interface) displays.

The signals for MIPI DSI are carried to same connector CN14 used for LVDS interface. Proper setting of dual DIP switch SW6 is necessary for its availability.

The power for LCD panel (VDD_LCD0) and panel backlight (VDD_BKLT0) are the same is in LVDS mode. Also in this case, the selection is made by CN18 and CN19, as described above.

Finally, the DDC Clock and Data Lines used for Flat Panel Detection and Control are the same is in LVDS mode.

Signal Description:

DSI0_D[0..3]+_CONN / LVDS0_D[0..3]-_CONN: SMARC® Module MIPI-DSI Channel#0 Differential pairs

DSI0_CLK+_CONN / LVDS0_CLK-_CONN: SMARC® Module MIPI-DSI Channel#0 Differential clock

DSI1_D[0..3]+_CONN / LVDS1_D[0..3]-_CONN: SMARC® Module MIPI-DSI Channel#1 Differential pairs

DSI1_CLK+_CONN / LVDS1_CLK-_CONN: SMARC® Module MIPI-DSI Channel#1 Differential clock

3.3.3 eDP connectors

eDP #0 connector – CN60				eDP #1 connector – CN61			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	---	21	VDD_LCD0	1	---	21	VDD_LCD1
2	VDD_BKLT0	22	VDD_LCD0	2	VDD_BKLT1	22	VDD_LCD1
3	VDD_BKLT0	23	VDD_LCD0	3	VDD_BKLT1	23	VDD_LCD1
4	VDD_BKLT0	24	GND	4	VDD_BKLT1	24	GND
5	VDD_BKLT0	25	eDP0_AUX-	5	VDD_BKLT1	25	eDP1_AUX-
6	---	26	eDP0_AUX+	6	---	26	eDP1_AUX+
7	---	27	GND	7	---	27	GND
8	LCD0_BKLT_PWM_3.3V	28	eDP0_TX0+	8	LCD1_BKLT_PWM_3.3V	28	eDP1_TX0+
9	LCD0_BKLT_EN_3.3V	29	eDP0_TX0-	9	LCD1_BKLT_EN_3.3V	29	eDP1_TX0-
10	GND	30	GND	10	GND	30	GND
11	GND	31	eDP0_TX1+	11	GND	31	eDP1_TX1+
12	GND	32	eDP0_TX1-	12	GND	32	eDP1_TX1-
13	GND	33	GND	13	GND	33	GND
14	eDP0_HPD_3.3V	34	eDP0_TX2+	14	eDP1_HPD_3.3V	34	eDP1_TX2+
15	GND	35	eDP0_TX2-	15	GND	35	eDP1_TX2-
16	GND	36	GND	16	GND	36	GND
17	GND	37	eDP0_TX3+	17	GND	37	eDP1_TX3+
18	GND	38	eDP0_TX3-	18	GND	38	eDP1_TX3-
19	---	39	GND	19	---	39	GND
20	VDD_LCD0	40	---	20	VDD_LCD1	40	---

According to SMARC® Rel. 2.1.1 specification, the other support on primary display interface from card edge connector, on same pins that can be used for LVDS / MIPI-DSI (par.3.3.2), is the connection of up to two Embedded Display Ports.

For the connection of this kind of displays, on-board there are two VESA® certified connectors C60 and CN61 for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions).

On these connectors, VDD_LCD0 / VDD_LCD1 and VDD_BKLT0 / VDD_BKLT1 are the voltage rails that can be used to supply each Backlight Unit and related LCD.

Their value can be set using dedicated jumpers CN18, CN19, CN20, CN21 (par.3.3.2).

Here following the signals involved in eDP channel#0 management:

eDP0_TX[0..3]+ / eDP0_TX[0..3]-: SMARC® module embedded DP channel#0 differential data pairs

eDP0_AUX+ / eDP0_AUX-: SMARC® module embedded DP channel#0 auxiliary channel differential data pair.

eDP0_HPD_3.3V: embedded DP channel#0 Hot Plug Detect for SMARC® module. Active high signal, +3.3V_RUN electrical level with 100kΩ pull down resistor

LCD0_VDD_EN_3V3: eDP channel#0 Panel power for LCD Enable Signal, derived by LCD0_VDD_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

LCD0_BKLTEN_3V3: eDP channel#0 Panel power for Backlight Enable Signal, derived by LCD0_BKLT_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

LCD0_BKLT_PWM_3V3: eDP channel#0 Panel Backlight Brightness Control, PWM signal derived by LCD0_BKLT_PWM from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

Here following the signals involved in eDP channel#1 management:

eDP1_TX[0..3]+ / eDP1_TX[0..3]-: SMARC® module embedded DP channel#1 differential data pairs

eDP1_AUX+ / eDP1_AUX-: SMARC® module embedded DP channel#1 auxiliary channel differential data pair.

eDP1_HPD_3.3V: embedded DP channel#1 Hot Plug Detect for SMARC® module. Active high signal, +3.3V_RUN electrical level with 100kΩ pull down resistor

LCD1_VDD_EN_3V3: eDP channel#1 Panel power for LCD Enable Signal, derived by LCD1_VDD_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

LCD1_BKLTEN_3V3: eDP channel#1 Panel power for Backlight Enable Signal, derived by LCD1_BKLT_EN from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

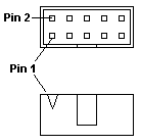
LCD1_BKLT_PWM_3V3: eDP channel#1 Panel Backlight Brightness Control, PWM signal derived by LCD1_BKLT_PWM from SMARC® Module through voltage level translator. +3.3V_RUN electrical level Output.

3.3.4 LCD Panels Voltage connectors

LCD Panel #0 Voltage connector – CN16				LCD Panel #1 Voltage connector – CN17			
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD_LCD0	2	VDD_BKLT0	1	VDD_LCD1	2	VDD_BKLT1
3	+5V_RUN	4	+12V_RUN	3	+5V_RUN	4	+12V_RUN
5	LCD0_VDD_EN_3V3	6	LCD0_BKLTEN_3V3	5	LCD1_VDD_EN_3V3	6	LCD1_BKLTEN_3V3
7	---	8	LCD0_BKLT_PWM_3V3	7	---	8	LCD1_BKLT_PWM_3V3
9	GND	10	GND	9	GND	10	GND

It is possible to use two additional connectors for connecting LCD panels voltage rails, both for LCD and for backlights.

LCD and backlight voltages can be set by using dedicated jumpers CN18, CN19, CN20 and CN21 described in par.3.3.2.



CN16 and CN17, are two IDC connectors, dual row, 10 pin, p2.54 mm connector, type MOLEX p/n 70246-1004 or equivalent.

Mating connector: MOLEX p/n 22-25-2102 with 70058 series female crimp terminals.

3.3.5 HDMI / DP1++ connectors

HDMI Connector – CN79			
Pin	**Signal**	**Pin**	**Signal**
1	HDMI_D2+_CON	2	GND
3	HDMI_D2-_CON	4	HDMI_D1+_CON
5	GND	6	HDMI_D1-_CON
7	HDMI_D0+_CON	8	GND
9	HDMI_D0-_CON	10	HDMI_CLK+_CON
11	GND	12	HDMI_CLK-_CON
13	---	14	---
15	HDMI_DDC_CLK_CON	16	HDMI_DDC_DAT_CON
17	GND	18	+5V$_{HDMI}$
19	HDMI_HPD_CON		

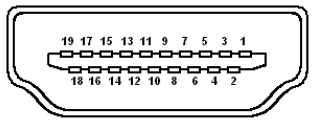
According to SMARC® Rel. 2.1.1 specification, the secondary display interface from card edge connector can be used to implement multi-purpose Digital Display Interfaces.

The secondary display interface can support native HDMI video interface. Alternatively, the same pins can be used to support one multimode display port, that can be either used as DP or HDMI interface. It also allows the use of DP++ to HDMI dongles.

Please notice that the effective support of this kind of displays depends only by the SMARC® module used with the CSM-B79 carrier board, it is not a feature dependent from the carrier board itself.

The pin-out of this card edge connector is given according to SMARC® Rel 2.1.1 specifications, so that the carrier board is ready for the use of any SMARC® module that follows those specifications. Please refer to the SMARC® module's User manual for the details regarding the panels supported and the availability of the HDMI / DP++ signals.

CSM-B79 board allows to interface to HDMI display, using the HDMI channel coming directly from the SMARC® module connector. This interface will be available on a standard certified HDMI connector CN79, type A, model MOLEX p/n 2086581001, with the pinout shown in the table on the left



Signals involved in HDMI management are the following:

HDMI_CLK+_CON / HDMI_CLK-_CON: SMARC® module HDMI differential Clock.

HDMI_D0+_CON / HDMI_D0-_CON: SMARC® module HDMI differential pair #0.

HDMI_D1+_CON / HDMI_D1-_CON: SMARC® module HDMI differential pair #1.

HDMI_D2+_CON / HDMI_D2-_CON: SMARC® module HDMI differential pair #2.

HDMI_DDC_DAT_CON: DDC Data line for HDMI panel. Bidirectional signal, electrical level +5V$_{HDMI}$ with 1.8kΩ pull up resistor

HDMI_DDC_CLK_CON: DDC Clock line for HDMI panel. Bidirectional signal, electrical level +5V$_{HDMI}$ with 1.8kΩ pull up resistor

HDMI_HPD_CON: Hot Plug Detect Input signal. Active high signal, +5V_RUN electrical level with 100kΩ pull down resistor

+5V$_{HDMI}$: Power voltage reference for HDMI, directly derived from +5V_RUN.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Always use HDMI-certified cables for the connection between the board and the HDMI display; a category 2 (High-Speed) cable is recommended for higher resolutions, category 1 cables can be used for 720p resolution.

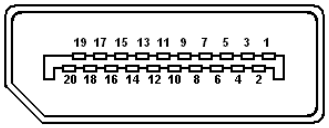
CN75 position	HDMI / DP#1 selector
1-2	HDMI
2-3	DP#1

In order to match the CSM-B79 Carrier Board with the secondary display interfaces effectively available on the SMARC® module, it is necessary to configure properly dedicated jumper CN75, which is a standard pin header, P2.54mm, 1x3 pin.

In order to support HDMI configuration, the jumper must be placed in 1-2 position.

Multimode DP#1 Connector – CN11			
Pin	Signal	Pin	Signal
1	DDI1_PAIR0+	2	GND
3	DDI1_PAIR0-	4	DDI1_PAIR1+
5	GND	6	DDI1_PAIR1-
7	DDI1_PAIR2+	8	GND
9	DDI1_PAIR2-	10	DDI1_PAIR3+
11	GND	12	DDI1_PAIR3-
13	DDI1_DDC_AUX_SEL	14	DDI1_CEC
15	DDI1_CTRLCLK_AUX+	16	GND
17	DDI1_CTRLDATA_AUX-	18	DDI1_HPD
19	GND	20	DD1_PWR

According to SMARC® Rel 2.1.1 specification, the other support on secondary display interface from card edge connector, on same pins that can be used for HDMI, is the connection to one right-angle standard DisplayPort Connector CN11, supporting DP++, type WINNING p/n WDPE-20F3L1BU3 or equivalent, with the pinout shown in the left table.



Signal Description:

DDI1_PAIR0+/DDI1_PAIR0-: SMARC® module DDI Interface #1 Differential Pair #0. Can be used as Display Port differential pair #0 or TMDS (HDMI) differential pair #2

DDI1_PAIR1+/DDI1_PAIR1-: SMARC® module DDI Interface #1 Differential Pair #1. Can be used as Display Port differential pair #1 or TMDS (HDMI) differential pair #1

DDI1_PAIR2+/DDI1_PAIR2-: SMARC® module DDI Interface #1 Differential Pair #2. Can be used as Display Port differential pair #2 or TMDS (HDMI) differential pair #0

DDI1_PAIR3+/DDI1_PAIR3-: SMARC® module DDI Interface #1 Differential Pair #3. Can be used as Display Port differential pair #3 or TMDS (HDMI) Clock differential pair

DDI1_CTRLCLK_AUX+/DDI1_CTRLDATA_AUX-: SMARC® module DDI Interface #1, Auxiliary channel for Display Port (differential pair) or DDC Clock and Data Line for TMDS

DDI1_HPD: DDI Interface #1 Hot Plug Detect. This signal is tied to GND through a 100kΩ resistor

DDI1_DDC_AUX_SEL: DDI Interface #1 Cable Adapter Detect signal. When this signal is detected high, then on the connector there is the TMDS interface (it means that a DP-to-HDMI adapter is connected). This signal is tied to GND through a 1MOhm resistor. Please refer to CN76 jumper for detailed description.

DDI1_CEC: this signal is tied to GND through a 5.1MOhm resistor

DD1_PWR: Power voltage reference for DisplayPort, directly derived from +3.3V_RUN through a current limited power switch

To redirect signals coming from card edge connector to this DP1++ connector, there is an onboard high-speed multiplexer, driven by 2-way jumper CN75, described above, that must be placed in 2-3 position. When selected, it is possible to configure this multimode display port to work in standard mode condition, i.e. can be either used as DP interface or HDMI with the use of external DP++ to HDMI dongle, or fixed HDMI or DP mode condition. This can be set with the 4-way jumper CN76 described below.

CN76 position	DP1++ Working mode
1-3	Fixed HDMI mode (DDC available)
3-4	Multimode DP (standard working)
3-5	Fixed DP mode (DP_AUX available)

Since CSM-B79 is a carrier board specifically designed for development purposes, onboard there is a 4-way jumper to select normal working of HDMI/DP1++ interface or to fix this interface's behaviour in DP or HDMI mode.

To select standard mode working, the jumper must be set in 3-4 position.

3.3.6 DP0++ connector

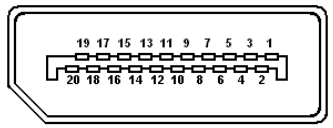
Multimode DP#0 Connector – CN74			
Pin	Signal	Pin	Signal
1	DDI0_PAIR0+	2	GND
3	DDI0_PAIR0-	4	DDI0_PAIR1+
5	GND	6	DDI0_PAIR1-
7	DDI0_PAIR2+	8	GND
9	DDI0_PAIR2-	10	DDI0_PAIR3+
11	GND	12	DDI0_PAIR3-
13	DDI0_DDC_AUX_SEL	14	DDI0_CEC
15	DDI0_CTRLCLK_AUX+	16	GND
17	DDI0_CTRLDATA_AUX-	18	DDI0_HPD
19	GND	20	DD0_PWR

According to SMARC® Rel. 2.1.1 specification, also the third display interface from card edge connector can be used to implement multi-purpose Digital Display Interfaces. As stated in the specification, the third display interface can support multimode display port, that can be either used as DP++ interface or HDMI over DP++ through external dongle. The difference with second display interface is that this one cannot support native HDMI, and this is the reason why there is not an high speed multiplexer to redirect signals from card edge connector as per second display interface (par.3.3.5)

Please notice that the effective support of this kind of displays depends only by the SMARC® module used with the CSM-B79 carrier board, it is not a feature dependent from the carrier board itself.

The pin-out of this card edge connector is given according to SMARC® Rel. 2.1.1 specifications, so that the carrier board is ready for the use of any SMARC® module that follows those specifications. Please refer to the SMARC® module's User manual for the details regarding the panels supported and the availability of the HDMI / DP++ signals.

The multimode Display Port interface (DP0++) from card edge connector is made available on connector CN74, type WINNING p/n WDPE-20F3L1BU3 or equivalent, with the pinout shown in the left table.



Signal Description:

DDI0_PAIR0+/DDI0_PAIR0-: SMARC® module DDI Interface #0 Differential Pair #0. Can be used as Display Port differential pair #0 or TMDS (HDMI) differential pair #2

DDI0_PAIR1+/DDI0_PAIR1-: SMARC® module DDI Interface #0 Differential Pair #1. Can be used as Display Port differential pair #1 or TMDS (HDMI) differential pair #1

DDI0_PAIR2+/DDI0_PAIR2-: SMARC® module DDI Interface #0 Differential Pair #2. Can be used as Display Port differential pair #2 or TMDS (HDMI) differential pair #0

DDI0_PAIR3+/DDI0_PAIR3-: SMARC® module DDI Interface #0 Differential Pair #3. Can be used as Display Port differential pair #3 or TMDS (HDMI) Clock differential pair

DDI0_CTRLCLK_AUX+/DDI0_CTRLDATA_AUX-: SMARC® module DDI Interface #0, Auxiliary channel for Display Port (differential pair) or DDC Clock and Data Line for TMDS

DDI0_HPD: DDI Interface #0 Hot Plug Detect. This signal is tied to GND through a 100kΩ resistor

DDI0_DDC_AUX_SEL: DDI Interface #0 Cable Adapter Detect signal. When this signal is detected high, then on the connector there is the TMDS interface (it means that a DP-to-HDMI adapter is connected). This signal is tied to GND through a 1MOhm resistor. Please refer to CN76 jumper for detailed description.

DDI0_CEC: this signal is tied to GND through a 5.1MOhm resistor

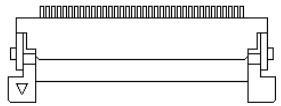
DD0_PWR: Power voltage reference for DisplayPort, directly derived from +3.3V_RUN through a current limited power switch

3.3.7 CSI Camera Connector

CSI Camera Connector – CN39			
Pin	Signal	Pin	Signal
1	+3.3V_RUN	19	I2C_CAM1_DAT
2	+3.3V_RUN	20	GPIO1/CAM1_PWR#
3	CSI1_RX0+	21	CAM_MCLK
4	CSI1_RX0-	22	GPIO0/CAM0_PWR#
5	GND	23	I2C_CAM0_CK
6	CSI1_RX1+	24	I2C_CAM0_DAT
7	CSI1_RX1-	25	GND
8	GND	26	CSI0_CK+
9	CSI1_RX2+	27	CSI0_CK-
10	CSI1_RX2-	28	GND
11	GPIO3/CAM1_RST#	29	CSI0_RX0+
12	CSI1_RX3+	30	CSI0_RX0-
13	CSI1_RX3-	31	GPIO2/CAM0_RST#
14	GND	32	CSI0_RX1+
15	CSI1_CK+	33	CSI0_RX1-
16	CSI1_CK-	34	GND
17	GND	35	---
18	I2C_CAM1_CK	36	---

According to SMARC® Rel. 2.1.1 specification, SMARC® module can offer up to two MIPI CSI serial camera interfaces. MIPI CSI0 supports up to two differential data lanes, while MIPI CSI1 can support up to four differential data lanes.

Both interfaces are carried to an FFC/FPC connector CN39, type Hirose p/n FH12A-36S-0.5SH(55), which is able to accept 36 poles 0.5mm pitch FFC cables, with the pinout shown in the table on the left.



Signal related to MIPI CSI0 (2-lanes MIPI-CSI) interface:

CSI0_RX0+ / CSI0_RX0-: SMARC® module MIPI CSI0 Port differential data pair #0

CSI0_RX1+ / CSI0_RX1-: SMARC® module MIPI CSI0 Port differential data pair #1

CSI0_CK+ / CSI0_CK-: SMARC® module MIPI CSI0 Port differential clock pair

I2C_CAM0_CK: SMARC® module I2C Bus clock line for MIPI CSI0 data support link

I2C_CAM0_DAT: SMARC® module I2C Bus data line for MIPI CSI0 data support link

GPIO0 / CAM0_PWR#: Power Enable for MIPI CSI0, Active Low Output. This signal shares the same pin from card edge connector with GPIO0 (par.3.3.27)

GPIO2 / CAM0_RST#: Reset signal for MIPI CSI0, Active Low Output. This signal shares the same pin from card edge connector with GPIO2 (par.3.3.27)

Signal related to MIPI CSI1 (4-lanes MIPI-CSI) interface:

CSI1_RX0+ / CSI1_RX0-: SMARC® module MIPI CSI1 Port differential data pair #0

CSI1_RX1+ / CSI1_RX1-: SMARC® module MIPI CSI1 Port differential data pair #1

CSI1_RX2+ / CSI1_RX2-: SMARC® module MIPI CSI1 Port differential data pair #2

CSI1_RX3+ / CSI1_RX3-: SMARC® module MIPI CSI1 Port differential data pair #3

CSI1_CK+ / CSI1_CK-: SMARC® module MIPI CSI1 Port differential clock pair

I2C_CAM1_CK: SMARC® module I2C Bus clock line for MIPI CSI1 data support link

I2C_CAM1_DAT: SMARC® module I2C Bus data line for MIPI CSI1 data support link

GPIO1 / CAM1_PWR#: Power Enable for MIPI CSI1, Active Low Output. This signal shares the same pin from card edge connector with GPIO1 (par.3.3.27)

GPIO3 / CAM1_RST#: Reset signal for MIPI CSI1, Active Low Output. This signal shares the same pin from card edge connector with GPIO3 (par.3.3.27)

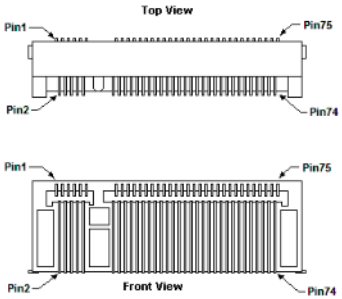
3.3.8 S-ATA connectors

M.2 SSD Slot (Socket 2 Key B type 2230/2242/2260) – CN35			
Pin	**Signal**	**Pin**	**Signal**
1	---	2	+3.3V_RUN
3	GND	4	+3.3V_RUN
5	GND	6	---
7	---	8	---
9	---	10	---
11	GND	20	---
21	---	22	---
23	---	24	---
25	---	26	---
27	GND	28	---
29	---	30	---
31	---	32	---
33	GND	34	---
35	---	36	---
37	---	38	---
39	GND	40	---
41	SATA_RX+	42	---
43	SATA_RX-	44	---
45	GND	46	---
47	SATA_TX-	48	---
49	SATA_TX+	50	---
51	GND	52	---
53	---	54	---

According to SMARC® Rel. 2.1.1 specification, SMARC® module can offer only one SATA interface, but there are plenty of different devices that the customer could use. For this reason, on CSM-B79 carrier board are available both a standard SATA Male 7 poles connector CN34 with dedicated power connector CN37 (par.3.3.9) and an M.2 Slot for SSD on M.2 Socket 2 Key B form factor.

The connector used for the M.2 SSD slot is CN35, which is a standard 75 pin M.2 Key B connector, type LOTES p/n APCI0087-P001A, H=8.5mm, with the pinout shown in the table on the left.

On the CSM-B79 carrier board there is also a Threaded Spacer which allows the placement of M.2 Socket 2 Key B SSD modules in 2230, 2242 or 2260 size.



55	---	56	---
57	GND	58	---
59	---	60	---
61	---	62	---
63	---	64	---
65	---	66	---
67	---	68	---
69	SATA_M2_SELECT#	70	+3.3V_RUN
71	GND	72	+3.3V_RUN
73	GND	74	+3.3V_RUN
75	---		

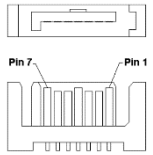
Signal Description:

SATA_TX+/SATA_TX-: Serial ATA Transmit differential pair.

SATA_RX+/SATA_RX-: Serial ATA Receive differential pair.

SATA 7p M Connector – CN34	
Pin	**Signal**
1	GND
2	SATA_TX-
3	SATA_TX+
4	GND
5	SATA_RX+
6	SATA_RX-
7	GND

For the connection of external Mass Storage Devices, there is a standard male S-ATA connector, CN34.



Since SMARC® modules can manage only one S-ATA interface, then only one of the two connectors (the SATA 7p M connector CN34 and the SATA M.2 SSD slot CN35) can work at a time.

Switching between the two connectors is automatic, and it is managed by the signal SATA_M2_SELECT# available on SATA M.2 Slot CN35 (pin 69).

When M.2 SSD is not plugged, the SATA interface is redirected by default to the 7p M connector CN34.

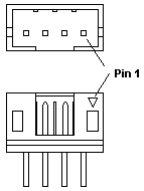
Vice versa, when M.2 SSD is plugged, the SATA interface is redirected by default to SATA M.2 SSD slot CN35.

When both an M.2 SSD and a SATA Drive are plugged, the SATA interface is switched toward the M.2 slot.

3.3.9 S-ATA Power Connector

S-ATA Power Connector – CN37	
Pin	**Signal**
1	+12V_RUN
2	GND
3	GND
4	+5V_RUN

A dedicated power connector, CN37, can be used to give supply to external Hard Disks (or Solid State Disks) connected to the SATA male connector CN34.



The dedicated power connector is a 4-pin male connector, type MOLEX p/n 89400-0420 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 87369-0400 crimp housing with MOLEX 51021 crimp terminals.

3.3.10 microSD Slot

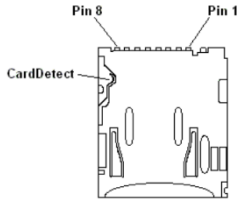
microSD Card Slot – CN77	
Pin	**Signal**
1	SDIO_D2
2	SDIO_D3
3	SDIO_CMD
4	SDIO_PWR
5	SDIO_CK
6	GND
7	SDIO_D0
8	SDIO_D1
CardDetect	SDIO_CD#

According to SMARC® Rel. 2.1.1 specification, SMARC® module can support signals for Secure Digital Input/Output and MultiMedia cards over the SMARC® SDIO interface, for the use of standard SD or MMC cards, to be used as Mass Storage Device and/or Boot Device (if the SMARC® module used with CSM-B79 implements this functionality).

Please refer to the User Manual of the used SMARC® module for information about Card types supported by the chipset.

The connector is a microSD connector, push-push type, H=1.68 mm, type JST DM3AT-SF-PEJM5 or equivalent.

Signal Description:



SDIO_CD#: Card Detect Input, indicating when a SDIO/MMC card is present

SDIO_CK: SD Clock Line (output)

SDIO_CMD: Command/Response bidirectional line, used for card initialization and for command transfers.

SDIO_D[0÷3]: SD Card data bus, SDIO_D0 signal is used for all communication mode, SDIO_D[1÷3] signals are required for 4-bit communication mode

SDIO_PWR voltage is derived from +3.3V_ALW power rail. It can be switched on and off via SW (SDIO_PWR_EN signal, managed directly by the SMARC® module).

For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

JP5 position	SDIO Write Protect
Not inserted	WP Enabled: microSD card cannot be written
Inserted	WP Disabled: microSD card can be written

Since microSD cards do not support the Write Protect functionality, which is instead supported by SMARC® module, then on CSM-B79 carrier board it is available a 2-way jumper, JP5, which allows forcing Write Protect signal input SDIO_WP, directly managed by the SMARC® module

3.3.11 Gigabit Ethernet connectors

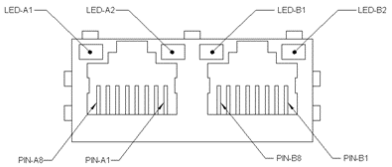
Gigabit Ethernet Ports #0 #1- CN27			
Pin	Signal	Pin	Signal
A1	GBE0_MDI0+	A5	GBE0_MDI2-
A2	GBE0_MDI0-	A6	GBE0_MDI1-
A3	GBE0_MDI1+	A7	GBE0_MDI3+
A4	GBE0_MDI2+	A8	GBE0_MDI3-
B1	GBE1_MDI0+	B5	GBE1_MDI2-
B2	GBE1_MDI0-	B6	GBE1_MDI1-
B3	GBE1_MDI1+	B7	GBE1_MDI3+
B4	GBE1_MDI2+	B8	GBE1_MDI3-

Gigabit Ethernet Ports #2 #3 - CN28			
Pin	Signal	Pin	Signal
A1	GBE2_MDI0+	A5	GBE2_MDI2-
A2	GBE2_MDI0-	A6	GBE2_MDI1-
A3	GBE2_MDI1+	A7	GBE2_MDI3+
A4	GBE2_MDI2+	A8	GBE2_MDI3-
B1	GBE3_MDI0+	B5	GBE3_MDI2-
B2	GBE3_MDI0-	B6	GBE3_MDI1-
B3	GBE3_MDI1+	B7	GBE3_MDI3+
B4	GBE3_MDI2+	B8	GBE3_MDI3-

According to SMARC® Rel. 2.1.1 specification, SMARC® module offers up to two Gigabit Ethernet interfaces, including GbE MAC and PHY.

Only the isolation magnetic (with a 1:1 turn ratio) is required.

For this reason, on board there is a double port RJ-45 socket CN27, type TRXCOM p/n TRJG27420AINL or equivalent, with 2kV decoupling capacitors.



According to SMARC® Rel 2.1.1 specification, SMARC® module can use SERDES (SERialized and DESerialized signals on a high-speed differential line) interfaces to implement additional LAN ports.

On CSM-B79 carrier board, SERDES0 and SERDES1 interfaces are utilized to connect an SGMII PHY to the interface. For this reason, there is a Gigabit Ethernet Physical Layer Transceiver, type Texas Instrument p/n DP83867CSRGZR, connected to the SERDES1 coming from SMARC® module, used to implement Gigabit Ethernet Ports #2. Another PHY transceiver, connected to SERDES0, is used to implement Gigabit Ethernet Ports #3.

For this reason, on board there is another double port RJ-45 socket CN28 type TRXCOM p/n TRJG27420AINL or equivalent, with 2kV decoupling capacitors.

In order to support SERDES interfaces used for Gigabit Ethernet Ports #2 #3, it is necessary to configure properly 1-3 position of the dual DIP switch SW17, type ADIMPEX p/n KVT04602-R, according to the table below.

SW17 position	PCIe routing selector
ON position (1-3)	SERDES0 / SERDES1
OFF position (1-3)	PCIe #C, #D to PCI-e x4 slot CN33
ON position (2-4)	PCIe #A, #B to M.2 Key E Slot CN36 (PCIe #B) and M.2 Key B Slot CN38 (PCIe #A)
OFF position (2-4)	PCIe #A, #B to PCI-e x4 slot CN33

On each connector CN27 and CN28, there are also two LEDs for each port. Left LED is bicolor (Green /Yellow) and shows 10/100 or 1000 connection: green means 100Mbps connection, yellow means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. The right LED is Green and shows ACTIVITY presence.

These interfaces are compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. They will configure automatically to work with the existing network.

Please be aware that they will work in Gigabit mode only in case that they are connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

Gigabit Ethernet interfaces Ports #0 #1 are directly manged by the SMARC® module, while Gigabit Ethernet interfaces Ports #2 #3 are managed by PHYs Transceivers on CSM-B79 carrier board interfaced to SERDES interfaces from SMARC® module. Please notice that the effective support of this kind of interfaces depends only by the SMARC® module used with the CSM-B79 carrier board, it is not a feature dependent from the carrier board itself.

Signal Description:

GBEx_MDI0+/GBEx_MDI0-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBEx_MDI1+/GBEx_MDI1-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

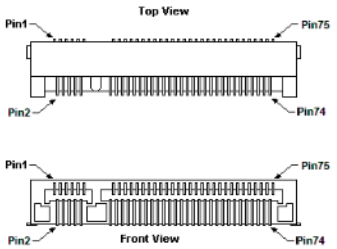
GBEx_MDI2+/GBEx_MDI2-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBEx_MDI3+/GBEx_MDI3-: Ethernet Controller #x Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

3.3.12 M.2 WLAN Key E Slot

M.2 Connectivity Slot (Socket 1 Key E type 2230) – CN36			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+3.3V_ALW
3	USB4+	4	+3.3V_ALW
5	USB4-	6	LED_1#
7	GND	8	---
9	---	10	---
11	---	12	---
13	---	14	---
15	---	16	LED_2#
17	---	18	GND
19	---	20	---
21	---	22	---
23	---	32	---
33	GND	34	---
35	PCIe_B_Tx+_M2	36	---
37	PCIe_B_Tx-_M2	38	---
39	GND	40	---
41	PCIe_B_Rx+_M2	42	---
43	PCIe_B_Rx-_M2	44	---
45	GND	46	---
47	PCIe_B_CLK+_M2	48	---
49	PCIe_B_CLK-_M2	50	---
51	GND	52	PCIe_B_RST#
53	PCIE_B_CLKREQ#	54	W_DISABLE2#_E
55	PCIe_WAKE#	56	W_DISABLE1#_E
57	GND	58	---
59	---	60	---
61	---	62	---
63	GND	64	---
65	---	66	---
67	---	68	---
69	GND	70	---
71	---	72	+3.3V_ALW
73	---	74	+3.3V_ALW
75	GND		

On CSM-B79 carrier board, to add communications functionality, it is available a dedicated M.2 Key E Slot for WLAN connectivity (WiFi/BT), which allows plugging modules with USB 2.0 and/or PCI-e x1 interface.
The connector used for the M.2 Connectivity slot is CN36, which is a standard 75 pin M.2 Key E connector, type LOTES p/n APCI0076-P001A, H=4.2mm, with the pinout shown in the table on the left.



On-board there is also a Threaded Spacer which allows the placement of M.2 Socket 1 Key E connectivity modules in 2230 size.

Please be aware that PCI-e interface will be available on this slot only if:

Used SMARC® modules offer at least 2x PCI-e x1 interfaces (since it is connected to PCI-e port #B), AND configure properly 2-4 position of the dual DIP switch SW17, according to the table at par.3.3.11

Two 2-way jumpers allow forcing the W_DISABLEX#_E signals available on this socket

JP16 position	W_DISABLE1#_E
Not Inserted	WiFi enabled
Inserted	WiFi disabled

JP15 position	W_DISABLE2#_E
Not Inserted	BT enabled
Inserted	BT disabled

Signals carried to M.2 WLAN Slot are the following:

PCIe_B_Tx+_M2 / PCIe_B_Tx-_M2: SMARC® module PCI Express lane #B, Transmitting Output Differential pair

PCIe_B_Rx+_M2 / PCIe_B_Rx-_M2: SMARC® module PCI Express lane #B, Receiving Input Differential pair

PCIe_B_CLK+_M2 / PCIe_B_CLK-_M2: SMARC® module PCI Express Reference Clock for lane #B, Differential Pair

USB4+ / USB4-: SMARC® module USB Port #4 differential pair

PCIe_WAKE#: Board's Wake Input, it must be externally driven by the M.2 WLAN module inserted in the slot when it requires waking up the system. This signal is connected directly to SMARC® module's PCIE_WAKE# signal

PCIe_B_RST#: WLAN specific reset Active Low Output Signal, directly driven by the SMARC® module to the module inserted in the M.2 WLAN slot

PCIE_B_CLKREQ#: PCI Express Clock Request Input for lane #B. This signal shall be driven low by the module inserted in the M.2 WLAN slot, in order to ensure that the PCI Express Reference Clock for lane #B is made available for this slot (i.e. PCIe_B_CLK+_M2 / PCIe_B_CLK-_M2)

W_DISABLE1_E#: this signal can be used to enable/disable the WiFi functionality of a M.2 WLAN module plugged in slot CN36. This signal is directly managed using jumper JP16 as described in the table below

W_DISABLE2_E#: this signal can be used to enable/disable the BT functionality of a M.2 WLAN module plugged in slot CN36. This signal is directly managed using jumper JP15, as described in the table below

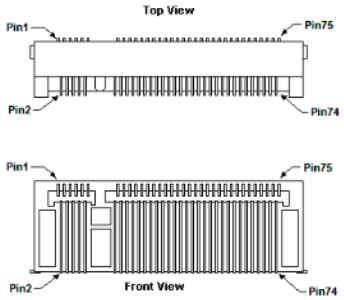
LED_1#: Indicator Output Signal driven low by the module inserted in the M.2 WLAN slot, used to activate LED diode D97 on CSM-B79 carrier board, signalling, when LED is ON, correct working of Wi-Fi functionality

LED_2#: Indicator Output Signal driven low by the module inserted in the M.2 WLAN slot, used to activate LED diode D98 on CSM-B79 carrier board, signalling, when LED is ON, correct working of BT functionality

3.3.13 M.2 WWAN Key B Slot

M.2 WWAN Slot (Socket 2 Key B type 2260/3042) – CN38			
Pin	Signal	Pin	Signal
1	---	2	+3.3V_ALW
3	GND	4	+3.3V_ALW
5	GND	6	+1.8V_ALW (2k2 pull-up)
7	USB5+	8	W_DISABLE1#_B
9	USB5-	10	M2_KEYB_LED
11	GND	20	---
21	---	22	---
23	---	24	---
25	---	26	W_DISABLE2#_B
27	GND	28	---
29	---	30	UIM_RST#
31	---	32	UIM_CLK
33	GND	34	UIM_DATA
35	---	36	UIM_PWR
37	---	38	---
39	GND	40	---
41	PCIE_A_RX-_M2	42	---
43	PCIE_A_RX+_M2	44	---
45	GND	46	---
47	PCIE_A_TX-_M2	48	---
49	PCIE_A_TX+_M2	50	PCIE_A_RST#
51	GND	52	PCIE_A_CLKREQ#
53	PCIE_A_CLK-_M2	54	PCIE_WAKE#

On CSM-B79 carrier board, to add communications functionality, it is available a dedicated M.2 Key B Slot for WWAN connectivity (Modems), which allows plugging modules with USB 2.0 and/or PCI-e x1 interface.
The connector used for the M.2 WWAN slot is CN38, which is a standard 75 pin M.2 Key B connector, type LOTES p/n APCI0087-P001A, H=8.5mm, with the pinout shown in the table on the left.



On-board there is also a Threaded Spacer which allows the placement of M.2 Socket 2 Key B WWAN modules in 2260 or 3042 size.

Please be aware that PCI-e interface will be available on this slot only if:

Used SMARC® modules offer at least 1x PCI-e x1 interface (since it is connected to PCI-e port #A), AND configure properly 2-4 position of the dual DIP switch SW17, according to the table at par.3.3.11

55	PCIE_A_CLK+_M2	56	---
57	GND	58	---
59	---	60	---
61	---	62	---
63	---	64	---
65	---	66	---
67	---	68	---
69	---	70	+3.3V_ALW
71	GND	72	+3.3V_ALW
73	GND	74	+3.3V_ALW
75	---		

Two 2-way jumpers allow forcing the W_DISABLEX#_B signals available on this socket

JP17 position	W_DISABLE1#_B
Not Inserted	WWAN enabled
Inserted	WWAN disabled

JP18 position	W_DISABLE2#_B
Not Inserted	WWAN enabled
Inserted	WWAN disabled

Signals carried to M.2 WLAN Slot are the following:

PCIe_A_Tx+_M2 / PCIe_A_Tx-_M2: SMARC® module PCI Express lane #A, Transmitting Output Differential pair

PCIe_A_Rx+_M2 / PCIe_A_Rx-_M2: SMARC® module PCI Express lane #A, Receiving Input Differential pair

PCIe_A_CLK+_M2 / PCIe_A_CLK-_M2: PCI Express Reference Clock for lane #A, directly derived by PCIE_A_REFCLK differential pair from SMARC® module using a Clock Buffer

USB5+ / USB5-: SMARC® module USB Port #5 differential pair

PCIe_WAKE#: Board's Wake Input, it must be externally driven by the M.2 WWAN module inserted in the slot when it requires waking up the system. This signal is connected directly to SMARC® module's PCIE_WAKE# signal

PCIe_A_RST#: WWAN specific reset Active Low Output Signal, directly driven by the SMARC® module to the module inserted in the M.2 WWAN slot

PCIE_A_CLKREQ#: PCI Express Clock Request Input for lane #A. This signal shall be driven low by the module inserted in the M.2 WWAN slot, in order to ensure that the PCI Express Reference Clock for lane #B is made available for this slot (i.e. PCIe_B_CLK+_M2 / PCIe_B_CLK-_M2)

W_DISABLE1_B#: this signal can be used to enable/disable the WWAN functionality of a M.2 WWAN module plugged in slot CN38. This signal is directly managed using jumper JP17 as described in the table above

W_DISABLE2_B#: this signal can be used to enable/disable the WWAN / GNSS functionality of a M.2 WWAN module plugged in slot CN38. This signal is directly managed using jumper JP18, as described in the table below

M2_KEYB_LED: Indicator Output Signal driven low by the module inserted in the M.2 WWAN slot, used to activate LED diode D116 on CSM-B79 carrier board, signalling, when LED is ON, correct working of Modem functionality

UIM_RST#: Reset signal line, sent from M.2 WWAN card to the UIM module

UIM_DATA: Bidirectional Data line between M.2 WWAN card and UIM module

UIM_CLK: Clock line, output from M.2 WWAN card to the UIM module

UIM_PWR: Power line for UIM module

3.3.14 microSIM Slot

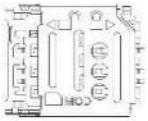
microSIM Card Slot – CN40			
Pin	Signal	Pin	Signal
1	UIM_PWR	5	GND
2	UIM_RST#	6	---
3	UIM_CLK	7	UIM_DATA
4	---	8	---

Interfaced to the M.2 WWAN slot CN38, there is a microSIM Card Slot, to be used in conjunction with M.2 Socket 2 Key B modems. Here it is possible to insert the microSIM card provided by any telecommunication operator for the connection to their network.

The socket is type MOLEX. p/n 78800-0001or equivalent, with the pinout shown in the table on the left.

For ESD protection, on all signal lines are placed clamping diodes for voltage transient suppression.

Signals related to UIM (SIM) card have already been described in previous paragraph.



3.3.15 PCI-e ports

According to SMARC® Rel. 2.1.1 specification, SMARC® modules foresee a maximum of 4 PCI-e x1 lanes, which can also be grouped (depending on the SMARC® module's chipset/processor). Four PCI-e reference clocks are also provided.

To allow the maximum flexibility, on CSM-B79 there is a dual DIP switch SW17, type ADIMPEX p/n KVT04602-R, in order to allow the routing of PCI-e root ports.

For PCI lanes #A and #B, these can be routed to M.2 Key E Slot CN36 (PCIe #B) and M.2 Key B Slot CN38 (PCIe #A) or to PCI-e x4 slot CN33, according to 2-4 position of SW17 (see table below).

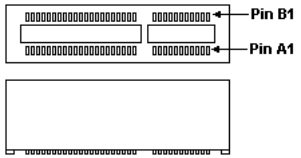
Since, according to SMARC® Rel 2.1.1 specification, PCI lanes #C and #D share the same pins on the card edge connector with the SERDES0 and SERDES1 interfaces (SERDES0/ PCIe #D and SERDES1/ PCIe #C), based on the SMARC® module's support and the needed interface, these can be routed to SERDES0 / SERDES1 (par.3.3.11) or to PCI-e x4 slot CN33, according to 1-3 position of SW17 (see table below).

SW17 position	PCIe routing selector
ON position (1-3)	SERDES0 / SERDES1
OFF position (1-3)	PCIe #C, #D to PCI-e x4 slot CN33
ON position (2-4)	PCIe #A, #B to M.2 Key E Slot CN36 (PCIe #B) and M.2 Key B Slot CN38 (PCIe #A)
OFF position (2-4)	PCIe #A, #B to PCI-e x4 slot CN33

The options for connectors used when routing PCIe lanes to M.2 Key E Slot CN36 (PCIe #B, par.3.3.12), to M.2 Key B Slot CN38 (PCIe #A, par.3.3.13) and SERDES (par.3.3.11) have been already described at reference paragraphs.

By setting both 1-3 switch and 2-4 switch in OFF position, four PCI-e lanes #A...#D coming from SMARC® card edge connector are carried to a standard PCI-e x4 card edge connector, type WINWIN p/n WPES-064AN41B22UWC or equivalent, with the pinout shown in the following table.

Please check the User Manual of the SMARC® module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.



PCI-e x 4 Slot CN33					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_CK with voltage level translator	PCIE_SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_DAT with voltage level translator	PCIE_SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation, connected directly to SMARC® module's PCIE_WAKE# signal	WAKE0#	B11	A11	PCIE_RST#_X4	Reset signal to the add-in card, derived by PCIE_A_RST# using an Ultra High Speed CMOS buffer.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIE_CLK+_X4	PCI-e reference clock lane +, for the add in card, directly derived by PCIE_A_REFCLK+ using a Clock Buffer
SMARC® module PCI-e lane Transmitter lane #A+	PCIE_A_TX+_X4	B14	A14	PCIE_CLK-_X4	PCI-e reference clock lane-, for the add in card, directly derived by PCIE_A_REFCLK- using a Clock Buffer
SMARC® module PCI-e lane Transmitter lane #A-	PCIE_A_TX-_X4	B15	A15	GND	Power Ground

Power Ground	GND	B16	A16	PCIE_A_RX+_X4	SMARC® module PCI-e lane Receiver lane #A+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot.	PRSNT2#	B17	A17	PCIE_A_RX-_X4	SMARC® module PCI-e lane Receiver lane #A-
Power Ground	GND	B18	A18	GND	Power Ground
SMARC® module PCI-e lane Transmitter lane #B+	PCIE_B_TX+_X4	B19	A19	RSVD	Not Connected
SMARC® module PCI-e lane Transmitter lane #B-	PCIE_B_TX-_X4	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_B_RX+_X4	SMARC® module PCI-e lane Receiver lane #B+
Power Ground	GND	B22	A22	PCIE_B_RX-_X4	SMARC® module PCI-e lane Receiver lane #B-
SMARC® module PCI-e lane Transmitter lane #C+	PCIE_C_TX+_X4	B23	A23	GND	Power Ground
SMARC® module PCI-e lane Transmitter lane #C-	PCIE_C_TX-_X4	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_C_RX+_X4	SMARC® module PCI-e lane Receiver lane #C+
Power Ground	GND	B26	A26	PCIE_C_RX-_X4	SMARC® module PCI-e lane Receiver lane #C-
SMARC® module PCI-e lane Transmitter lane #D+	PCIE_D_TX+_X4	B27	A27	GND	Power Ground
SMARC® module PCI-e lane Transmitter lane #D-	PCIE_D_TX-_X4	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_D_RX+_X4	SMARC® module PCI-e lane Receiver lane #D+
Not Connected	RSVD	B30	A30	PCIE_D_RX-_X4	SMARC® module PCI-e lane Receiver lane #D-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

3.3.16 USB Connectors

According to SMARC® Rel. 2.1.1 specification, SMARC® modules can have up to 2x USB 3.0 ports + 4x USB 2.0 only ports or 6x USB2.0 ports.

USB#0 and USB#3 ports can also have, optionally, the OTG / client capability.

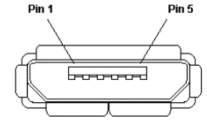
Considering these possibilities, CSM-B79 carrier board offers:

- USB 2.0 port #0, which could be able to manage OTG functionality, is carried to USB micro-AB connector CN30 (described below);
- USB 2.0 port #1 is carried to standard USB 2.0 Type-A Slot CN50 (described below);
- USB 3.0 port #2 is carried to standard USB 3.0 Type-A slot CN72 (described below);
- USB 3.1 port #3, which could be able to manage OTG functionality, is carried to USB Type-C connector CN9 (described below);
- USB 2.0 port #4 is available on M.2 Key E slot CN36 (par.3.3.12);
- USB 2.0 port #5 is available on M.2 Key B slot CN38 (par.3.3.13).

For all USB ports described below, common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

Micro-AB USB Connector – CN30	
Pin	**Signal**
1	+5V_USB0_VBUS
2	USB0_OTG-
3	USB0_OTG+
4	USB0_OTG_ID
5	GND



According to SMARC® Rel. 2.1.1 specification, USB Port #0, coming out from SMARC® module, could support OTG functionalities (it depends on the functionalities offered by the SMARC® module used, however).

For this reason, this port is carried out through a standard micro-AB connector, type Hirose p/n ZX62-AB 5PA(11), described in the table on the left.

Depending on the support offered by the SMARC® module, and from the needed use of the system, it is necessary to connect micro-A or micro-B USB cables to connector CN30.

A micro-A USB cable has to be used when the system has to work in Host mode. In this case, +5V_USB0_VBUS is a power output of CSM-B79 Carrier Board for the connected device.

When a micro-B USB cable is used, its USB0_OTG_ID pin is floating; this way, the board acknowledges that it must configure itself to work as a Client. In this case, +5V_USB0_VBUS is an input power for the carrier board from the external Host.
Signal description of this port:

USB0_OTG+/USB0_OTG-: SMARC® Module USB Port #0 differential pair

+5V_USB0_VBUS: USB voltage rail. It is an input for USB port working in Client mode, an output for Host mode and in this case the power rail is derived by +5V_ALW with a dedicated 600 mA current-limited power switch IC

USB_ID: Client/Host identification signal. This signal is high when the USB port works in client mode, is low when works in Host mode.

USB 2.0 type A receptacle – CN50	
Pin	**Signal**
1	$+5V_{USB1}$
2	USB1-
3	USB1+
4	GND

USB Port #1, coming out from SMARC® module is directly carried to a standard Type-A receptacle, type TE Connectivity p/n 1903814-1.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 devices using Standard-A USB 2.0 cables.

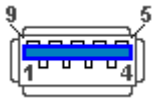
Signal description of this port:

USB1+ / USB1- : SMARC® Module USB Port #1 differential pair

$+5V_{USB1}$ is derived from +5V_ALW power rail with a dedicated 600 mA current-limited power switch IC.

USB 3.0 type A receptacle – CN72			
Pin	**Signal**	**Pin**	**Signal**
1	$+5V_{USB2}$	5	USB2_SSRX-
2	USB2-	6	USB2_SSRX+
3	USB2+0+	7	GND
4	GND	8	USB2_SSTX-
		9	USB2_SSTX+

USB Port #2, coming out from SMARC® module, is an USB 3.0 port and consists of a USB 2.0 port and a set of unidirectional SuperSpeed differential pair signals.



The connector used is a standard type-A USB 3.0 receptacle.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

Signal description of this port:

USB2+ / USB2- : SMARC® Module USB Port #2 differential pair

USB2_SSRX- / USB2_SSRX+ : SMARC® Module USB Super Speed Port #2 receive signal differential pair

USB2_SSTX- / USB2_SSTX+ : SMARC® Module USB Super Speed Port #2 transmit signal differential pair

$+5V_{USB2}$ is derived from +5V_ALW power rail with a dedicated 1A current-limited power switch IC.

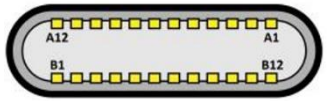
! Please be aware that USB 3.0 connectivity can be obtained only in case that it is supported by the SMARC® Module plugged onto the Carrier Board. In case the SMARC® Module used doesn't offer USB 3.0 ports, it will be always possible to use USB 2.0 ports, simply by plugging an USB 2.0 cable. Avoid using USB 3.0 cables if the SMARC® Module used doesn't offer such an interface.

USB 3.1 Type-C Socket – CN9			
Pin	**Signal**	**Pin**	**Signal**
A1	GND	B12	GND
A2	USBC_Tx1+	B11	USB_Rx1+
A3	USBC_Tx1-	B10	USBC_Rx1-
A4	VBUS_C	B9	VBUS_C
A5	USBC_CC1	B8	---
A6	USB_D1+	B7	USB_D2-
A7	USB_D1-	B6	USB_D2+
A8	---	B5	USBC_CC2
A9	VBUS_C	B4	VBUS_C
A10	USBC_Rx2-	B3	USBC_Tx2-
A11	USBC_Rx2+	B2	USBC_Tx2+
A12	GND	B1	GND

USB Port #3, coming out from SMARC® module, could support OTG functionalities (it depends on the functionalities offered by the SMARC® module used, however).

For this reason, this port is carried out through a standard type-C Socket, type Amphenol p/n 12401610E4#2A, described in the table on the left.

This USB Type-C port CN9 has Power Delivery functionality, made possible by the source controller on CSM-B79 carrier board with integrated 1.5A @5V USB power switch. This IC controller does monitor USBC_CC1 / USBC_CC2 to detect when a USB sink is attached and applies power to VBUS_C with the defined current sourcing capability (1.5A @5V).



USB Type-C supports USB 2.0, USB 3.0 and USB 3.1 Gen 2 standards. This support, however, is strictly related to SMARC® module features on USB Port #3, so it's recommended to refer to SMARC® module user manual intended to be used.

In addition, USB Type-C is a flippable connector, meaning that this interface is designed in a way that the plug can be flipped relative to the receptacle. The redundancy for the signal on Row A and B is included only to provide a flippable connector.

The Power Delivery controller on CSM-B79 carrier board by reading channel configurations pins USBC_CC1 and USBC_CC2 will drive the multiplexer on board to correctly re-route the data on the employed differential pairs through the connector.

Signal description of this port:

USBC_TxX+ / USBC_TxX- : SMARC® Module USB Super Speed Port #3 transmit signal differential pair

USBC_RxX+ / USBC_RxX- : SMARC® Module USB Super Speed Port #3 receive signal differential pair

USB_DX+ / USB_DX- : SMARC® Module USB Port #3 differential pair

USBC_CC1 / USBC_CC2: Configuration Channels, used to detect cable attachment and removal, receptacle/plug orientation detection, and current advertisement. Signals directly manged by the USB Type-C source controller on CSM-B79 carrier board

VBUS_C: Power bus, current limited to 1.5A @5V by power switch controller.

USB Enable / Overcurrent Internal Header – CN80			
Pin	Signal	Pin	Signal
1	GND	2	USB0_EN_OC#
3	GND	4	USB1_EN_OC#
5	GND	6	USB2_EN_OC#
7	GND	8	USB3_EN_OC#

For debugging purposes, onCSM-B79 carrier board it is also available an 8-pin connector, type Adimpex p/n LE008208-R or equivalent, for the connection of USBx_EN_OC# signals.

USB0_EN_OC#: USB over-current sense signal for USB Port #0. Active Low Input Signal, driven by current-limited power switch IC for +5V_USB0_VBUS and manged by SMARC® module

USB1_EN_OC#: USB over-current sense signal for USB Port #1. Active Low Input Signal, driven by current-limited power switch IC for +$5V_{USB1}$ and manged by SMARC® module

USB2_EN_OC#: USB over-current sense signal for USB Port #2. Active Low Input Signal, driven by current-limited power switch IC for +$5V_{USB2}$ and manged by SMARC® module

USB3_EN_OC#: USB over-current sense signal for USB Port #3. Active Low Input Signal, driven by current-limited power switch IC for VBUS_C and manged by SMARC® module

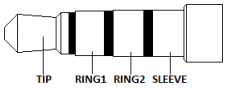
3.3.17 Audio Connectors

According to SMARC® Rel. 2.1.1 specification, SMARC® modules include an I2S0 dedicated interface and an I2S2 / HD Audio shared interface.

For this reason, on the CSM-B79 carrier board there are both an I2S Audio Codec (TI p/n TLV320AIC3204), connected to I2S0 interface, and an HD Audio codec (Cirrus Logic CS4207), connected to I2S2 / HD Audio interface.

TRRS Audio headset jack- CN41	
Pin	**Signal**
TIP	Line Out Left Channel
RING1	Line Out Right Channel
RING2	Mic_IN_p or Mic_IN_n signal
SLEEVE	Mic_IN_n or Mic_IN_p signal

Both these codecs are connected to a single TRRS Combo Audio Socket, i.e. a single socket which offer both stereo Line Out and Mic In functionalities.

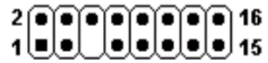


Such TRRS Combo Audio socket can be used with any 4-poles 3.5mm diameter audio jack, with pinout compatible with the most recent Headsets, shown in the table on the left.

The TRSS Audio Headset jack can support indifferently Headset with Mic In_p signal on RING2 position and Mic In_n signal on SLEEVE position or viceversa.

Since only one Codec at a time can manage this connector, it is necessary to switch the connection from the TRRS jack to the proper codec by using the dedicated dual DIP switch SW16, described below.

I2S Audio Header – CN81			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GP_I2C_DAT_3V3
3	+3V3_RUN	4	GP_I2C_CLK_3V3
		6	---
7	+12V_RUN	8	I2S2_SDIN_3.3V
9	+3V3_RUN	10	I2S2_SDOUT_3.3V
11	GND	12	I2S2_LRCLK_3.3V
13	+3V3_RUN	14	I2S2_RST#_3.3V
15	GND	16	I2S2_CLK_3.3V



If the SMARC® module has I2S audio support, then the I2S Audio Codec on-board will manage the I2S0 interface from card edge connector for the TRSS Audio Jack CN41. In addition, if the SMARC® module has a secondary I2S audio support, the I2S2 interface from card edge connector is made available, without further elaborations, on a dedicated I2S Audio header CN81, which is a 15-pin pin header, p2.54 mm h= 6mm, type NELTRON p/n 2213S-16G-E5 or equivalent, with the pinout shown in the table on the left. This connector can be used to connect external audio codec modules, specific for the kind of interface offered by the SMARC® module used.

If the SMARC® module has HD audio support, then the HD Audio Codec on-board will manage the HDA interface from card edge connector for the TRSS Audio Jack CN41. In this case, only the support on TRSS Audio Jack CN41 will be available, since I2S2 / HD Audio share the same pins from card edge connector.

To proper setting, refer to I2S / HDA Codec selector DIP switch SW16 below.

SW16 Switch	ON Position	OFF Position
1 – 3	---	---
2 – 4	HDA codec to audio jack CN41	I2S0 codec to audio jack CN41 I2S2 interface to pin header CN81

Signal description of I2S Audio Header CN81:

I2S2_SDIN_3.3V: I2S Digital Audio Input Signal, derived from SMARC® Module I2S2_SDIN. +3V3_RUN electrical level

I2S2_SDOUT_3.3V: I2S Digital Audio Output Signal, derived from SMARC® Module I2S2_SDOUT. +3V3_RUN electrical level

I2S2_LRCLK_3.3V: I2S Left & Right Synchronization Clock, derived from SMARC® Module I2S2_LRCK. +3V3_RUN electrical level

I2S2_RST#_3.3V: I2S Digital Audio Reset Output, active low signal. This signal is routed through 3-way jumper CN82, so the signal is derived by HDA_RST# (1-2 position) or by RESET_OUT# (2-3 position, default)

I2S2_CLK_3.3V: I2S Digital Audio Clock Signal, derived from SMARC® Module I2S2_CK. +3V3_RUN electrical level

GP_I2C_DAT_3V3: General Purpose I2C I/O Data Signal, derived from SMARC® I2C_GP_DAT with a set of back to back FETs to voltage translate. +3.3V_RUN electrical level with 2k2Ω pull up resistor. Also carried to Feature Header CN45 (par.3.3.26)

GP_I2C_CLK_3V3: General Purpose I2C Clock Output Signal, derived from SMARC® I2C_GP_CK with a set of back to back FETs to voltage translate. +3.3V_RUN electrical level with 2k2Ω pull up resistor. Also carried to Feature Header CN45 (par.3.3.26)

3.3.18 COM Port Header

Dual RS-232/RS-422/RS-485 pin header- CN25			
Pin	**Signal RS-232 mode**	**Signal RS-422 mode**	**Signal RS-485 mode**
1	COM0_RxD	COM0_Rx+	
2	COM2_RxD	COM2_Rx+	
3	COM0_TxD	COM0_Tx-	COM0_Data-
4	COM2_TxD	COM2_Tx-	COM2_Data-
5	GND	GND	GND
7	COM0_RTS#	COM0_Tx+	COM0_Data+
8	COM2_RTS#	COM2_Tx+	COM2_Data+
9	COM0_CTS#	COM0_Rx-	
10	COM2_CTS#	COM2_Rx-	

According to SMARC® Rel. 2.1.1 specification, SMARC® modules foresee a maximum of four asynchronous serial ports on the card edge connector, two of them complete of Flow control RTS# and CTS# signals (SER#0 and SER#2), the other with only Tx and Rx signals (SER #1 and SER #3).

SER#0 and SER#2 ports are managed through multistandard (RS-232/RS-422/RS-485) transceivers, and the output is available on an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

The selection of the kind of interface (RS-232, RS-422 or RS-485) can be made by using 3-way jumpers CN23 and CN24.

CN23 position	COM Port #0 mode
1-2	RS-422
2-3	RS-232
Not inserted	RS-485

CN24 position	COM Port #2 mode
1-2	RS-422
2-3	RS-232
Not inserted	RS-485

Please be aware that for proper RS-485 working, the RTS# signals must be used as a handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-458 port is in transmitting mode.

The port referenced as COM0 is the transceivered signal from the SMARC® module SER#0 interface, while the port referenced as COM2 is the transceivered signal from the SMARC® module SER#2 interface.

Signals Description:

COM0_RxD/COM2_RxD: COM port #0 / #2 RS-232 Receive data,

COM0_TxD/COM2_TxD: COM port #0 / #2 RS-232 Transmit data

COM0_RTS#/COM2_RTS#: COM port #0 / #2 RS-232 Request to Send handshaking signal

COM0_CTS#/COM2_CTS#: COM port #0 / #2 RS-232 Clear To Send handshaking signal

COM0_Rx+/COM0_Rx-: COM port #0 RS-422 Receive differential pair

COM0_Tx+/COM0_Tx-: COM port #0 RS-422 Transmit differential pair

COM2_Rx+/COM2_Rx-: COM port #2 Full Duplex RS-485 (RS-422) Receive differential pair

COM2_Tx+/COM2_Tx-: COM port #2 Full Duplex RS-485 (RS-422) Transmit differential pair

COM0_Data+/COM0_Data-: COM Port #0 Half Duplex RS-485 Differential Pair

COM2_Data+/COM2_Data-: COM Port #2 Half Duplex RS-485 Differential Pair

Other two 3-way jumpers, CN63 and CN64, can be used to place 120Ohm terminations between the differential pairs of COM0 and COM2 when working in RS-422/RS-485 modes.

CN63 position	COM Port #0 termination
1-2	120Ohm on Data differential pairs (RS-485 mode)
2-3	No terminations
Not inserted	120Ω on Tx and Rx differential pairs (RS-422 mode)

CN64 position	COM Port #2 termination
1-2	120Ohm on Data differential pairs (RS-485 mode)
2-3	No terminations
Not inserted	120Ω on Tx and Rx differential pairs (RS-422 mode)

SER#1 serial port, instead, is carried to the feature connector (see par.3.3.26) or used to manage the micro-B USB connector for Debug (see par.3.3.20), depending on the SER#1 redirector dual DIP switch SW7 (see par.3.3.20).

SER#3 serial port, instead, is carried directly from card edge connector to the feature connector (see par.3.3.26)

3.3.19 CAN ports

According to SMARC® Rel. 2.1.1 specification, SMARC® modules foresee two CAN bus interfaces.The CSM-B79 carrier board include two dedicated transceivers, corresponding CAN output interfaces are available on two dedicated 3-pin PCB terminal blocks, type Phoenix Contact P/N MKDSFW 1,5/ 3-3,5 – 1868131 or equivalent, particluar suited for this kind of application.

CAN Port #0 Connector – CN65	
Pin	**Signal**
1	CAN0_H
2	GND
3	CAN0_L

CAN Port #1 Connector – CN66	
Pin	**Signal**
1	CAN1_H
2	GND
3	CAN1_L

Signals Description:

CANx_H: High-Level CAN bus line

CANx_L: Low-Level CAN bus line

JP12 position	CAN #0 120Ohm termination
Not Inserted	No termination
Inserted	Termination placed

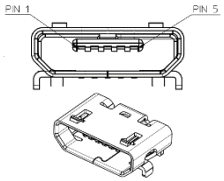
JP13 position	CAN #1 120Ohm termination
Not Inserted	No termination
Inserted	Termination placed

For each interface, by using a 2-way jumper it is possible to insert a 120Ω termination between CANx_H and CANx_L lines

3.3.20 USB Debug Connector

For Debug Purposes, it is present an USB-to-Serial Bridge, connected to SMARC®'s UART#1 (SER#1, also available on feature header). External interface is available on an USB micro-B connector, CN73, type Molex p/n 105017000, with standard pinout for USB 2.0 device connections.

Since SER#1 port can also be connected to the feature header described at par.3.3.26, an on-board dual DIP switch SW7 allows selecting if SER#1 port is used to manage the USB Debug Port or is redirected to the feature header connector.



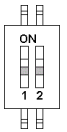
Debug USB micro-B – CN73	
Pin	**Signal**
1	+5V_VBUS
2	USB_DBG-
3	USB_DBG+
4	--
5	GND

Signal description:

USB_DBG+ / USB_DBG-: Debug USB Port differential pair

+5V_VBUS: USB voltage rail

SW7 Switch	ON Position	OFF Position
1 – 3	SER#1 on USB Debug connector CN73	SER#1 on Feature Header CN45
2 – 4	---	---

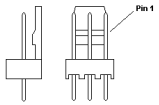


3.3.21 FAN Connector

3-Wire FAN Connector – CN56	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

CN55 position	FAN_PWR Level
1-2	12V_RUN
2-3	5V_RUN

On CSM-B79 carrier board it is available a 3-pin connector, type MOLEX p/n 22-27-2031 or equivalent, for the connection of tachometric FANs.



Mating connector: MOLEX 22-01-2035 receptacle with MOLEX 2759 or 4809 KK® crimp terminals.

FAN_POWER: FAN Power signal, PWM controlled for FAN speed by using GPIO5/PWM_OUT signal coming from SMARC® module. Furthermore, the voltage level is selectable to be at 12V_RUN or 5V_RUN. Selection must be done through a 3-way jumper, CN55.

FAN_TACHO_IN: FAN Tachometer Input signal for SMARC® module

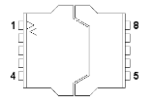
3.3.22 SPI interface

SPI Flash Socket – CN43			
Pin	**Signal**	**Pin**	**Signal**
1	SPI0_CS1#	8	1.8V_ALW
2	SPI0_DIN	7	10kΩ pull-up 1.8V_ALW
3	10kΩ pull-up 1.8V_ALW	6	SPI0_CK
4	GND	5	SPI0_DOUT

SPI header – CN91			
Pin	**Signal**	**Pin**	**Signal**
1	SPI0_CS0#	2	1.8V_ALW
3	SPI0_DIN	4	SPI0_CS0#
5	SPI0_WP#	6	SPI0_CK
7	GND	8	SPI0_DOUT

According to SMARC® Rel. 2.1.1 specification, SMARC® modules foresee up two Serial Peripheral Interfaces, coming out from SMARC® card edge connector, for the connection of external SPI devices, included boot devices.

The first one is SPI0, while the second one, SPI1, does share the same pins with QSPI or eSPI interface.



The SPI0 interface available on SMARC® card edge connector is available both on a SPI Flash Socket CN43, type LOTES p/n ACA-SPI-004-K01 or equivalent, and on a dual-row 8-pin SMT male pin-header CN91, p. 1.27mm, type TOWNES P1035-2*04MGF-084-A or equivalent, with pinout shown in the table on the left.

Signal description:

SPI0_DIN: SMARC® module SPI0 Master input / Slave output, also referred to as MISO

SPI0_DOUT: SMARC® module SPI0 Master output / Slave input, also referred to as MOSI

SPI0_CK: SMARC® module SPI0 Clock

SPI0_CS0#: SMARC® module SPI0 Master Chip Select 0, active low output signal

SPI0_CS1#: SMARC® module SPI0 Master Chip Select 1, active low output signal

SPI0_WP#: this signal is tied, through a 10kΩ resistor, to 1.8V_ALW. This means that when the external attached SPI device is powered, the protection from writing is automatically removed.

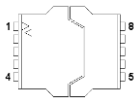
SPI_HOLD#: this signal too is tied, through a 10kΩ resistor, to 1.8V_ALW signal. This means that when the external attached SPI device is powered, the Hold condition of serial communication is automatically removed.

If SMARC® module selected to work with CSM-B79 Carrier Board does not handle SPI0_CS1# signal, do not connect any SPI flash boot device in CN43.

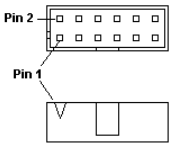
3.3.23 eSPI interface

According to SMARC® Rel. 2.1.1 specification, SMARC® modules second SPI (SPI1) can be implemented as QuadSPI (QSPI) or enhanced SPI (eSPI). In case selected SMARC® module has the support for eSPI, this interface is available both on an eSPI Flash Socket CN69, type LOTES p/n ACA-SPI-004-K01 or equivalent, and on an internal 14-pin dual row p.2.54 mm header CN44 (type MOLEX p/n 70246-1404 or equivalent), with the following pinout:

eSPI Flash Socket – CN69			
Pin	Signal	Pin	Signal
1	ESPI_CS0#	8	1.8V_ALW
2	ESPI_IO1	7	---
3	ESPI_IO2	6	ESPI_CK
4	GND	5	ESPI_IO0



eSPI Header – CN44			
Pin	Signal	Pin	Signal
1	GND	2	ESPI_CS0#
3	ESPI_CK	4	ESPI_IO3
5	---	6	ESPI_IO2
7	ESPI_RESET#	8	ESPI_IO1
9	3.3V_RUN	10	ESPI_IO0
11	ESPI_ALERT1#	12	ESPI_CS1#
13	3.3V_ALW	14	ESPI_ALERT0#



Signal description

ESPI_CK: SMARC® module eSPI Master Clock Output

ESPI_IO_[0:3]: SMARC® module eSPI Master Data Input / Outputs. These are bi-directional input/output signals used to transfer data between master and slaves.

ESPI_CS0#: SMARC® module eSPI Master Chip Select #0. Active low output signal.

ESPI_CS1#: SMARC® module eSPI Master Chip Select #1. Active low output signal.

ESPI_RESET#: SMARC® module eSPI Reset Signal for both master and slaves devices. Active low output signal.

ESPI_ALERT0#: SMARC® module eSPI signal used by eSPI slave to request service from the eSPI master. Active low input signal.

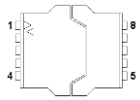
ESPI_ALERT1#: SMARC® module eSPI signal used by eSPI slave to request service from the eSPI master. Active low input signal.

3.3.24 I2C EEPROM Socket

I2C EEPROM Flash Socket – CN71			
Pin	**Signal**	**Pin**	**Signal**
1	10kΩ pull-up 1.8V_DSW	8	1.8V_DSW
2	10kΩ pull-up 1.8V_DSW	7	I2C_Write Protect
3	10kΩ pull-up 1.8V_DSW	6	I2C_PM_CK
4	GND	5	I2C_PM_DAT

According to SMARC® Rel. 2.1.1 specification, SMARC® modules have a dedicated I2C bus (I2C_PM) from card edge connector dedicated to power management functions, such as Smart Battery System Management. On the CSM-B79 carrier board, this I2C bus is voltage level translated from SMARC® modules before being used by these slave devices.

In addition, on CSM-B79 carrier board, the I2C_PM bus is directly carried, at 1.8V electrical level, to an 8-pin Flash Socket, type LOTES p/n ASPI0001-P001A, for the mounting of I2C EEPROMs in SO-8 format, with the pinout on left table.



JP14	I2C_Write Protect
Not Inserted	Writings allowed
Inserted	Writings not allowed

Signal description:

I2C_PM_DAT: SMARC® module Power management I2C bus DATA

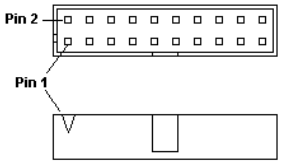
I2C_PM_CK: SMARC® module Power management I2C bus CLK

There is a dedicated 2-way jumper, JP14, for driving signal I2C_Write Protect, allowing protecting this Flash EEPROM from writings.

3.3.25 JTAG Connector

JTAG Connector – CN70			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_ALW	2	---
3	JTAG_TRST# (P73)	4	GND
5	JTAG_TDI (S45)	6	GND
7	JTAG_TMS (P77)	8	GND
9	JTAG_TCK (P78)	10	GND
11	10kΩ pull-down to GND	12	GND
13	JTAG_TDO (S46)	14	GND
15	JTAG_RST# (P72)	16	GND
17	---	18	GND
19	---	20	GND

On CSM-B79 carrier board, for Debug Purposes, it is also available a MOLEX p/n 70246-2004 or equivalent connector, with the pinout shown in the left table. Mapping to SMARC® module card edge connector pins is also provided within brackets.



Mating connector: MOLEX p/n 22-25-2202 with 70058 series female crimp terminals.

For signal description, do refer directly to SMARC® module user manual intended to be used with CSM-B79 carrier board.

JTAG_TDI and JTAG_TDO signals share the same pins on the card edge connector with MDIO signals used to manage the PHYs for SERDES interfaces. They are available on this connector only in case they are supported by the SMARC® module; in this case, to use them as a JTAG, set SW17 switch 1-3 in OFF position (par.3.3.15).

JTAG_TMS signal shares the same pin on the card edge connector with PCIE_B_CLKREQ# signal request for M.2 WLAN Key E Slot, while JTAG_TCK shares the same pin on the card edge connector with PCIE_A_CLKREQ# They are available on this connector only in case they are supported by the SMARC® module; in this case, to use them as a JTAG, set SW14 switch 2-4 in ON position and / or 3-way jumper CN78 in 2-3 position.

3.3.26 Feature Header

Feature header – CN45			
Pin	**Signal**	**Pin**	**Signal**
1	+5V_RUN (with 750mA resettable fuse)	2	+5V_ALW (with 750mA resettable fuse)
3	330Ohm Pull-up to 5V_RUN	4	SATA_ACT#
5	GP_I2C_DAT_3V3	6	SMB_CLK_BAT
7	GP_I2C_CLK_3V3	8	SMB_DAT_BAT
9	SER1_TX	10	GND
11	SER1_RX	12	+3V3_RUN (with 750mA resettable fuse)
13	CHARGING#	14	+3V3_ALW (with 750mA resettable fuse)
15	SUS_S3#_3V3	16	+3V3_DSW (with 750mA resettable fuse)
17	GND	18	GND
19	CHARGER_PRSNT#	20	SMB_ALERT#
21	---	22	SUS_S5#_3.3V_A
23	GBE1_SDP	24	---
25	---	26	SUS_S5#_3.3V_A
27	WDT_TIME_OUT#	28	RESET_OUT#
29	TEST#	30	LID#
31	BATLOW#	32	SER3_TX
33	GBE0_SDP	34	SER3_RX
35	SLEEP#	36	RESET_IN#
37	GND	38	GND
39	POWER_BTN#	40	VIN_PWR_BAD#

For further expandability of the system, on CSM-B79 carrier board, are carried others signals available from SMARC® cad edge connector.

For this purpose, it is available a dual row 40-pin p 2.54 mm pin header, type ADIMPEX p/n LE008240-R.

Signal description:

GP_I2C_DAT_3V3: General Purpose I2C I/O Data Signal, derived from SMARC® I2C_GP_DAT with a set of back to back FETs to voltage translate. +3.3V_RUN electrical level with 2k2Ω pull up resistor. Also carried to I2S Audio Header CN81 (par.3.3.17)

GP_I2C_CLK_3V3: General Purpose I2C Clock Output Signal, derived from SMARC® I2C_GP_CK with a set of back to back FETs to voltage translate. +3.3V_RUN electrical level with 2k2Ω pull up resistor. Also carried to I2S Audio Header CN81 (par.3.3.17)

SER1_TX / SER1_RX: SMARC® module SER#1 Asynchronous Serial Data pairs, routing to this header is driven by dual DIP switch SW7 (par.) that must set 1-3 switch in OFF position

SER3_TX / SER3_RX: SMARC® module SER#3 Asynchronous Serial Data pairs

SUS_S3#_3V3: Signal indicating the system is in Suspend to RAM (S3) state. Active Low Output Signal with a 10kΩ pull down resistor, driven by SMARC® module CARRIER_STBY#

SUS_S5#_3.3V_A: Signal indicating the system is in Soft Off (S5) state. Active Low Output Signal, driven by SMARC® module CARRIER_PWR_ON

CHARGING#: SMARC® module Battery Charging Input Signal, active low

CHARGER_PRSNT#: SMARC® module Battery Charger Present Input Signal, active low

BATLOW#: SMARC® module Battery Low indication signal, active low

GBE0_SDP: SMARC® module IEEE 1588 Trigger Signal for Hardware Implementation of PTP (Precision Time Protocol)

GBE1_SDP: SMARC® module IEEE 1588 Trigger Signal for Hardware

Implementation of PTP (Precision Time Protocol)

WDT_TIME_OUT#: SMARC® module Watchdog Timer Signal. Active Low Output Signal, it reports that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

TEST#: SMARC® module Active Low Input Signal to invoke specific test function(s). Please refer to specific SMARC® module user manual intended to be used to have details on what specific test functions this signal will enable. This signal can be also driven by 2-4 position of dual DIP switch SW14. To force this signal to be always activated, set SW14 switch 2-4 in ON position, otherwise set in OFF position for normal operation (default)

SLEEP#: SMARC® module Sleep Button event signal input, used to bring the module in sleep state or wake it up again. Active Low Input signal. This signal can be directly driven by SW5 pushbutton (par.3.3.30) and upon its pressure, the pulse of this signal will let the transition of the module from Working to Sleep status, or vice versa

POWER_BTN#: Power Button event signal input, used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Active low input signal. This signal can be directly driven by SW3 pushbutton (par.3.3.30) and upon its pressure, the pulse of this signal will let the switched voltage rails turn on or off

SATA_ACT#: SMARC® module Serial ATA Activity Indicator. Active low output signal. This signal also drives the activation of diode LED D99, signalling working condition when external storage device is attached (par.3.3.8)

SMB_CLK_BAT: Smart Battery System Management bus bidirectional clock line, +3.3V_DSW electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_CK signal

SMB_DAT_BAT: Smart Battery System Management bus bidirectional data line, +3.3V_DSW electrical level with 2.2kΩ pull up resistor, derived by I2C_PM_DAT signal

SMB_ALERT#: Smart Battery System Management bus Alert Interrupt Signal. Active low input signal, +3.3V_DSW electrical level with 7.5kΩ pull up resistor, derived by SMARC® module SMB_ALERT# signal

RESET_OUT#: SMARC® module general purpose reset, active low output signal

RESET_IN#: SMARC® module general purpose reset, active low input signal. This signal can be directly driven by SW4 pushbutton (par.3.3.30) and upon its pressure, the pulse of this signal will let the SMARC® module to perform a reset. There is jumper JP20 not mounted by default associated to this signal, used to prevent SMARC® module from booting when runtime voltages are not good.

LID#: SMARC® module Lid open/close indication signal. Active low input signal. This signal can be directly driven by SW15 pushbutton (par.3.3.30) and upon its pressure, the pulse of this signal will indicate the closure of an external lid (which module may use to initiate a sleep state). In addition, this signal can be also driven by 1-3 position of dual DIP switch SW14. To force LID button simulation, set SW14 switch 1-3 in ON position, otherwise set in OFF position for normal operation (default)

VIN_PWR_BAD#: SMARC® module Power bad indication signal. Active low input signal. To have this indication signal enabled, the 3-way jumper CN62 must be set in 2-3 position. Otherwise, when set in 1-2 position (default) this control signal is disabled.

3.3.27 GPIO / FuSa Header

GPIO / FuSa Header – CN92		
Pin	**Signal**	**FuSa Interface**
1	+5V_ALW (with 1.5 resettable fuse)	
2	+12V_RUN (with 1.5 resettable fuse)	
3	GND	
4	GND	
5	GPIO0 / CAM0_PWR#	FUSA_OKNOK0
6	GPIO1 / CAM1_PWR#	FUSA_OKNOK1
7	GPIO2 / CAM0_RST#	FUSA_ALERT#
8	GPIO3 / CAM1_RST#	FUSA_SPIS_CS#
9	GPIO4 / HDA_RST#	FUSA_SPIS_SCLK
10	GPIO5 / PWM_OUT	FUSA_SPIS_MISO
11	GPIO6 / TACHIN	FUSA_SPIS_MOSI
12	RSVD3	FUSA_CHXPMICEN_IN
13	GPIO7	FUSA_CHXPMIC_EN
14	GPIO8	FUSA_CHXRLYSWITCH
15	GPIO9	FUSA_CHXOKNOK0
16	GPIO10	FUSA_CHXOKNOK1
17	GPIO11	FUSA_SPIM_CS#
18	GPIO12	FUSA_SPIM_SCLK
19	GPIO13	FUSA_SPIM_MISO
20	JTAG_RST# (P72)	FUSA_SPIM_MOSI
21	I2C_CAM1_CLK	FUSA_PROCHOT
22	JTAG_TRST# (P73)	FUSA_THERMTRIP
23	---	

According to SMARC® Rel 2.1.1 specification, SMARC® modules foresee up to fourteen general purpose I/O pins at 1.8V electrical level: GPIO0 to GPIO13.

Each of these can be configured as an input or output pin.

GPIO7 to GPIO13 are dedicated GPIOs, while the other seven GPIOs are multiplexed pins supporting functions like Camera Power Enable, Camera Reset, Tachometer input, PWM output etc. All these GPIOs, together with others signals from card edge connector, are made available to a dual row, 28 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008228-R, with the pinout shown in the table on the left.

This connector can be also used to provide functional safety functions for FuSa applications through signals listed in left table. Please be aware that FuSa functionality can be obtained only in case that it is supported by the SMARC® modules used with CSM-B79 carrier board. Please refer to specific SMARC® module user manual for a signal description related to this section (FuSa interface).

Signal description:

GPIO0 / CAM0_PWR#: SMARC® module GPIO0. This signal shares the same pin from card edge connector with CAM0_PWR# (par.3.3.7)

GPIO1 / CAM1_PWR#: SMARC® module GPIO1. This signal shares the same pin from card edge connector with CAM1_PWR# (par.3.3.7)

GPIO2 / CAM0_RST#: SMARC® module GPIO2. This signal shares the same pin from card edge connector with CAM0_RST# (par.3.3.7)

GPIO3 / CAM1_RST#: SMARC® module GPIO3. This signal shares the same pin from card edge connector with CAM1_RST# (par.3.3.7)

GPIO4 / HDA_RST#: SMARC® module GPIO4. This signal shares the same pin from card edge connector with HDA_RST# (par.3.3.17)

GPIO5 / PWM_OUT: SMARC® module GPIO5. This signal shares the same pin from card edge connector with PWM_OUT (par.3.3.21)

24	---	
25	I2C_CAM1_DAT	FUSA_POWERFAIL#
26	RESET_IN#	
27	---	
28	POWER_BTN#	

GPIO6 / TACHIN: SMARC® module GPIO6. This signal shares the same pin from card edge connector with TACHIN (par.3.3.21)

GPIO[7..13]: SMARC® module General Purpose I/O signals

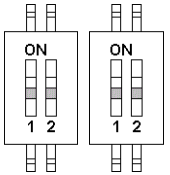
I2C_CAM1_CLK: I2C Bus clock line for MIPI CSI1 data support link. This signal is also carried to CSI Camera Connector CN39 (par.3.3.7)

I2C_CAM1_DAT: I2C Bus data line for MIPI CSI1 data support link. This signal is also carried to CSI Camera Connector CN39 (par.3.3.7)

3.3.28 Boot Select switches

On CSM-B79 carrier board there is a dual DIP switch array, made by SW12 and SW13, that manages properly the BOOT_SEL[0-2]# and FORCE_RECOV# signals, according to SMARC® Boot select table:

SW13-1 BOOT_SEL2#	SW12-2 BOOT_SEL1#	SW12-1 BOOT_SEL0#	BOOT Source
ON	ON	ON	Carrier SATA
ON	ON	OFF	Carrier SD card
ON	OFF	ON	Carrier eSPI (CS0#)
ON	OFF	OFF	Carrier SPI (CS0#)
OFF	ON	ON	Module device – vendor specific
OFF	ON	OFF	Remote boot – vendor specific
OFF	OFF	ON	Module eMMC
OFF	OFF	OFF	Module SPI



For the BOOT source options referred to vendor specific, please refer to specific SMARC® module user manual for details.

Switch 2 of dual DIP Switch SW13 manages the FORCE_RECOV# signal. When the SW is in ON position, then the forced recovery functions are enabled.

3.3.29 POST Code Display

For debugging purposes, it is available a display made by 4x 7-segment LED display (D62 to D65), type Kingbright KCSC02-105 or equivalent.

The management of this display is done using a HT16K33_SOP28 LED controller, driven through the SMARC® module's I2C_GP Bus

3.3.30 Buttons

On the CSM-B79 carrier board, there are four momentary pushbuttons (with contacts normally open) for the direct handling of SMARC® module power management signals.

The first pushbutton, SW3, is placed on POWER_BTN# signal. Upon the pressure of this pushbutton, the SMARC® module will perform a power up / power down sequence.

The second pushbutton, SW4, is placed on RESET_IN# signal. Upon the pressure of this pushbutton, the SMARC® module will perform a reset.

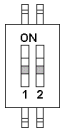
The third pushbutton, SW5, is placed on SLEEP# signal. Upon the pressure of this pushbutton, the SMARC® module will enter in a sleep state (if such states are supported by the module).

The fourth pushbutton, SW15, is placed on LID# signal. Such a signal can be used by the SMARC® module to detect the opening / the closure of an external lid switch, like those used to detect opening / closure of the notebooks. Upon changes in LID # state, the OS could trigger the transition of the module from Working to Sleep status, or vice versa.

All the above signals can be also remoted by using feature header CN45 (par.3.3.26)

In addition, it is possible to manage the LID# signal also using dedicated DIP Switch SW14, which also manages the TEST# signal (par.3.3.26)

SW14 Switch	ON Position	OFF Position
1	LID Button Simulation	Normal operation
2	Test mode	Normal operation



3.3.31 Others configuration Jumpers

CN53 position	SUS_S5
1-2	Normal working
2-3	Force _ALW voltages to enabled

CN53 jumper is is a 3-way jumper which allows to select between normal working mode or to disable the control of _ALW rails through CARRIER_PWRON signal to make them behave as _DSW rails.

CN62 position	VIN_PWR_BAD#
1-2	Not controlled
2-3	VSMARC Power Good

CN62 jumper is a 3-way jumper which allows to select if SMARC® Signal VIN_PWRBAD# must be controlled by an on-board voltage detector, which checks when VSMARC power rail is good, or must be left floating. This jumper can be used for its functionality (i.e. set in 2-3 position) only when the SMARC® module power in voltage VDD_IN value is set to 5V (7-8 position on CN8, par.2.3.3).

CN78 position	SMARC Pinout compatibility
1-2	SMARC V2.1 specs
2-3	SMARC V2.0 specs

CN78 jumper must be used to select if SMARC® MXM connector's signals are compliant to SMARC® specifications Rel. 2.0 or Rel. 2.1

3.3.32 Power / Status LEDs

On CSM-B79 carrier board there are some LEDs dedicated to notify the presence of voltage power rails:

D103: VDD_IN (ON, if present)

D104: +5V_ALW (ON, if present)

D105: +3V3_ALW (ON, if present)

D108: +12V_RUN (ON, if present)

D109: +5V_RUN (ON, if present)

D110: +3V3_RUN (ON, if present)

D107: +3V3_ALW, driven by +1V8_RUN (ON, if present)

D100: +3V3_ALW, driven by +1V8_ALW (ON, if present)

Some other LEDs are used to notify power management status:

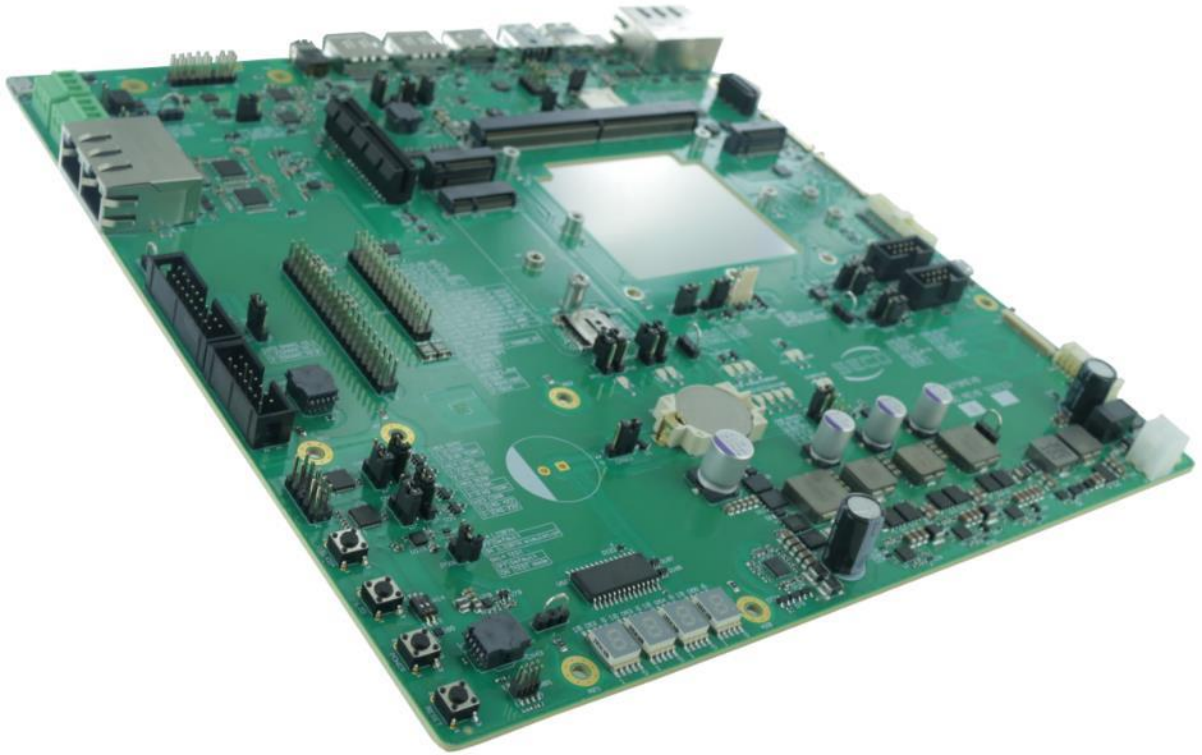
D114: VIN_PWR_BAD# (ON, if VDD_IN power rail is good)

D101: CARRIER_PWR_ON (ON, if Power on is ok)

D102: CARRIER_STBY# (OFF, if in standby mode)

Chapter 4.
Appendices

- Thermal Design
- Accessories



4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like SMARC® modules, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

SMARC® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the SMARC® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent a cooling solution. Until the modules are used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with fan could be sufficient for modules' cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat.

Indeed, when using CSM-B79 carrier board with any SMARC® module, it is necessary to consider carefully the global heat generated by the system, and the scenario of utilisation.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide SMARC® modules' specific heatspreaders and heatsinks (active and passive), but please remember that their use must be evaluated accurately inside the final system (electronics + mechanics), and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions, which also keeps the surface temperature of all carrier board's components in the temperature range specified for the specific carrier board configuration (industrial or commercial grade).

4.2 Accessories

The CSM-B79 Carrier Board will not be sold alone, but as a part of a more comprehensive Development kit, like those already available for Qseven Carrier boards.

The full development kit is coded as SMARC DEV KIT and does contain:

- Carrier board for SMARC® rel. 2.0 / 2.1 compliant modules CSM-B79
- Power adapter cable (Free wires on one extremity)
- 2 x DB-9 Serial cable adapter
- SATA 15p Power cable
- HDMI video cable
- DP video cable
- DP++ to HDMI video adapter converter
- eDP cable

A more detailed description can be found at related product page in Seco S.p.A website: SMARC DEV KIT (seco.com)

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