Com express

User Manual

COMe-C08 BT6

COM-Express™ Type 6 Module with the Intel® 8th generation Core™ / Xeon® CPUs

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	16 November 2018	First Official Release	SB

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

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INTRODUCTION

- Warranty
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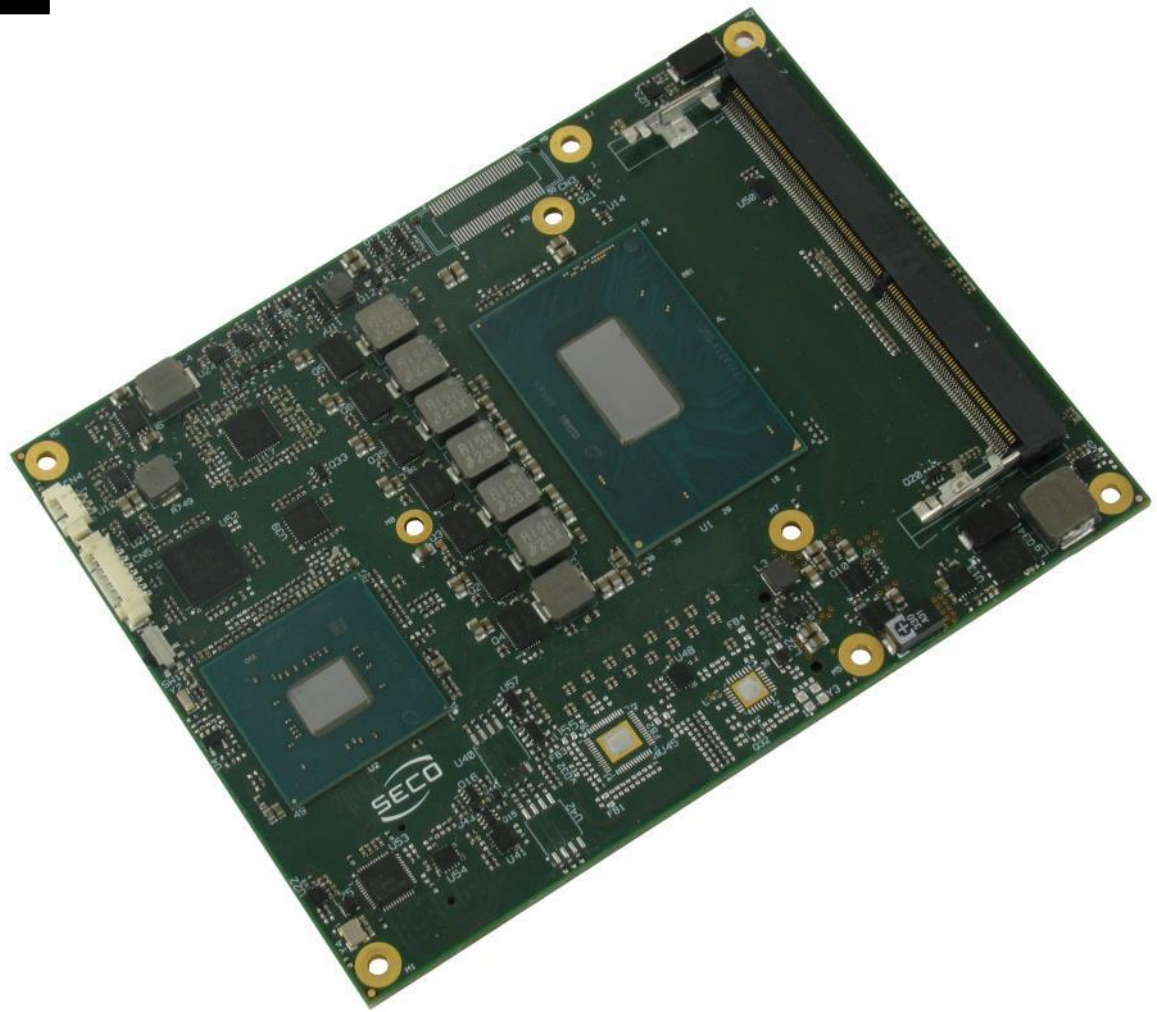


1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The COMe-C08-BT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The COMe-C08-BT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a COMe-C08-BT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The COMe-C08-BT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR4	DDR, 4th generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
ECC	Error Correcting Code, a peculiar type of memory module with 72-bit of data instead of 64, where the additional 8 bit are used to detect and correct possible errors on the remaining 64-bit data bus
eDP	embedded Display Port, a type of digital video display interface specifically developed for the internal connections between boards and digital displays
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signaling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable
N.C.	Not Connected

OS	Operating System
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port
PCH	Platform Controller Hub
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

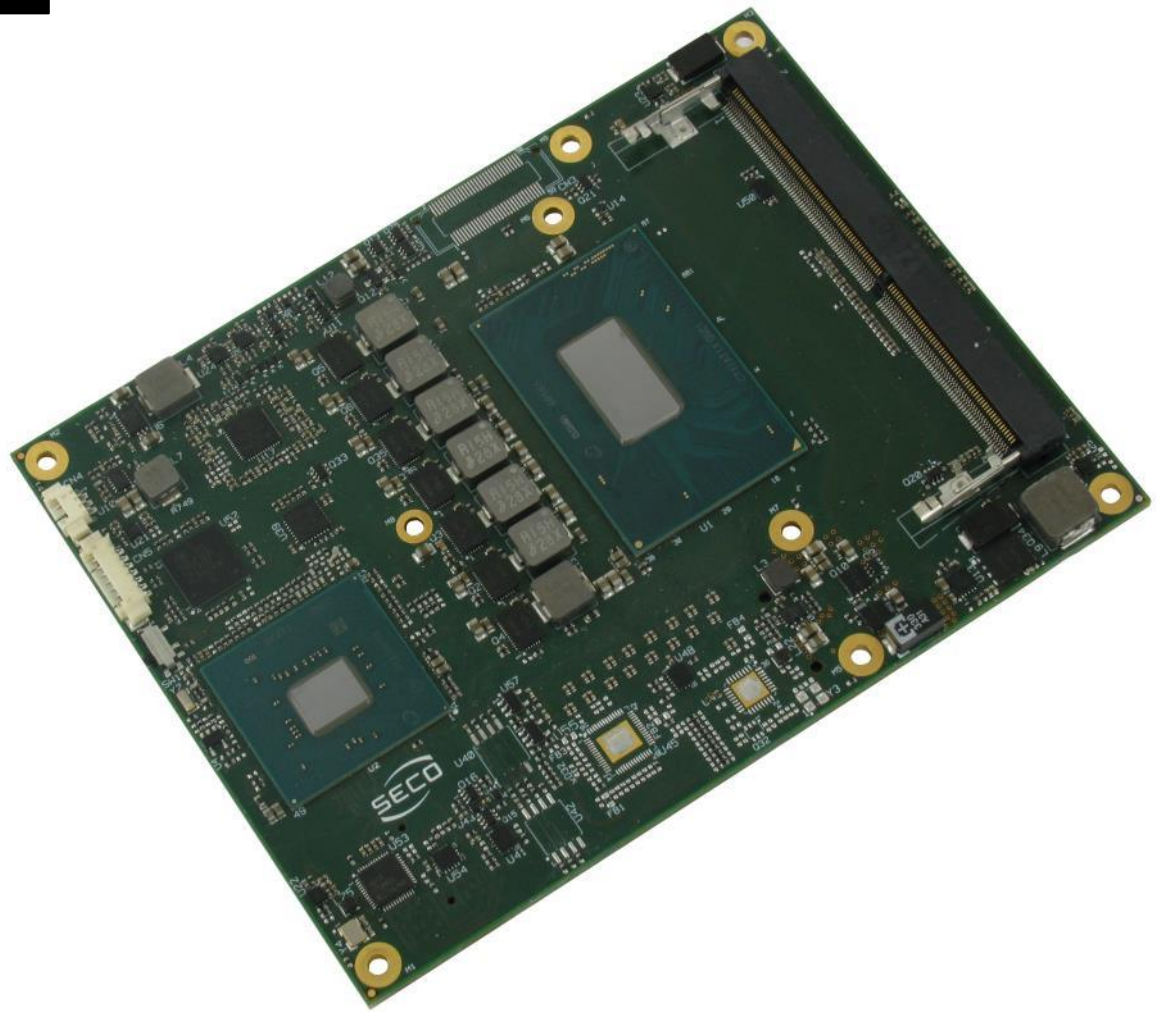
1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com Express	https://www.picmg.org/openstandards/com-express/
Com Express Carrier Design Guide	http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	https://cache.nxp.com/documents/user_manual/UM10204.pdf?fsrch=1&sr=2&pageNum=1
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
xHCI	http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html?wapkw=xhci
Intel® 8th generation Core™ / Xeon® CPUs	https://ark.intel.com/it/products/codename/97787/Coffee-Lake#@embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

The COMe-C08-BT6 is a COM Express® Type 6, basic Form Factor, based on the Intel® 8th generation Core™ or Xeon® CPUs, interfaced to Intel® QM370, HM370 or CM246 Platform Controller Hub, which completes its standard functionalities. A complete list of CPUs available is detailed in the next chapter.

All the supported CPUs offer a 64-bit Instruction set. Hyper Threading capabilities are also available on all CPUs, except for Core™-i3 CPUs.

The CPUs have direct access to the memory, which is available on two SODIMM DDR4 memory modules. Depending on the CPU, memory frequencies up to 2666MHz are supported, with a maximum capacity up to 32GB. Please notice that total amount of memory available is OS dependant.

The COMe-C08-BT6 modules equipped with Intel® Core™-i3 or Xeon® CPUs, combined with CM246 PCH, can support also ECC memory modules.

All CPUs integrate an Intel® UHD Graphics Controller, which offers an advanced 2D and 3D graphic engine and it is able to manage up to 3 independent displays (any combination possible between HDMI, DVI, DP++, eDP, LVDS and VGA). It makes available three Digital Display Interfaces that can be used to drive external Display Port, HDMI or DVI displays; moreover, the embedded Display Port interface can be carried out on COM Express connectors directly or used to realise a Dual Channel LVDS 18/24bit interface or a VGA interface (these are factory configurations; VGA interface will limit eDP interface to two lanes only, and DDI3 to HDMI only). Further graphical possibilities are given by CPU's PCI Express graphics x 16 interface, which can also be bifurcated in two PEG x8 ports or tifurcated in a PEG x8 plus two PEG x4 ports.

The embedded PCH complete the functionalities of the board offering HD Audio Interface, 9 x PCI Express ports (one of them used to manage a Gigabit Ethernet controller), 4 x Serial ATA channels, 8 USB 2.0 ports, 4 USB 3.0 ports, Real Time Clock, 2 x SPI interfaces, LPC and SM Bus.

The module can be offered with an optional additional TPM module.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.3.0 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available. Specifically, COMe-C08-BT6 is a COM Express® module, Basic Form factor, Type 6 (125mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means that once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

CPU

Intel® Xeon® E-2176M, Six Core @ 2.7GHz (4.4GHz in Turbo Boost), with HT, 12MB Cache, 45W TDP
Intel® Core™ i7-8850H, Six Core @ 2.6GHz (4.3GHz in Turbo Boost), with HT, 9MB Cache, 45W TDP
Intel® Core™ i5-8400H, Quad Core @ 2.5GHz (4.2GHz in Turbo Boost), with HT, 8MB Cache, 45W TDP
Intel® Core™ i3-8100H, Quad Core @ 3.0GHz, 6MB Cache, 45W TDP

Chipset

Intel® QM370, HM370 or CM246 Platform Controller Hub (PCH)

Memory

Two DDR4 SO-DIMM Slots supporting DDR4-2666
ECC DDR4 memory modules supported only with Xeon® and Core™ i3 CPUs combined with CM246 PCH

Graphics

Intel® UHD Graphics 630 (Core™ processors), P630 (Xeon® processors)
Up to 3 independent displays supported
DirectX® 12.1, OpenGL 4.5, and OpenCL 2.1 support
HW accelerated video decode MPEG2, VC1 / WMV9, AVC / H.264, VP8, JPEG / MJPEG, HEVC / H.265 (8-/10- bit), VP9
HW accelerated video encode MPEG2, AVC / H.264, VP8, JPEG, HEVC / H.265, VP9

Video Interfaces

Up to 3 x Digital Display Interfaces (DDIs), supporting DP1.2, DVI and HDMI 1.4
eDP 1.4 **or** 18/24 bit single/dual channel LVDS interface **or** LVDS + VGA interface

Video Resolutions

eDP, DP:	up to 4096x2304 @60Hz, 24bpp
HDMI:	up to 4096x2160 @30Hz, 24bpp
LVDS, VGA:	up to 1920x1200 @ 60Hz

Mass Storage

4 x S-ATA Gen3 channels
SD interface (shared with GPI/Os)

USB

8 x USB 2.0 Host Ports
4 x USB 3.0 Host ports

Networking

Gigabit Ethernet interface
Intel® I219-LM GbE Controller
Supports remote management (Intel® AMT Technology)

Audio

HD Audio interface

PCI Express

8 x PCI-e x1 Gen3 lanes
PCI Express Graphics (PEG) Gen3 x16 interface

Serial Ports

2 x serial ports (Tx/Rx only, TTL interface)

Other Interfaces

SPI
I2C
SM Bus
LPC bus
FAN management
4 x GPI, 4 x GPO (pins shared with SD interface)
LID# / SLEEP# / PWRBTN#, Watchdog
Optional TPM 2.0 on-board

Power supply voltage: +12V_{DC} ± 10% and + 5V_{SB} (optional)

Operating temperature: 0°C ÷ +60°C (commercial version) **

Dimensions: 125 x 95 mm (4.92" x 3.74")

! *** Temperatures indicated (minimum and maximum) are those measured at any point of SECO standard heat-spreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heat-spreader temperature in the range indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to COM Express® specifications, the COMe-C08-BT6 board needs to be supplied only with an external +12V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN6-AB and CN6-CD.

All remaining voltages needed for board's working are generated internally from +12V_{DC} power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

_SUS: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_SUS.

2.3.2 Power Consumption

COMe-C08-BT6 module, like all COM Express™ modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Therefore, power consumptions of the board are measured using a CCOMe-965 Carrier board on +12V_RUN power rail that supplies the board. For this reason, the values indicated in the table below are real power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board.

Power consumption in Suspend and Soft-Off States have been measured on +5V_ALW power rail. RTC power consumption has been measured on carrier board's backup battery when the system is not powered (VCC_RTC power rail). For the measurements, it has been used a DC Power Analyzer Keysight N6700B.

The current consumptions, written in the table of this page, have been measured using the following setup:

- O.S. Windows 10
- 16GB DDR4 (2 x 8GB SO-DIMM DDR4 2666MHz modules, p/n HYNIX HX426S15IB2K2/16)
- 120GB SATA Gen3 SSD (p/n Sandisk SDSSDA-120G-G27) connected
- USB mouse and keyboard connected
- HDMI display connected.

Status	CPU							
	i7-8850H + QM370		i5-8400H + HM370		i3-8100H		E-2176M + CM246	
	Average	Peak	Average	Peak	Average	Peak	Average	Peak
Idle, power saving configuration	0.323A	0.644A	0.320A	0.535A	0.357A	0.744A	0.320A	1.201A
OS Boot, power saving configuration	1.330A	5.979A	1.076A	6.380A	1.008A	2.407A	1.030A	7.730A
Video reproduction@1080p, power saving configuration	0.581A	1.493A	0.832A	1.135A	0.631A	0.786A	0.589A	1.021A
Video reproduction@4K, high performance	1.438A	3.360A	1.497A	1.788A	0.814A	1.058A	0.873A	3.812A
Intel Thermal Analysis Tool, high performance	4.539A	5.669A	4.598A	5.208A	3.773A	3.958A	4.476A	5.484A
Suspend to RAM (typical)	77mA							
Soft Off (typical)	120mA							
RTC Power consumption (typical)	2.9µA							

2.4 Mechanical Specifications

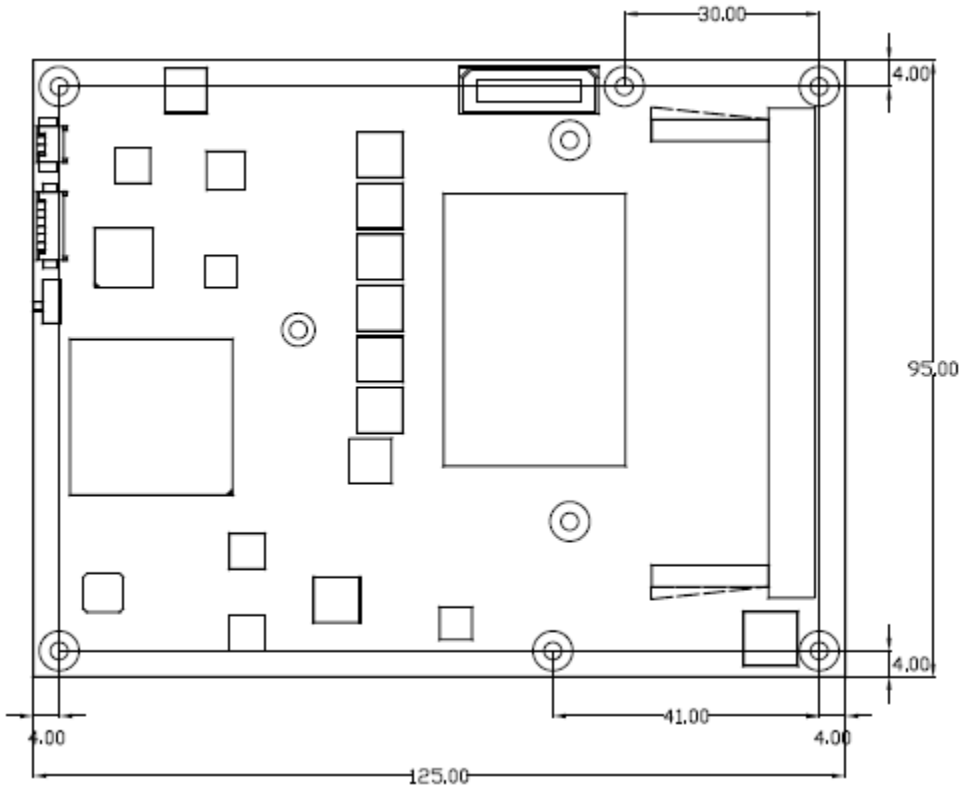
The COMe-C08-BT6 is a COM Express board, Basic form Factor type; therefore its dimensions are 125 mm x 95 mm (4.92" x 3.74").

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

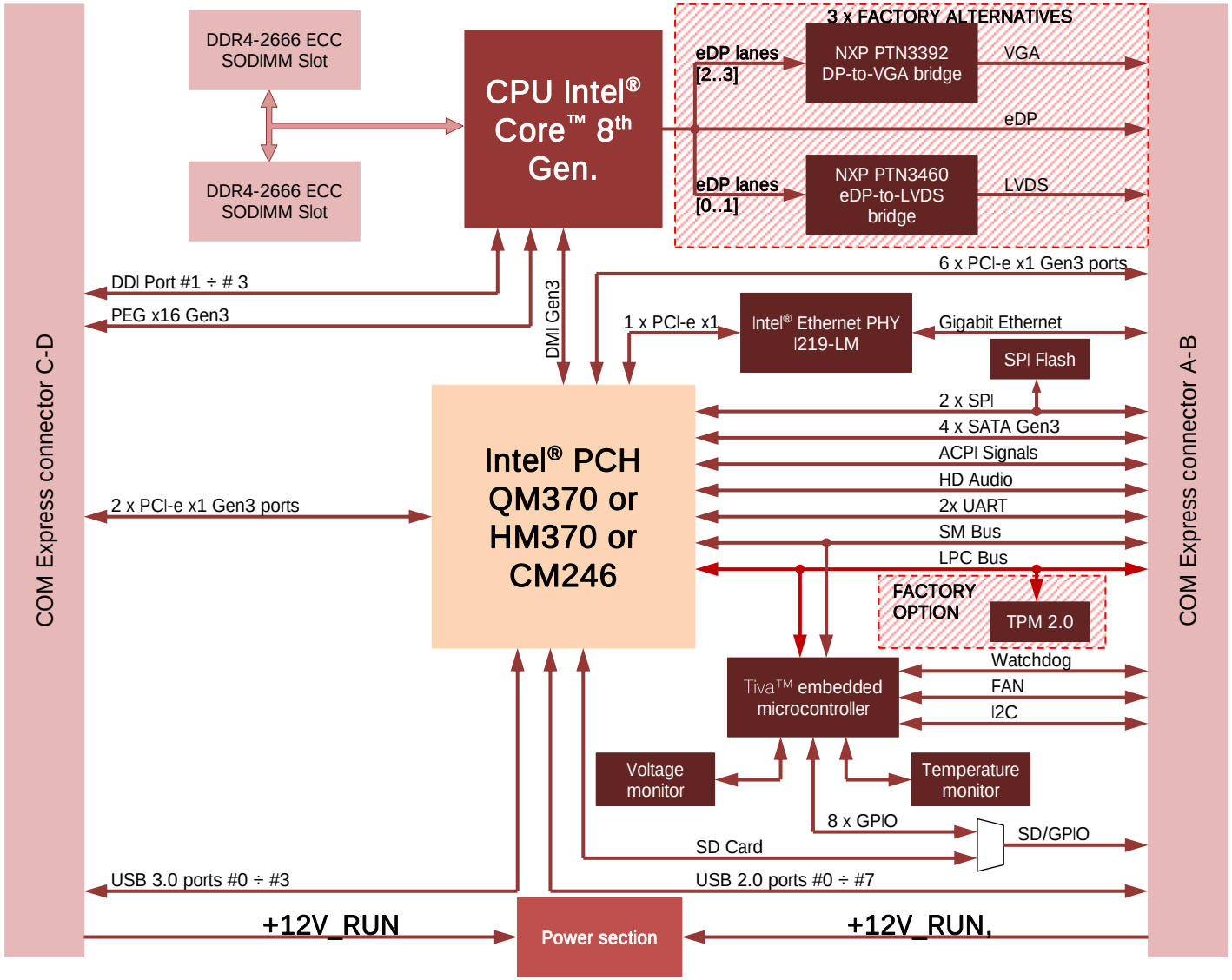
According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector's height is chosen, in designing a custom carrier board please remember that the SO-DIMM connector on bottom side of COMe-C08-BT6 is 4mm high (it is the component with the maximum height).

This value must be kept in high consideration when choosing the carrier board plugs' height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.

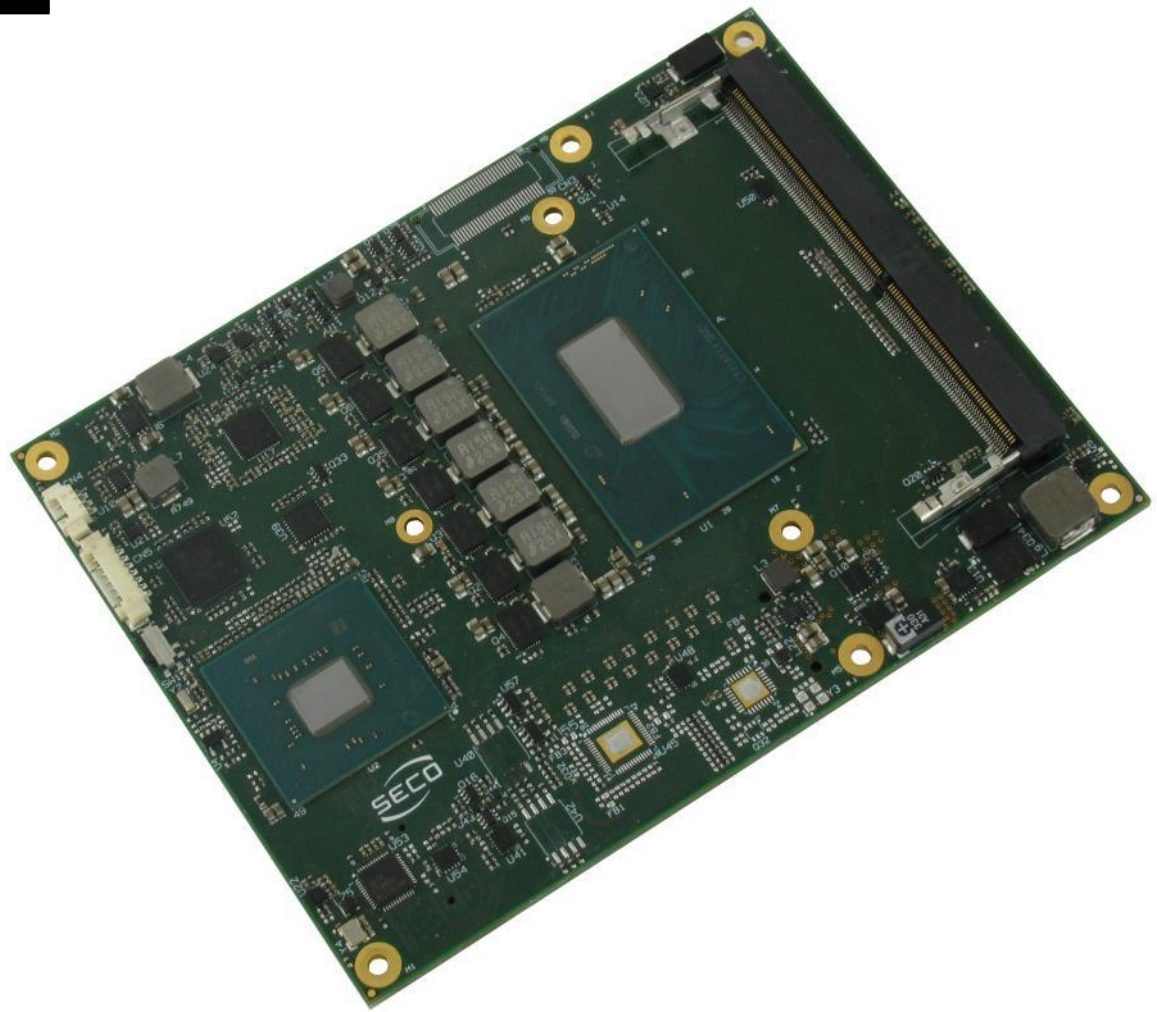


2.5 Block Diagram



Chapter 3.
CONNECTORS

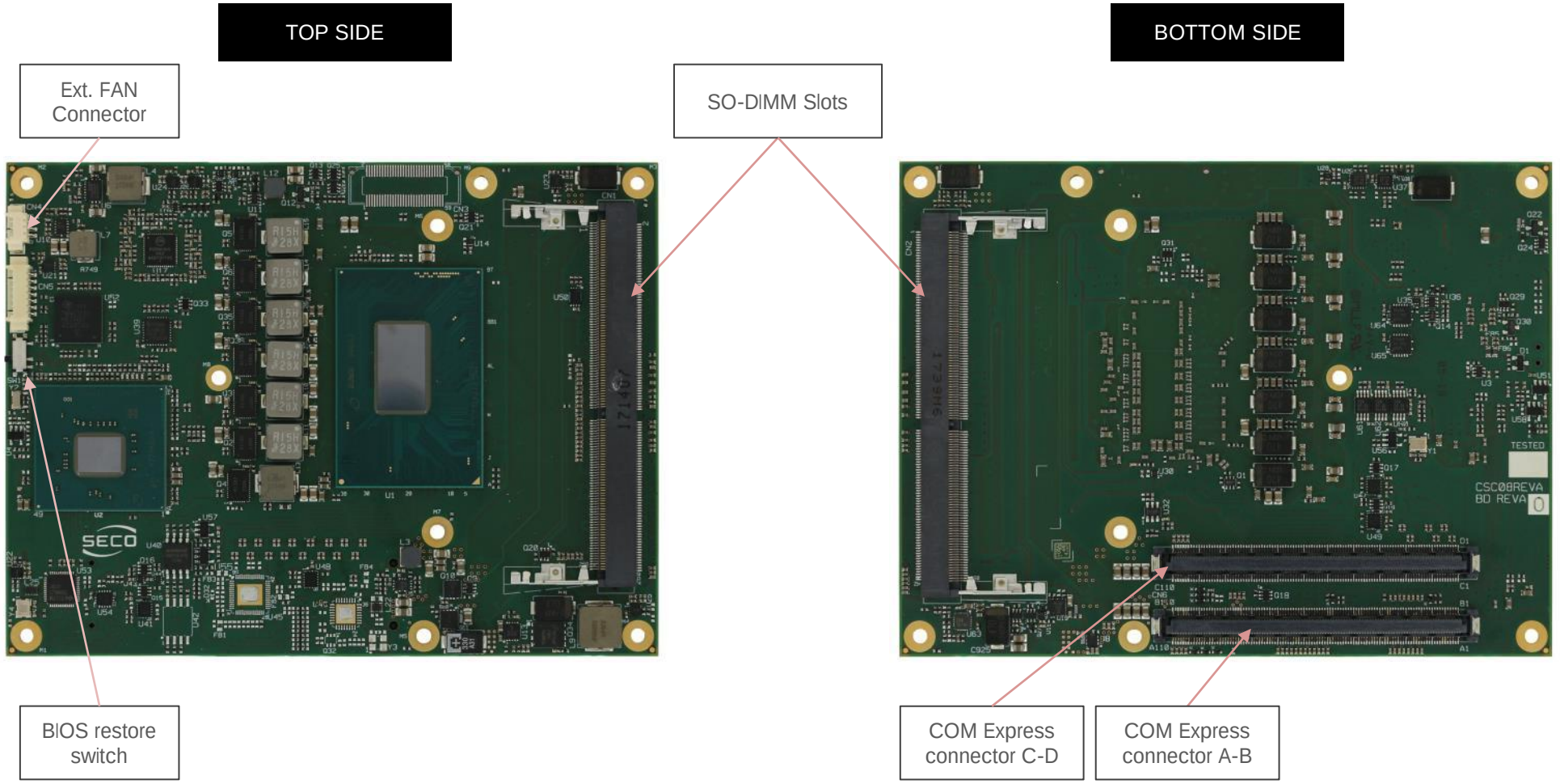
- Introduction
- Connectors description



3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.

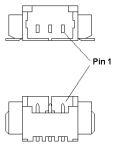


3.2 Connectors description

3.2.1 FAN Connector

FAN Connector - CN4	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of COMe-C08-BT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12V_{DC} FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0319 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_RUN derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_RUN electrical level signal with 10kΩ pull-up resistor and Schottky diode.

3.2.2 SO-DIMM DDR4 Slots

CPUs used on the COMe-C08-BT6 board provide support to DDR4-2666 SO-DIMM memory modules. Both ECC and non-ECC modules are supported.

Please be aware, however, that ECC DDR4 memory modules are supported only with Xeon® and Core™ i3 processors combined with CM246 Platform Controller Hub.

For use of this memories, on board there are two SO-DIMM DDR4 slots.

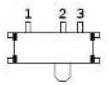
The socket placed on top side (CN1) is type LOTES p/n ADDR0208-P003A or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications.

The socket placed on bottom side (CN2) is type LOTES p/n ADDR0205-P003A or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support to dual channel memories.

3.2.3 BIOS Restore switch

In some cases, a wrong configuration of BIOS parameters could lead the module in an unusable state (i.e. no video output, all USB HID devices disabled).

For these cases, on the module it has been placed a 3-way switch which can be used to restore the BIOS to factory default configuration. To do so, it is necessary to place the contact of the switch in 1-2 position, then turn on the module, wait until the board has started regularly then turn off the module. The contact MUST be now placed back to 2-3 position.



During normal use, the contact MUST be always placed in 2-3 position.

3.2.4 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-C08-BT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

COM Express® Connector AB - CN6							
		ROW A			ROW B		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	A1	B1	GND	PWR	
GBE	I/O	GBE0_MDI3-	A2	B2	GBE0_ACT#	O	GBE
GBE	I/O	GBE0_MDI3+	A3	B3	LPC_FRAME#	O	LPC
GBE	O	GBE0_LINK100#	A4	B4	LPC_AD0	I/O	LPC
GBE	O	GBE0_LINK1000#	A5	B5	LPC_AD1	I/O	LPC
GBE	I/O	GBE0_MDI2-	A6	B6	LPC_AD2	I/O	LPC
GBE	I/O	GBE0_MDI2+	A7	B7	LPC_AD3	I/O	LPC
GBE	O	GBE0_LINK#	A8	B8	LPC_DRQ0#	I	LPC
GBE	I/O	GBE0_MDI1-	A9	B9	LPC_DRQ1#	I	LPC
GBE	I/O	GBE0_MDI1+	A10	B10	LPC_CLK	O	LPC
	PWR	GND	A11	B11	GND	PWR	
GBE	I/O	GBE0_MDI0-	A12	B12	PWRBTN#	I	PWR_MGMT
GBE	I/O	GBE0_MDI0+	A13	B13	SMB_CK	I/O	SMBUS
	N.A.	N.C.	A14	B14	SMB_DAT	O	SMBUS
PWR_MGMT	O	SUS_S3#	A15	B15	SMB_ALERT#	I	SMBUS
SATA	O	SATA0_TX+	A16	B16	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	A17	B17	SATA1_TX-	O	SATA
PWR_MGMT	O	SUS_S4#	A18	B18	SUS_STAT#	O	PWR_MGMT
SATA	I	SATA0_RX+	A19	B19	SATA1_RX+	I	SATA
SATA	I	SATA0_RX-	A20	B20	SATA1_RX-	I	SATA

	PWR	GND	A21	B21	GND	PWR	
SATA	O	SATA2_TX+	A22	B22	SATA3_TX+	O	SATA
SATA	O	SATA2_TX-	A23	B23	SATA3_TX-	O	SATA
PWR_MGMT	O	SUS_S5#	A24	B24	PWR_OK	I	PWR_MGMT
SATA	I	SATA2_RX+	A25	B25	SATA3_RX+	I	SATA
SATA	I	SATA2_RX-	A26	B26	SATA3_RX-	I	SATA
PWR_MGMT	I	BATLOW#	A27	B27	WDT	O	MISC
SATA	O	SATA_ACT#	A28	B28	HDA_SDIN2	I/O	AUDIO
AUDIO	O	HDA_SYNC	A29	B29	HDA_SDIN1	I/O	AUDIO
AUDIO	O	HDA_RST#	A30	B30	HDA_SDIN0	I/O	AUDIO
	PWR	GND	A31	B31	GND	PWR	
AUDIO	O	HDA_BITCLK	A32	B32	SPKR	O	MISC
AUDIO	O	HDA_SDOUT	A33	B33	I2C_CK	O	I2C
SPI	I	BIOS_DIS0#	A34	B34	I2C_DAT	I/O	I2C
MISC	O	THRMTRIP#	A35	B35	THRM#	I	MISC
USB	I/O	USB6-	A36	B36	USB7-	I/O	USB
USB	I/O	USB6+	A37	B37	USB7+	I/O	USB
USB	I	USB_6_7_OC#	A38	B38	USB_4_5_OC#	I	USB
USB	I/O	USB4-	A39	B39	USB5-	I/O	USB
USB	I/O	USB4+	A40	B40	USB5+	I/O	USB
	PWR	GND	A41	B41	GND	PWR	
USB	I/O	USB2-	A42	B42	USB3-	I/O	USB
USB	I/O	USB2+	A43	B43	USB3+	I/O	USB
USB	I	USB_2_3_OC#	A44	B44	USB_0_1_OC#	I	USB
USB	I/O	USB_0-	A45	B45	USB1-	I/O	USB
USB	I/O	USB_0+	A46	B46	USB1+	I/O	USB
	PWR	VCC_RTC	A47	B47	eSPI_EN#	I	LPC
	N.A.	N.C.	A48	B48	N.C.	N.A.	
	N.A.	N.C.	A49	B49	SYS_RESET#	I	PWR_MGMT
LPC	I/O	LPC_SERIRQ	A50	B50	CB_RESET#	O	PWR_MGMT

	PWR	GND	A51	B51	GND	PWR	
PCIE	O	PCIE_TX5+	A52	B52	PCIE_RX5+	I	PCIE
PCIE	O	PCIE_TX5-	A53	B53	PCIE_RX5-	I	PCIE
GPIO	I	GPI0	A54	B54	GPO1	O	GPIO
PCIE	O	PCIE_TX4+	A55	B55	PCIE_RX4+	I	PCIE
PCIE	O	PCIE_TX4-	A56	B56	PCIE_RX4-	I	PCIE
	PWR	GND	A57	B57	GPO2	O	GPIO
PCIE	O	PCIE_TX3+	A58	B58	PCIE_RX3+	I	PCIE
PCIE	O	PCIE_TX3-	A59	B59	PCIE_RX3-	I	PCIE
	PWR	GND	A60	B60	GND	PWR	
PCIE	O	PCIE_TX2+	A61	B61	PCIE_RX2+	I	PCIE
PCIE	O	PCIE_TX2-	A62	B62	PCIE_RX2-	I	PCIE
GPIO	I	GPI1	A63	B63	GPO3	O	GPIO
PCIE	O	PCIE_TX1+	A64	B64	PCIE_RX1+	I	PCIE
PCIE	O	PCIE_TX1-	A65	B65	PCIE_RX1-	I	PCIE
	PWR	GND	A66	B66	WAKE0#	I	PWR_MGMT
GPIO	I	GPI2	A67	B67	WAKE1#	I	PWR_MGMT
PCIE	O	PCIE_TX0+	A68	B68	PCIE_RX0+	I	PCIE
PCIE	O	PCIE_TX0-	A69	B69	PCIE_RX0-	I	PCIE
	PWR	GND	A70	B70	GND	PWR	
eDP/LVDS	O	eDP_TX2+/LVDS_A0+	A71	B71	LVDS_B0+	O	LVDS
eDP/LVDS	O	eDP_TX2-/LVDS_A0-	A72	B72	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP_TX1+/LVDS_A1+	A73	B73	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP_TX1-/LVDS_A1-	A74	B74	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP_TX0+/LVDS_A2+	A75	B75	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP_TX0-/LVDS_A2-	A76	B76	LVDS_B2-	O	LVDS
eDP/LVDS	O	eDP/LVDS_VDD_EN	A77	B77	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3+	A78	B78	LVDS_B3-	O	LVDS
LVDS	O	LVDS_A3-	A79	B79	eDP/LVDS_BKLT_EN	O	eDP/LVDS
	PWR	GND	A80	B80	GND	PWR	

eDP/LVDS	O	eDP_TX3+/LVDS_A_CK+	A81	B81	LVDS_B_CK+	O	LVDS
eDP/LVDS	O	eDP_TX3-/LVDS_A_CK-	A82	B82	LVDS_B_CK-	O	LVDS
eDP/LVDS	I/O	eDP_AUX+/LVDS_I2C_CK	A83	B83	eDP/LVDS_BKLT_CTRL	O	eDP/LVDS
eDP/LVDS	I/O	eDP_AUX-/LVDS_I2C_DAT	A84	B84	+5V_ALW	PWR	
GPIO	I	GPI3	A85	B85	+5V_ALW	PWR	
	N.A.	N.C.	A86	B86	+5V_ALW	PWR	
eDP	I	eDP_HPD	A87	B87	+5V_ALW	PWR	
PCIE	O	PCIE_CLK_REF+	A88	B88	BIOS_DIS1#	I	SPI
PCIE	O	PCIE_CLK_REF-	A89	B89	VGA_RED	O	VGA
	PWR	GND	A90	B90	GND	PWR	
SPI	O	SPI_POWER	A91	B91	VGA_GRN	O	VGA
SPI	I	SPI_MISO	A92	B92	VGA_BLU	O	VGA
GPIO	O	GPO0	A93	B93	VGA_HSYNC	O	VGA
SPI	O	SPI_CLK	A94	B94	VGA_VSYNC	O	VGA
SPI	O	SPI_MOSI	A95	B95	VGA_I2C_CK	I/O	VGA
MISC	I	TPM_PP	A96	B96	VGA_I2C_DAT	I/O	VGA
TYPE	N.A.	TYPE10#: N.C.	A97	B97	SPI_CS#	O	SPI
UART	O	SER0_TX	A98	B98	N.C.	N.A.	
UART	I	SER0_RX	A99	B99	N.C.	N.A.	
	PWR	GND	A100	B100	GND	PWR	
UART	O	SER1_TX	A101	B101	FAN_PWNOUT	O	MISC
UART	I	SER1_RX	A102	B102	FAN_TACHIN	I	MISC
PWR_MGMT	I	LID#	A103	B103	SLEEP#	I	PWR_MGMT
	PWR	+12V_RUN	A104	B104	+12V_RUN	PWR	
	PWR	+12V_RUN	A105	B105	+12V_RUN	PWR	
	PWR	+12V_RUN	A106	B106	+12V_RUN	PWR	
	PWR	+12V_RUN	A107	B107	+12V_RUN	PWR	
	PWR	+12V_RUN	A108	B108	+12V_RUN	PWR	
	PWR	+12V_RUN	A109	B109	+12V_RUN	PWR	
	PWR	GND	A110	B110	GND	PWR	

COM Express® Connector CD - CN6							
		ROW C			ROW D		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	C1	D1	GND	PWR	
	PWR	GND	C2	D2	GND	PWR	
USB	I	USB_SSRX0-	C3	D3	USB_SSTX0-	O	USB
USB	I	USB_SSRX0+	C4	D4	USB_SSTX0+	O	USB
	PWR	GND	C5	D5	GND	PWR	
USB	I	USB_SSRX1-	C6	D6	USB_SSTX1-	O	USB
USB	I	USB_SSRX1+	C7	D7	USB_SSTX1+	O	USB
	PWR	GND	C8	D8	GND	PWR	
USB	I	USB_SSRX2-	C9	D9	USB_SSTX2-	O	USB
USB	I	USB_SSRX2+	C10	D10	USB_SSTX2+	O	USB
	PWR	GND	C11	D11	GND	PWR	
USB	I	USB_SSRX3-	C12	D12	USB_SSTX3-	O	USB
USB	I	USB_SSRX3+	C13	D13	USB_SSTX3+	O	USB
	PWR	GND	C14	D14	GND	PWR	
	N.A.	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	I/O	DDI
	N.A.	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	I/O	DDI
	N.A.	N.C.	C17	D17	N.C.	N.A.	
	N.A.	N.C.	C18	D18	N.C.	N.A.	
PCIE	I	PCIE_RX6+	C19	D19	PCIE_TX6+	O	PCIE
PCIE	I	PCIE_RX6-	C20	D20	PCIE_TX6-	O	PCIE
	PWR	GND	C21	D21	GND	PWR	
PCIE	I	PCIE_RX7+	C22	D22	PCIE_TX7+	O	PCIE
PCIE	I	PCIE_RX7-	C23	D23	PCIE_TX7-	O	PCIE
DDI	I	DDI1_HPD	C24	D24	N.C.	N.A.	
	N.A.	N.C.	C25	D25	N.C.	N.A.	
	N.A.	N.C.	C26	D26	DDI1_PAIR0+	O	DDI

	N.A.	N.C.	C27	D27	DDI1_PAIR0-	O	DDI
	N.A.	N.C.	C28	D28	N.C.	N.A.	
	N.A.	N.C.	C29	D29	DDI1_PAIR1+	O	DDI
	N.A.	N.C.	C30	D30	DDI1_PAIR1-	O	DDI
	PWR	GND	C31	D31	GND	PWR	
DDI	I/O	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	O	DDI
DDI	I/O	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	O	DDI
DDI	I	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	I	DDI
	N.A.	N.C.	C35	D35	N.C.	N.A.	
DDI	I/O	DDI3_CTRLCLK_AUX+	C36	D36	DDI1_PAIR3+	O	DDI
DDI	I/O	DDI3_CTRLDATA_AUX-	C37	D37	DDI1_PAIR3-	O	DDI
DDI	I	DDI3_DDC_AUX_SEL	C38	D38	N.C.	N.A.	
DDI	O	DDI3_PAIR0+	C39	D39	DDI2_PAIR0+	O	DDI
DDI	O	DDI3_PAIR0-	C40	D40	DDI2_PAIR0-	O	DDI
	PWR	GND	C41	D41	GND	PWR	
DDI	O	DDI3_PAIR1+	C42	D42	DDI2_PAIR1+	O	DDI
DDI	O	DDI3_PAIR1-	C43	D43	DDI2_PAIR1-	O	DDI
DDI	I	DDI3_HPD	C44	D44	DDI2_HPD	I	DDI
	N.A.	N.C.	C45	D45	N.C.	N.A.	
DDI	O	DDI3_PAIR2+	C46	D46	DDI2_PAIR2+	O	DDI
DDI	O	DDI3_PAIR2-	C47	D47	DDI2_PAIR2-	O	DDI
	N.A.	N.C.	C48	D48	N.C.	N.A.	
DDI	O	DDI3_PAIR3+	C49	D49	DDI2_PAIR3+	O	DDI
DDI	O	DDI3_PAIR3-	C50	D50	DDI2_PAIR3-	O	DDI
	PWR	GND	C51	D51	GND	PWR	
PEG	I	PEG_RX0+	C52	D52	PEG_TX0+	O	PEG
PEG	I	PEG_RX0-	C53	D53	PEG_TX0-	O	PEG
TYPE	N.A.	TYPE0#: N.C.	C54	D54	PEG_LANE_RV#	I	PEG
PEG	I	PEG_RX1+	C55	D55	PEG_TX1+	O	PEG
PEG	I	PEG_RX1-	C56	D56	PEG_TX1-	O	PEG

TYPE	N.A.	TYPE1#: N.C.	C57	D57	TYPE2#: GND	N.A.	TYPE
PEG	I	PEG_RX2+	C58	D58	PEG_TX2+	O	PEG
PEG	I	PEG_RX2-	C59	D59	PEG_TX2-	O	PEG
	PWR	GND	C60	D60	GND	PWR	
PEG	I	PEG_RX3+	C61	D61	PEG_TX3+	O	PEG
PEG	I	PEG_RX3-	C62	D62	PEG_TX3-	O	PEG
	N.A.	N.C.	C63	D63	N.C.	N.A.	
	N.A.	N.C.	C64	D64	N.C.	N.A.	
PEG	I	PEG_RX4+	C65	D65	PEG_TX4+	O	PEG
PEG	I	PEG_RX4-	C66	D66	PEG_TX4-	O	PEG
	N.A.	N.C.	C67	D67	GND	PWR	
PEG	I	PEG_RX5+	C68	D68	PEG_TX5+	O	PEG
PEG	I	PEG_RX5-	C69	D69	PEG_TX5-	O	PEG
	PWR	GND	C70	D70	GND	PWR	
PEG	I	PEG_RX6+	C71	D71	PEG_TX6+	O	PEG
PEG	I	PEG_RX6-	C72	D72	PEG_TX6-	O	PEG
	PWR	GND	C73	D73	GND	PWR	
PEG	I	PEG_RX7+	C74	D74	PEG_TX7+	O	PEG
PEG	I	PEG_RX7-	C75	D75	PEG_TX7-	O	PEG
	PWR	GND	C76	D76	GND	PWR	
	N.A.	N.C.	C77	D77	N.C.	N.A.	
PEG	I	PEG_RX8+	C78	D78	PEG_TX8+	O	PEG
PEG	I	PEG_RX8-	C79	D79	PEG_TX8-	O	PEG
	PWR	GND	C80	D80	GND	PWR	
PEG	I	PEG_RX9+	C81	D81	PEG_TX9+	O	PEG
PEG	I	PEG_RX9-	C82	D82	PEG_TX9-	O	PEG
	N.A.	N.C.	C83	D83	N.C.	N.A.	
	PWR	GND	C84	D84	GND	PWR	
PEG	I	PEG_RX10+	C85	D85	PEG_TX10+	O	PEG
PEG	I	PEG_RX10-	C86	D86	PEG_TX10-	O	PEG

	PWR	GND	C87	D87	GND	PWR	
PEG	I	PEG_RX11+	C88	D88	PEG_TX11+	O	PEG
PEG	I	PEG_RX11-	C89	D89	PEG_TX11-	O	PEG
	PWR	GND	C90	D90	GND	PWR	
PEG	I	PEG_RX12+	C91	D91	PEG_TX12+	O	PEG
PEG	I	PEG_RX12-	C92	D92	PEG_TX12-	O	PEG
	PWR	GND	C93	D93	GND	PWR	
PEG	I	PEG_RX13+	C94	D94	PEG_TX13+	O	PEG
PEG	I	PEG_RX13-	C95	D95	PEG_TX13-	O	PEG
	PWR	GND	C96	D96	GND	PWR	
	N.A.	N.C.	C97	D97	N.C.	N.A.	
PEG	I	PEG_RX14+	C98	D98	PEG_TX14+	O	PEG
PEG	I	PEG_RX14-	C99	D99	PEG_TX14-	O	PEG
	PWR	GND	C100	D100	GND	PWR	
PEG	I	PEG_RX15+	C101	D101	PEG_TX15+	O	PEG
PEG	I	PEG_RX15-	C102	D102	PEG_TX15-	O	PEG
	PWR	GND	C103	D103	GND	PWR	
	PWR	+12V_RUN	C104	D104	+12V_RUN	PWR	
	PWR	+12V_RUN	C105	D105	+12V_RUN	PWR	
	PWR	+12V_RUN	C106	D106	+12V_RUN	PWR	
	PWR	+12V_RUN	C107	D107	+12V_RUN	PWR	
	PWR	+12V_RUN	C108	D108	+12V_RUN	PWR	
	PWR	+12V_RUN	C109	D109	+12V_RUN	PWR	
	PWR	GND	C110	D110	GND	PWR	

3.2.4.1 Audio interface signals

The COMe-C08-BT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard. Up to 3 HD audio codecs on the carrier board can be supported.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_ALW.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_ALW.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_ALW.

HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_ALW.

HDA_SDIN[0..2]: HD Audio Serial Data In signal. Inputs to the module from the Codec(s) placed on the Carrier board, electrical level +3.3V_ALW. HDA_SDIN2 is not managed by the PCH, it only has a 100kΩ pull-down resistor on the module.

The first four signals have to be connected to all the HD Audio codecs present on the carrier board. For each Codec, only one HDA_SDIN signal must be used. Please refer to the chosen Codecs' Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.4.2 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on COMe-C08-BT6 module, using an Intel® I219 Gigabit Ethernet controller, which is interfaced to the PCH through PCI-express lane #5.

Here following the signals involved in Gigabit Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

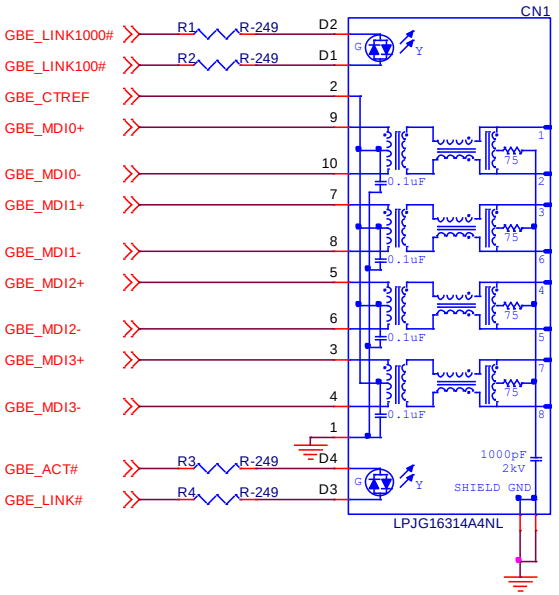
GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_ALW.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_ALW.



These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic given as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I219 Gigabit Ethernet controller, however, doesn't need the analogue powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.4.3 S-ATA signals

The Intel® HM370 / QM370 / CM246 PCH offer four S-ATA interfaces. All of them are carried out on COM Express® connector AB.

All SATA ports support 1.5 Gbps, 3.0 Gbps and 6.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA2_TX+/SATA2_TX-: Serial ATA Channel #2 Transmit differential pair.

SATA2_RX+/SATA2_RX-: Serial ATA Channel #2 Receive differential pair.

SATA3_TX+/SATA3_TX-: Serial ATA Channel #3 Transmit differential pair.

SATA3_RX+/SATA3_RX-: Serial ATA Channel #3 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_RUN voltage.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors.

3.2.4.4 PCI Express interface signals

COMe-C08-BT6 can offer externally eight PCI Express lane, which are managed by the Intel® HM370 / QM370 / CM246 PCH.

PCI express Gen3 (8GT/s) is supported.

PCI Express Lanes #0 ÷ #3 can be managed as:

- 1x PCI-e x4
- 2x PCI-e x2
- 1x PCI-e x2 + 2x PCI-e x1
- 4x PCI-e x1 ports.

The same occur with PCI Express Lanes #4 ÷ #7.

Please also be aware that these groupings cannot be changed dynamically, it is a fixed feature of the BIOS.

Unless differently specified, all the COMe-C08-BT6 purchased modules will be shipped in the "4+4 PCI-e x1 ports" configuration. When ordering a COMe-C08-BT6 module, please take care of specifying which are the desired PCI-e groupings.

Here following the signals involved in PCI express management (lanes #6 and #7 are available on connector CD, the other lanes are available on connector AB).

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE3_TX+/PCIE3_TX-: PCI Express lane #3, Transmitting Output Differential pair

PCIE3_RX+/PCIE3_RX-: PCI Express lane #3, Receiving Input Differential pair

PCIE4_TX+/PCIE4_TX-: PCI Express lane #4, Transmitting Output Differential pair

PCIE4_RX+/PCIE4_RX-: PCI Express lane #4, Receiving Input Differential pair

PCIE5_TX+/PCIE5_TX-: PCI Express lane #5, Transmitting Output Differential pair

PCIE5_RX+/PCIE5_RX-: PCI Express lane #5, Receiving Input Differential pair

PCIE6_TX+/PCIE6_TX-: PCI Express lane #6, Transmitting Output Differential pair

PCIE6_RX+/PCIE6_RX-: PCI Express lane #6, Receiving Input Differential pair

PCIE7_TX+/PCIE7_TX-: PCI Express lane #7, Transmitting Output Differential pair

PCIE7_RX+/PCIE7_RX-: PCI Express lane #7, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are eight different PCI express lanes and one PEG. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer must be used to replicate the reference clock to all the devices.

3.2.4.5 PEG interface signals

In addition to the seven PCI express lanes, described in the previous paragraph, the COMe-C08-BT6 module offer a PCI-Express x16 graphics interface (PEG), which can be used for connection of external graphics cards. Such an interface is directly managed by the Intel® Core™ / Xeon® processor's embedded GPUs.

The PEG signals can be managed as a single PCI-e x16 port, two PCI-e x8 ports or one PCI-ex8 plus two PCI-e x4 ports. Selection is made via BIOS (see par. 4.3.20)

PCI express Gen 3.0 is supported.

Here following the signals involved in PEG management.

PEG_TX[0..15]+/PEG_TX[0..15]-: PCI Express Graphics lane #0 ÷ #15, Transmitting Output Differential pairs.

PEG_RX[0..15]+/PEG_RX[0..15]-: PCI Express Graphics lane #0 ÷ #15, Receiving Output Differential pairs.

PEG_LANE_RV#: PCI Express Graphics lane reversal input strap, electrical level +3.3V_RUN with a 10kΩ pull-up resistor. This signal must be driven low, on the carrier board, only in case it is necessary to reverse the lane order of PEG interface. It must be left unconnected if lane reversal is not necessary.

3.2.4.6 USB interface signals

Intel® HM370 / QM370 / CM246 PCHs embed an xHCI controller, which is able to manage up to ten Superspeed ports (i.e. USB 3.0 compliant) and up to fourteen USB 1.x / 2.0 Host ports. Via BIOS settings it is possible to enable or disable the xHCI controller, therefore enabling USB 3.0 functionalities or leaving only USB 1.1 and USB 2.0 support.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB_0+/USB_0-: Universal Serial Bus Port #0 bidirectional differential pair.

USB_1+/USB_1-: Universal Serial Bus Port #1 bidirectional differential pair.

USB_2+/USB_2-: Universal Serial Bus Port #2 bidirectional differential pair.

USB_3+/USB_3-: Universal Serial Bus Port #3 bidirectional differential pair.

USB_4+/USB_4-: Universal Serial Bus Port #4 bidirectional differential pair.

USB_5+/USB_5-: Universal Serial Bus Port #5 bidirectional differential pair.

USB_6+/USB_6-: Universal Serial Bus Port #6 bidirectional differential pair.

USB_7+/USB_7-: Universal Serial Bus Port #7 bidirectional differential pair.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-C08-BT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signa.l, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-C08-BT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-C08-BT6 module.

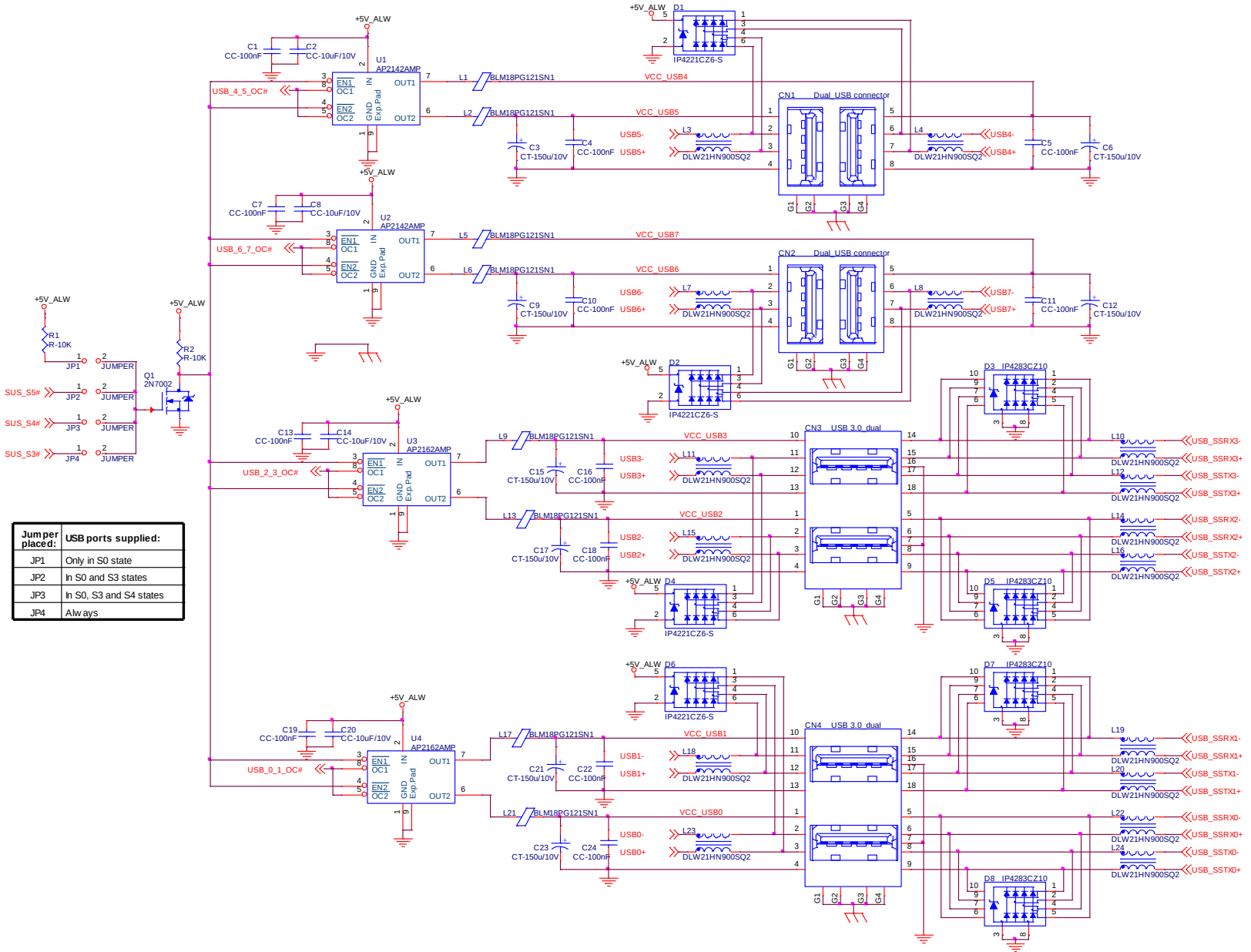
USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-C08-BT6 module.

100nF AC series decoupling capacitors are placed on each transmitting line of USB Super speed differential pairs.

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and 3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	In S0, S3 and S4 states
JP4	Always

3.2.4.7 LVDS Flat Panel signals

The Intel® 8th generation Core™ / Xeon® family of CPUs offers a native embedded Display Port (eDP). Conversely, the LVDS interface, which is frequently used in many application fields, is not directly supported by these CPUs.

For this reason, considering that LVDS interface can be multiplexed on the same pin with the eDP interface, on COMe-C08-BT6 module can be implemented an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for the Intel® 8th generation Core™ / Xeon® family of CPUs, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is possible to have available LVDS first channel **or** eDP interface.
>
> Please take care of specifying if LVDS interface or eDP is needed, before placing an order of COMe-C08-BT6 module.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: +3.3V_RUN electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: +3.3V_RUN electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

3.2.4.8 Embedded Display Port (eDP) signals

As described in the previous paragraph, the Intel® 8th generation Core™ / Xeon® family of CPUs offers a native 4-lanes embedded Display Port (eDP) interface.

As a factory option, the module can be configured with this eDP interface available on COM Express connector AB, which allows supporting displays with a resolution up 4096x2304 @ 60Hz.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1.

eDP_TX2+/eDP_TX2-: eDP channel differential data pair #2.

eDP_TX3+/eDP_TX3-: eDP channel differential data pair #3.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_RUN electrical level input with 100kΩ pull-down resistor.

eDP_VDD_EN: +3.3V_RUN electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: +3.3V_RUN electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

3.2.4.9 LPC interface signals

According to COM Express® specifications rel. 3.0, on the on COM Express connector AB there are 8 pins that can be used for implementation of Low Pin Count (LPC) Bus or enhanced SPI (eSPI) interfaces, which are two multiplexed interfaces made available by the PCH. However, since LPC bus is needed for the management of the Embedded microcontroller, then COMe-C08-BT6 module makes available only the LPC interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_RUN electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_RUN electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_RUN electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_RUN electrical level with 10kΩ pull-down resistor. This signal is used only by peripherals requiring Interrupt support.

LPC_DRQ[0÷1]#: LPC Serial DMA Request, +3.3V_RUN electrical level. These signals only have a 100kΩ pull-up resistor on module, internally they are not used

by the chipset nor by the Embedded Controller.

eSPI_EN#: this input signal should be used by the carrier board to request eSPI interface configuration, which is, however, not supported by the module. Therefore, driving low this signal would have no effect. Electrical level +3.3V_RUN with 100kΩ pull-up resistor.

3.2.4.10 SPI interface signals

The Intel® 8th generation Core™ / Xeon® family of CPUs offers also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of Serial Flash devices. Please be aware that this interface can be used exclusively to support platform firmware (BIOS).

Signals involved with SPI management are the following:

SPI_CS#: SPI Chip select, active low output signal, +3.3V_ALW electrical level with 10kΩ pull-up resistor. It can be internally multiplexed, depending on configuration of BIOS Disable x# signals, to be connected to the PCH's SPI_CS0# or SPI_CS1# signal

SPI_MISO: SPI Master In Slave Out, Input to COM Express® module from SPI devices embedded on the Carrier Board. Electrical level +3.3V_ALW.

SPI_MOSI: SPI Master Out Slave In, Output from COM Express® module to SPI devices embedded on the Carrier Board. Electrical level +3.3V_ALW with 3k1Ω pull-up resistor

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_ALW. Supported clock frequencies are 20, 33 and 50 MHz.

SPI_POWER: +3.3V_ALW Power Supply Output for carrier board's SPI devices.

BIOS_DIS[0÷1]#: BIOS Disable strap signals. These two signals are inputs of the COM Express® Module, that on the carrier board can be left floating or pulled down in order to select which SPI Flash device has to be used for module's boot. Please refer to table 4.13 of COM Express® Module Base Specifications rel. 2.1 for the meaning of possible configurations of these two signals.

3.2.4.11 Analog VGA interface

The Intel® 8th generation Core™ / Xeon® family of CPUs doesn't offer any analog display interface, which could be used for the connection of older VGA/CRT displays.

As a factory option, however, it is possible to purchase COMe-C08-BT6 modules equipped with an eDP to VGA bridge (NXP PTN3356BS), which allow the implementation of a VGA interface with a maximum supported resolution of 2048x1536 @ 50Hz (reduced blanking). Modules equipped with the eDP-to-VGA bridge can also mount the eDP-to-LVDS bridge, since the two bridges use different eDP lanes.

> **!** Please remember that the VGA interface is not native for the Intel® 8th generation Core™ / Xeon® family of CPUs, it is derived from an optional eDP-to-VGA bridge. Furthermore, DDI Port #3 Aux channel is required to drive the VGA bridge. This means that, on modules equipped with the eDP-to-VGA bridge only, the DDI interface #3 can be used exclusively in HDMI/DVI mode, not in DP++ mode
>
> Please take care of specifying if VGA interface is needed, before placing an order of COMe-C08-BT6 module.

Signals dedicated to VGA interface are the following:

VGA_RED: Red Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_GRN: Green Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_BLU: Blue Signal video output. A 150Ω pull-down resistor is placed on the line.

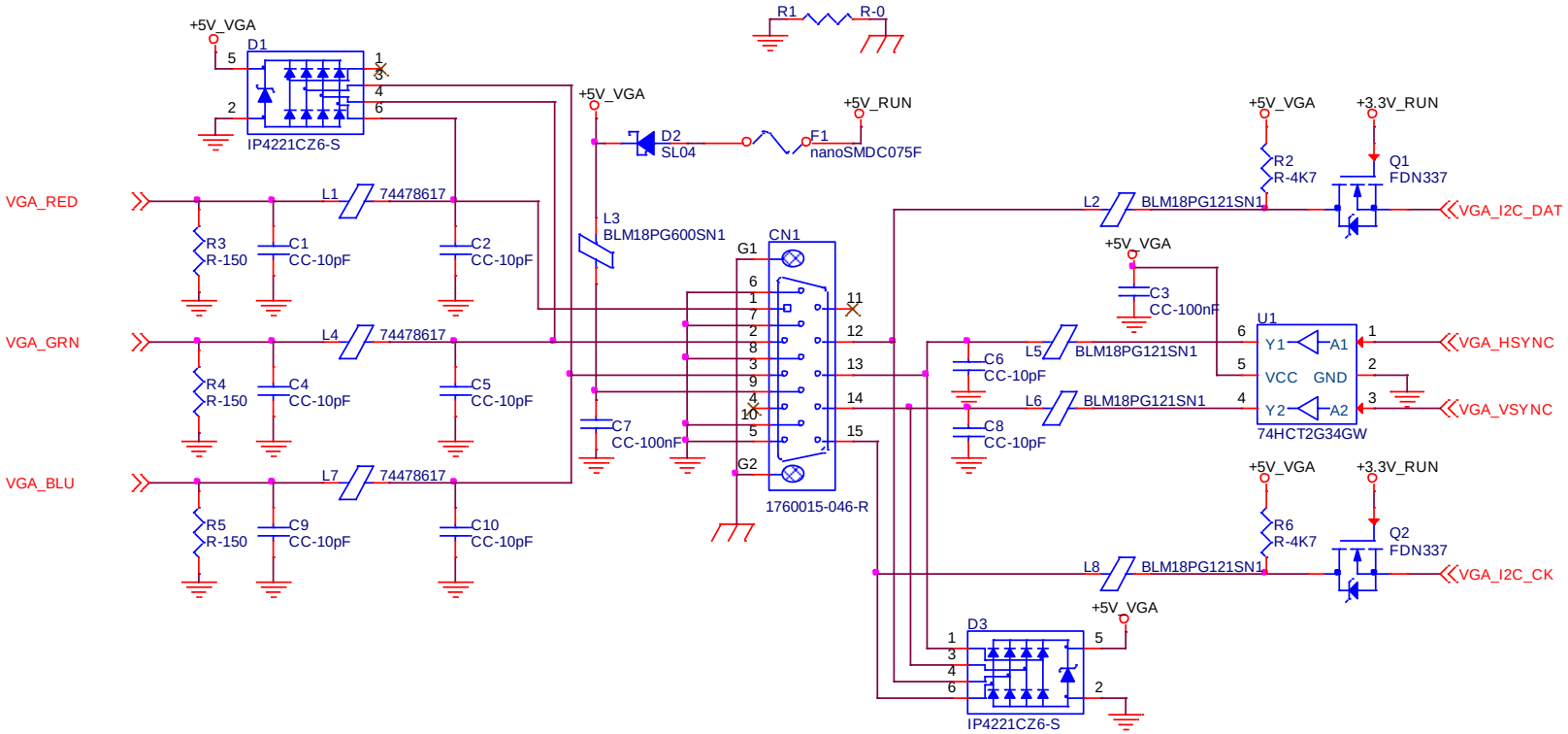
VGA_HSYNC: Horizontal Synchronization output signal.

VGA_VSYNC: Vertical Synchronization output signal.

VGA_I2C_CK: DDC Clock line for VGA displays detection. Output signal, electrical level +3.3V_RUN with 2K2Ω pull-up resistor.

VGA_I2C_DAT: DDC Clock line for VGA displays detection. Bidirectional signal, electrical level +3.3V_RUN with 2K2Ω pull-up resistor.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection like in the following example schematics.



3.2.4.12 Digital Display interfaces

The Intel® HD Graphics 630 / P630 controller, embedded inside the Intel® 8th generation Core™ / Xeon® family of CPUs, offer three Digital Display interfaces, which can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

Digital Display Interfaces - Pin multiplexing					
		Multimode Display Port mode		TMDS (HDMI/DVI) mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
D26	DDI1_PAIR0+	DP1_LANE0+	DP1 Differential pair #0 non-inverting line	TMDS1_DATA2+	TMDS1 Differential pair #2 non-inverting line
D27	DDI1_PAIR0-	DP1_LANE0-	DP1 Differential pair #0 inverting line	TMDS1_DATA2-	TMDS1 Differential pair #2 inverting line
D29	DDI1_PAIR1+	DP1_LANE1+	DP1 Differential pair #1 non-inverting line	TMDS1_DATA1+	TMDS1 Differential pair #1 non-inverting line
D30	DDI1_PAIR1-	DP1_LANE1-	DP1 Differential pair #1 inverting line	TMDS1_DATA1-	TMDS1 Differential pair #1 inverting line
D32	DDI1_PAIR2+	DP1_LANE2+	DP1 Differential pair #2 non-inverting line	TMDS1_DATA0+	TMDS1 Differential pair #0 non-inverting line
D33	DDI1_PAIR2-	DP1_LANE2-	DP1 Differential pair #2 inverting line	TMDS1_DATA0-	TMDS1 Differential pair #0 inverting line
D36	DDI1_PAIR3+	DP1_LANE3+	DP1 Differential pair #3 non-inverting line	TMDS1_CLK+	TMDS1 Differential clock non-inverting line
D37	DDI1_PAIR3-	DP1_LANE3-	DP1 Differential pair #3 inverting line	TMDS1_CLK-	TMDS1 Differential clock inverting line
C24	DDI1_HPD	DP1_HPD	DP1 Hot Plug Detect signal	HDMI1_HPD	HDMI #1 Hot Plug Detect signal
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	DP1 Auxiliary channel non-inverting line	HDMI1_CTRLCLK	DDC Clock line for HDMI panel #1.
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	DP1 Auxiliary channel inverting line	HDMI1_CTRLDATA	DDC Data line for HDMI panel #1.
D34	DDI1_DDC_AUX_SEL	DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
D39	DDI2_PAIR0+	DP2_LANE0+	DP2 Differential pair #0 non-inverting line	TMDS2_DATA2+	TMDS2 Differential pair #2 non-inverting line
D40	DDI2_PAIR0-	DP2_LANE0-	DP2 Differential pair #0 inverting line	TMDS2_DATA2-	TMDS2 Differential pair #2 inverting line
D42	DDI2_PAIR1+	DP2_LANE1+	DP2 Differential pair #1 non-inverting line	TMDS2_DATA1+	TMDS2 Differential pair #1 non-inverting line
D43	DDI2_PAIR1-	DP2_LANE1-	DP2 Differential pair #1 inverting line	TMDS2_DATA1-	TMDS2 Differential pair #1 inverting line
D46	DDI2_PAIR2+	DP2_LANE2+	DP2 Differential pair #2 non-inverting line	TMDS2_DATA0+	TMDS2 Differential pair #0 non-inverting line

D47	DDI2_PAIR2-	DP2_LANE2-	DP2 Differential pair #2 inverting line	TMDS2_DATA0-	TMDS2 Differential pair #0 inverting line
D49	DDI2_PAIR3+	DP2_LANE3+	DP2 Differential pair #3 non-inverting line	TMDS2_CLK+	TMDS2 Differential clock non-inverting line
D50	DDI2_PAIR3-	DP2_LANE3-	DP2 Differential pair #3 inverting line	TMDS2_CLK-	TMDS2 Differential clock inverting line
D44	DDI2_HPD	DP2_HPD	DP2 Hot Plug Detect signal	HDMI2_HPD	HDMI #2 Hot Plug Detect signal
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	DP2 Auxiliary channel non-inverting line	HDMI2_CTRLCLK	DDC Clock line for HDMI panel #2..
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	DP2 Auxiliary channel inverting line	HDMI2_CTRLDATA	DDC Data line for HDMI panel #2.
C34	DDI2_DDC_AUX_SEL	DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
C39	DDI3_PAIR0+	DP3_LANE0+	DP3 Differential pair #0 non-inverting line	TMDS3_DATA2+	TMDS3 Differential pair #2 non-inverting line
C40	DDI3_PAIR0-	DP3_LANE0-	DP3 Differential pair #0 inverting line	TMDS3_DATA2-	TMDS3 Differential pair #2 inverting line
C42	DDI3_PAIR1+	DP3_LANE1+	DP3 Differential pair #1 non-inverting line	TMDS3_DATA1+	TMDS3 Differential pair #1 non-inverting line
C43	DDI3_PAIR1-	DP3_LANE1-	DP3 Differential pair #1 inverting line	TMDS3_DATA1-	TMDS3 Differential pair #1 inverting line
C46	DDI3_PAIR2+	DP3_LANE2+	DP3 Differential pair #2 non-inverting line	TMDS3_DATA0+	TMDS3 Differential pair #0 non-inverting line
C47	DDI3_PAIR2-	DP3_LANE2-	DP3 Differential pair #2 inverting line	TMDS3_DATA0-	TMDS3 Differential pair #0 inverting line
C49	DDI3_PAIR3+	DP3_LANE3+	DP3 Differential pair #3 non-inverting line	TMDS3_CLK+	TMDS3 Differential clock non-inverting line
C50	DDI3_PAIR3-	DP3_LANE3-	DP3 Differential pair #3 inverting line	TMDS3_CLK-	TMDS3 Differential clock inverting line
C44	DDI3_HPD	DP3_HPD	DP3 Hot Plug Detect signal	HDMI3_HPD	HDMI #3 Hot Plug Detect signal
C36	DDI3_CTRLCLK_AUX+	DP3_AUX+	DP3 Auxiliary channel non-inverting line	HDMI3_CTRLCLK	DDC Clock line for HDMI panel #3.
C37	DDI3_CTRLDATA_AUX-	DP3_AUX-	DP3 Auxiliary channel inverting line	HDMI3_CTRLDATA	DDC Data line for HDMI panel #3.
C38	DDI3_DDC_AUX_SEL	DDI#3 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			

All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are +3.3V_RUN electrical level signal, active high with 100KΩ pull-down resistors.

All HDMI Control signals (CTRLCLK and CTRLDATA) are bidirectional signal, electrical level +3.3V_RUN with a 100kΩ pull-up (on Data) / pull-down (on clock) resistor

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

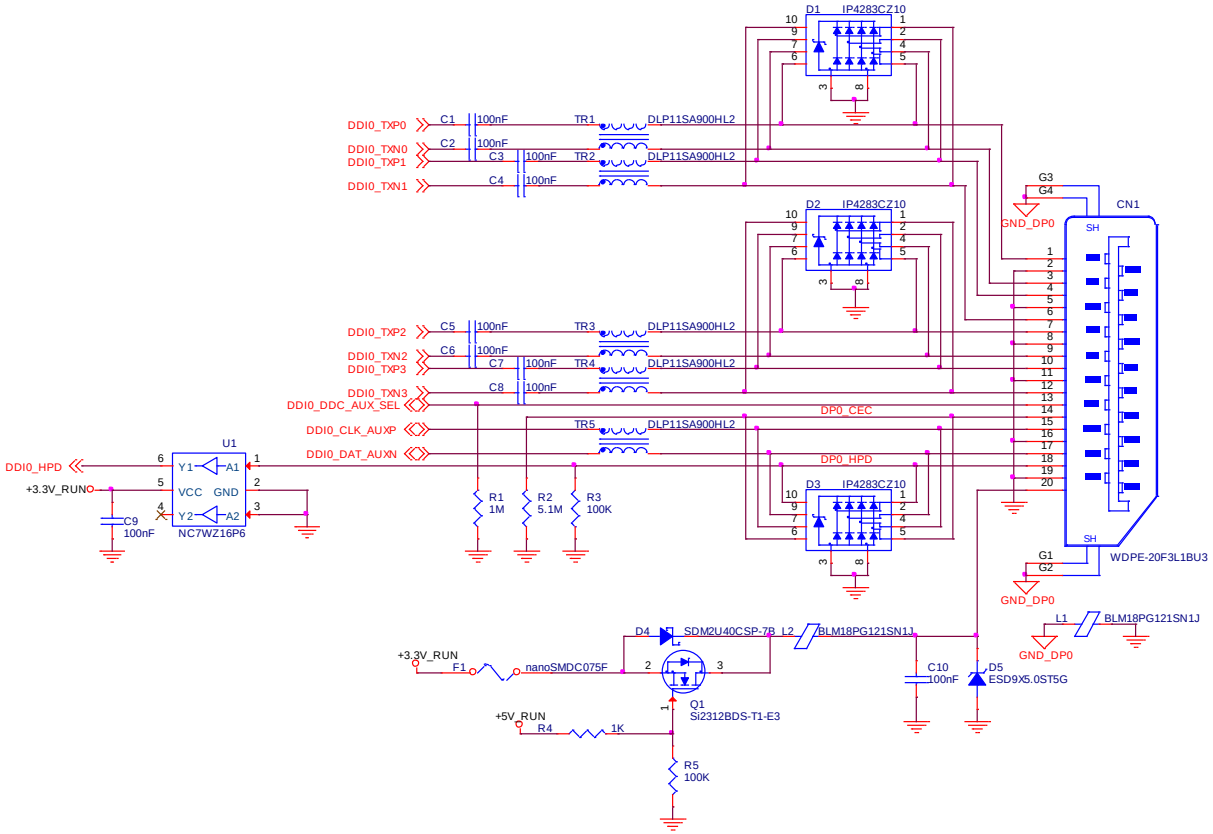
Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

!

Please remember that modules configured with the VGA video output will use the DDI Port #3 Aux channel to drive the eDP-to-VGA bridge. This means that on these modules, the DDI interface #3 can be used exclusively in HDMI/DVI mode, not in DP++ mode

Please take care of specifying if VGA interface is needed, before placing an order of COMe-C08-BT6 module.

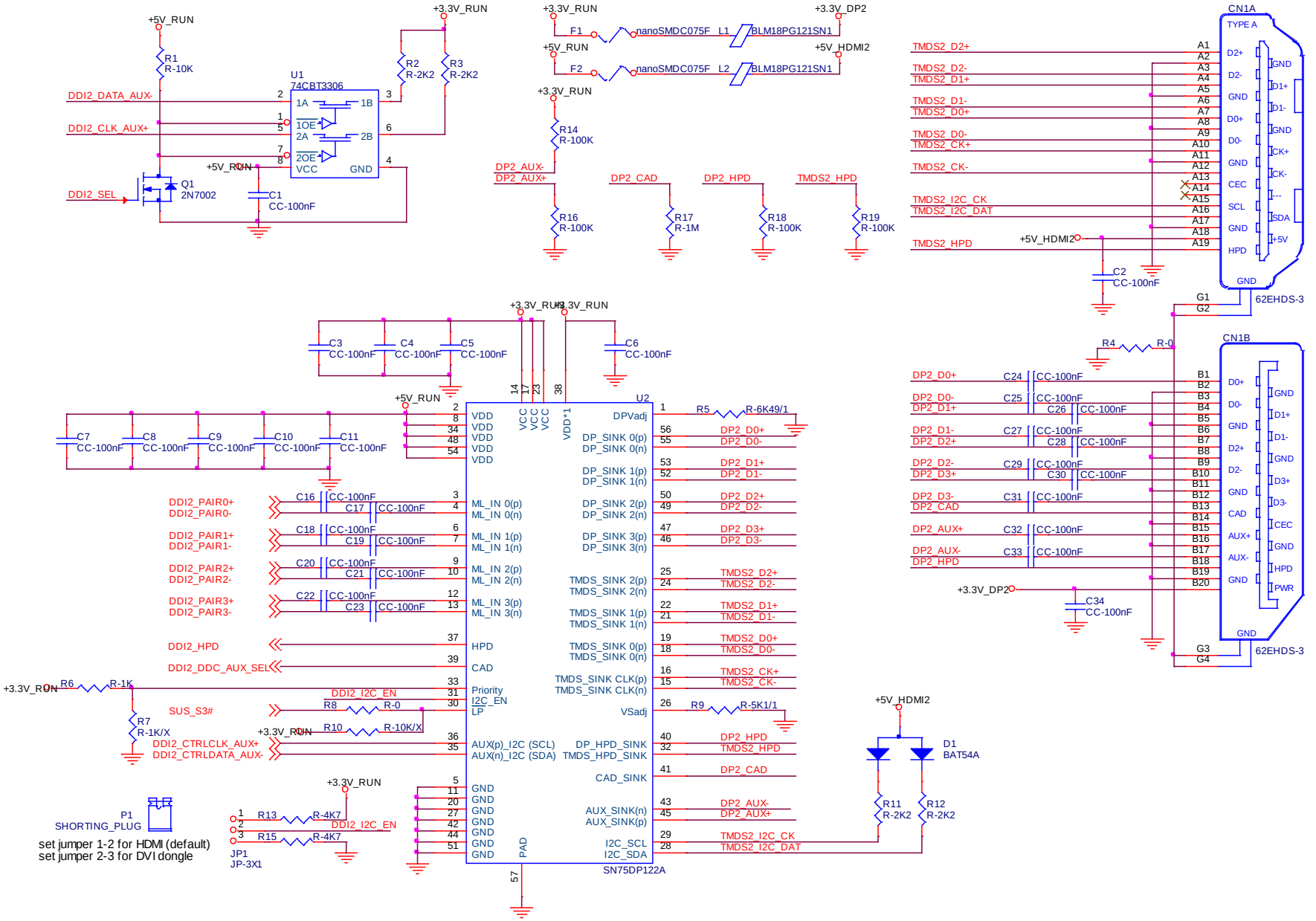
Here following an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #1, but any DDI interface can be used.



The example schematics in the following page, instead, shows the implementation (using DDI interface #2, but any DDI can be used for this purpose) of a double connector DP++ and HDMI, managed using a DisplayPort 1:2 Switch with Integrated TMDS Translator, which provides to TMDS voltage level shifter for HDMI/DVI connection.

By implementing such a schematic, the module can configure itself automatically to work with external HDMI/DVI or multimode Display Port interfaces, depending on the cable connected. In case both an HDMI and a DP are connected, the HDMI interface will take priority automatically. This order can be changed by removing resistor R6 and mounting resistor R7.

The jumper JP1 is used to enable or disable switch's I2C internal registers, for use of TMDS interface, respectively, for HDMI or DVI displays.


+5V_RUN
+3.3V_RUN
+3.3V_DP2
+5V_HDMI2
R1
R-10K
R2
R-2K2
R3
R-2K2
U1
74CBT3306
DDI2_DATA_AUX-
DDI2_CLK_AUX+
DDI2_SEL
Q1
2N7002
C1
CC-100nF
F1
F2
nanoSMDC075F
L1
L2
BLM18PG121SN1
R14
R-100K
R16
R-100K
R17
R-1M
R18
R-100K
R19
R-100K
DP2_AUX-
DP2_AUX+
DP2_CAD
DP2_HPD
TMDS2_HPD
CN1A
TYPE A
TMDS2_D2+
TMDS2_D2-
TMDS2_D1+
TMDS2_D1-
TMDS2_D0+
TMDS2_D0-
TMDS2_CK+
TMDS2_CK-
TMDS2_I2C_CK
TMDS2_I2C_DAT
C2
CC-100nF
G1
G2
62EHDS-3
C3
C4
C5
C6
C7
C8
C9
C10
C11
U2
SN75DP122A
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_HPD
DDI2_DDC_AUX_SEL
DDI2_I2C_EN
SUS_S3#
DDI2_CTRLCLK_AUX+
DDI2_CTRLDATA_AUX-
R4
R-0
CN1B
DP2_D0+
DP2_D0-
DP2_D1+
DP2_D1-
DP2_D2+
DP2_D2-
DP2_D3+
DP2_D3-
DP2_CAD
DP2_AUX+
DP2_AUX-
DP2_HPD
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
R5
R-6K49/1
R6
R-1K
R7
R-1K/X
R8
R-0
R9
R-5K1/1
R10
R-10K/X
D1
BAT54A
R11
R-2K2
R12
R-2K2
P1
SHORTING_PLUG
set jumper 1-2 for HDMI (default)
set jumper 2-3 for DVI dongle
R13
R-4K7
R15
R-4K7
JP1
JP-3X1

3.2.4.13 UART interface signals

According to COM Express® Rel. 3.0 specifications, since the COMe-C08-BT6 is a Type 6 module, it can offer two UART interfaces, which are directly managed by the Intel® HM370 / QM370 / CM246 PCH.

Here following the signals related to UART interface:

SER0_TX: UART Interface #0, Serial data Transmit (output) line, 3.3V_RUN electrical level.

SER0_RX: UART Interface #0, Serial data Receive (input) line, 3.3V_RUN electrical level.

SER1_TX: UART Interface #1, Serial data Transmit (output) line, 3.3V_RUN electrical level.

SER1_RX: UART Interface #1, Serial data Receive (input) line, 3.3V_RUN electrical level.

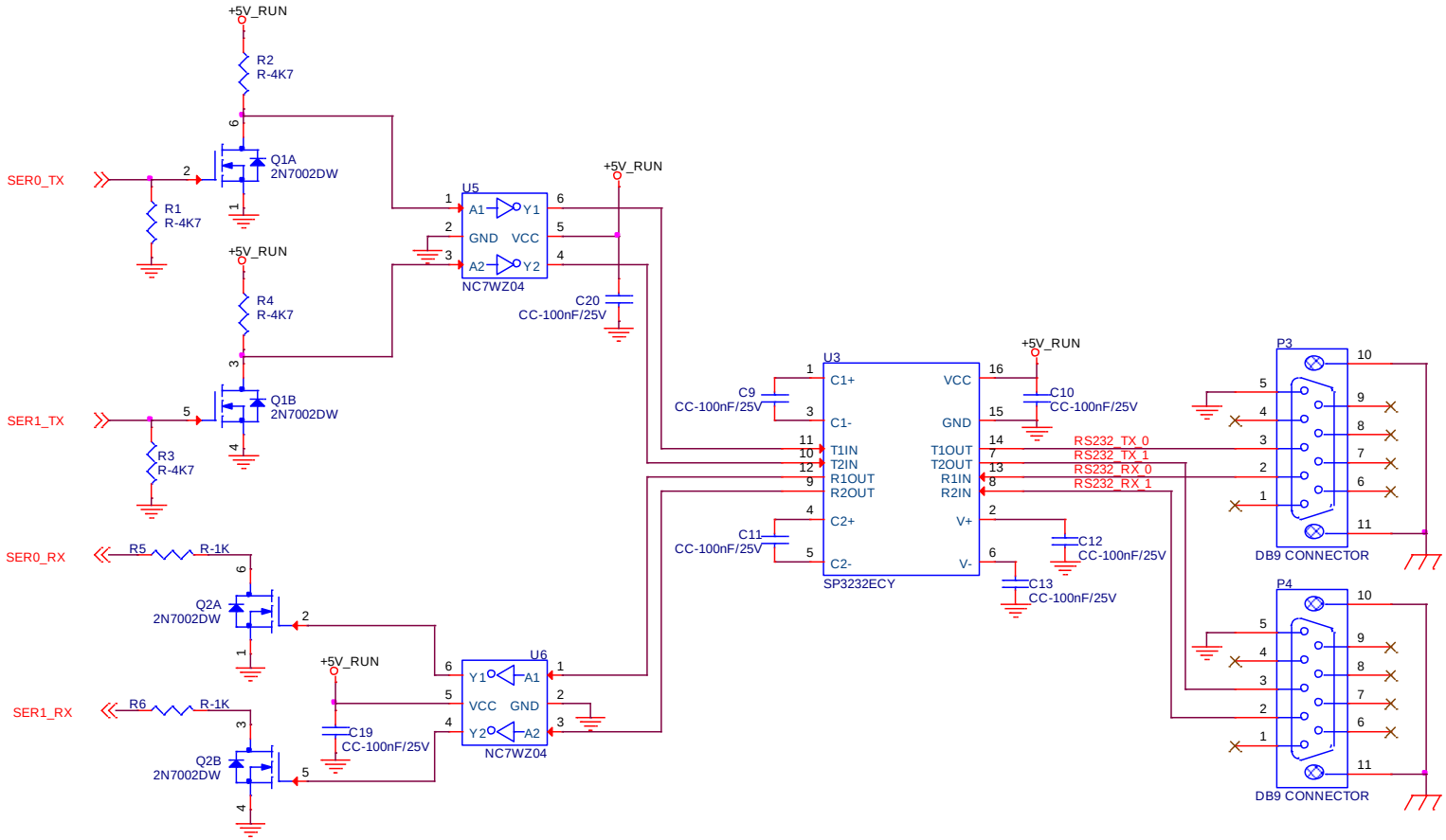
In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to +12V_{IN} power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then Schottky-diodes have been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the next page shows an example of implementation of RS-232 transceiver for the Carrier board.

Please be aware that the UARTs offered by the Intel® Processors are HS UARTs and not standard (legacy) COM ports.

Linux is able to manage them anyway, while Windows recognizes these interfaces as HS UART devices, not as legacy COM ports. This means that using Windows it is necessary to use specific drivers for the devices connected, it is not possible to use them using standard communication software like Tera Term, Putty…



3.2.4.14 I2C interface signals

This interface is managed by the embedded microcontroller.

Signals involved are the following

I2C_CK: general purpose I2C Bus clock line. Output signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

3.2.4.15 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-C08-BT6 module.

SPKR: Speaker output, +3.3V_ALW voltage signal, managed by the Intel® HM370 / QM370 / CM246 PCHs' embedded counter 2.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_RUN voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWM_OUT*: PWM output for FAN speed management, +3.3V_RUN voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHOIN*: External FAN Tachometer Input. +3.3V_RUN voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence Input, +3.3V_ALW voltage signal with 10kΩ pull-up resistor, managed by the optional TPM device on-module.

THRM#: Thermal Alarm Input. Active Low +3.3V_RUN voltage signal with 10kΩ pull-up resistor, directly managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_RUN voltage output signal with 10kΩ pull-up resistor. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the CPU began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

3.2.4.16 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_ALW buffered voltage signal with 47kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_ALW voltage signal with 47kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the COMe-C08-BT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_RUN voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is recommended.

PWR_OK: Power Good Input, +3.3V_RUN active high signal with 4k7Ω pull-up resistor. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_ALW electrical voltage signal. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal with 100kΩ pull-down resistor. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

S4#: S4 status output, active low +3.3V_ALW electrical voltage signal with 100kΩ pull-down resistor. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S4 (Suspend to Disk) power state.

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S5 (Soft Off) power state.

WAKE0#: PCI Express Wake Input, active low +3.3V_ALW electrical voltage signal with 1kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_ALW electrical voltage signal with 2k2Ω pull-up resistor. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used. While WAKE0# signal is managed directly by the Intel® HM370 / QM370 / CM246 PCHs, WAKE1#signal is managed by the Embedded microcontroller.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_ALW electrical level signal, with 47kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_ALW electrical level signal, with 47kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to LID# and SLEEP# inputs were dedicated to +12V_{IN} power rail. Protection circuitry has been added on LID# and SLEEP# so that they are +12V Tolerant. This has been made in order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6.

3.2.4.17 SMBus signals

This interface is managed by the Intel® HM370 / QM370 / CM246 PCH.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 2k2Ω pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 2k2Ω pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_ALW with a 1kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

3.2.4.18 GPIO/SDIO interface signals

According to COM Express® specifications rel. 2.0, there are 8 pins that can be used as General Purpose Inputs and Outputs **OR** as a SDIO interface.

The Intel® 8th generation Core™ / Xeon® family of CPUs, along with the HM370 / QM370 / CM246 PCHs offer the SD Card management, while the four GPIs and the four GPOs are managed by the embedded microcontroller. The choice between SD and GPIO interface can be made via BIOS (please check paragraph 4.3.20.

Please refer to the following table for a description of the signals in both configurations.

GPIO/SDIO Interfaces - Pin multiplexing					
		GPIO mode		SDIO mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
A54	GPI0	GPI0	General Purpose Input #0	SD_DATA0	SD Card Data Line 0.
A63	GPI1	GPI1	General Purpose Input #1	SD_DATA1	SD Card Data Line 2. Required only for 4-bit communication mode
A67	GPI2	GPI2	General Purpose Input #2	SD_DATA2	SD Card Data Line 2. Required only for 4-bit communication mode
A85	GPI3	GPI3	General Purpose Input #3	SD_DATA3	SD Card Data Line 1. Required only for 4-bit communication mode
A93	GPO0	GPO0	General Purpose Output #0	SD_CLK	SD Clock Output
B54	GPO1	GPO1	General Purpose Output #1	SD_CMD	SD Command/Response line. Bidirectional signal, used to send command from Host to the connected card, and the response from the card to the Host.
B57	GPO2	GPO2	General Purpose Output #2	SD_WP	Write Protect input. It is used to communicate the status of Write Protect switch of the external SD card.
B63	GPO3	GPO3	General Purpose Output #3	SD_CD#	Card Detect Input, active low Signal. This signal must be externally pulled low to signal when a SD Card Device is present.

Special consideration about SD_WP signal: since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal is tied to GND, otherwise the OS will always consider the card as protected from writing.

3.2.5 BOOT Strap Signals

Configuration straps are signals that, during system reset, are set as inputs (independently by their behaviour during normal operations) in order to allow the proper configuration of the processor / PCH. For this reason, on COMe-C08-BT6 are placed the pull-up or pull-down resistors that are necessary to configure the board properly.

The customer must avoid to place, on the carrier board, pull-up or pull-down resistors on signals that are used as strap signal, since it could result in malfunctions of COMe-C08-BT6 module.

The following signals are used as configuration straps by COMe-C08-BT6 module at system reset.

SPKR: pin B32 of connector AB. +3.3V_RUN voltage signal with PCH internal weak pull-down. Used to disable the PCH's "Top Swap" mode.

SMB_ALERT#: pin B15 of connector AB. +3.3V_ALW voltage signal with 1kΩ pull-up resistor. Used to support Intel® AMT with TLS (Transport Layer Security) and Intel® SBA (Small Business Advantage) with TLS.

SPI_MOSI: pin A95 of connector AB. Electrical level +3.3V_ALW with 3k1Ω pull-up resistor. This signal must always sample high during strap sampling.

HDA_SDOUT: pin A33 of connector AB. Used to disable Flash Descriptor Security. Signal at +3.3V_RUN voltage level with an internal weak pull-down resistor.

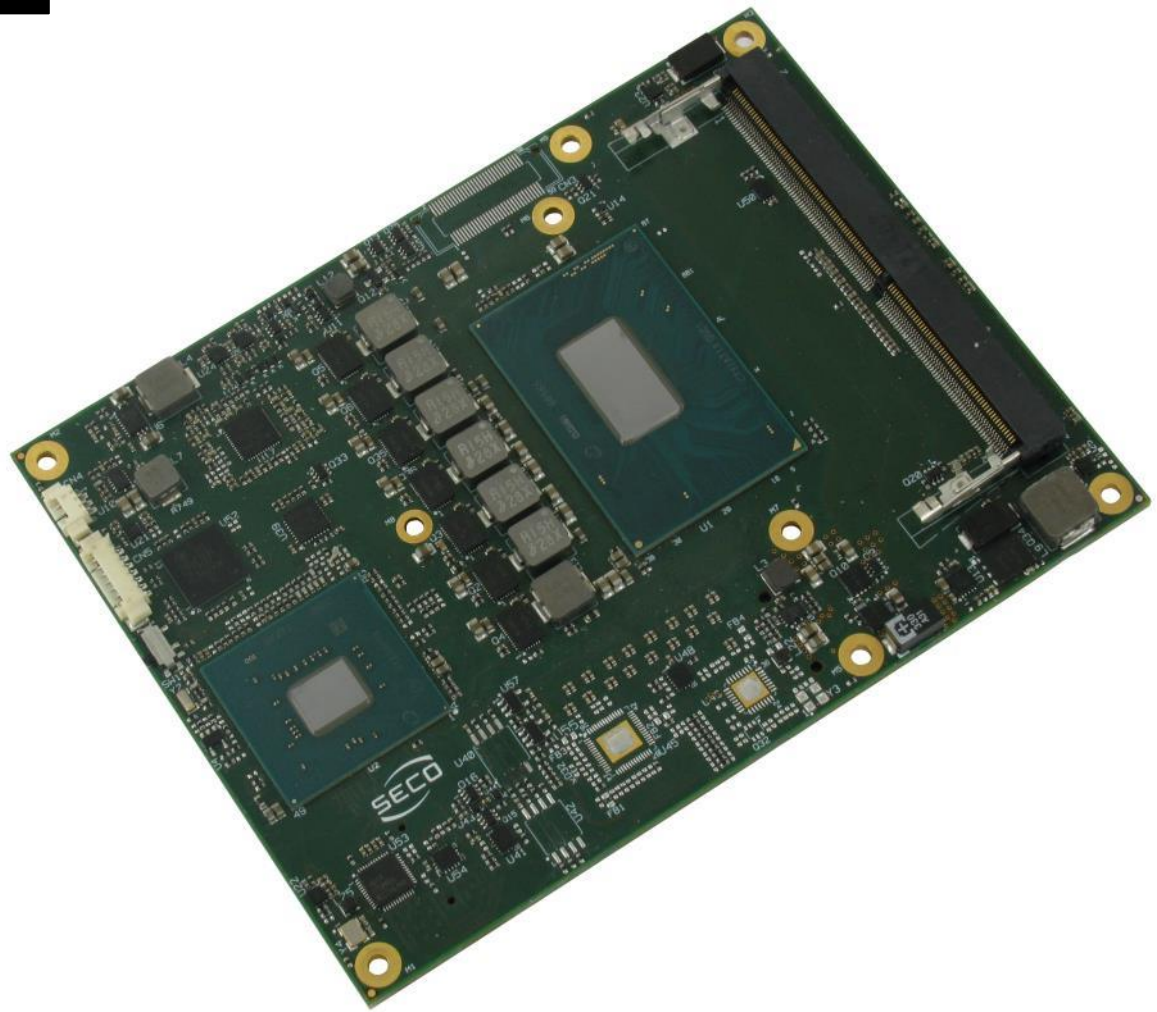
DPB_DATA_AUX_N: pin D16 of connector CD. This signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_RUN voltage level with a 100kΩ pull-up resistor.

DPC_DATA_AUX_N: pin C33 of connector CD. This signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_RUN voltage level with a 100kΩ pull-up resistor.

DPD_DATA_AUX_N: pin C37 of connector CD. This signal is used to detect (and therefore, to enable) the port. Signal at +3.3V_RUN voltage level with a 100kΩ pull-up resistor.

Chapter 4.
BIOS SETUP

- Aptio setup Utility
- Main setup menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu



4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. "Aptio Setup Utility", that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select "SCU" icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
+ / -	+ and - keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows displaying the General Help screen.
<F2>	Previous Values
<F3>	<F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted
<F4>	<F4> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub- screens.

It is possible to reset the UEFI BIOS Setup to Factory Defaults by using the dedicated switch available on module. Please check par. 3.2.3.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Power & Performance	See submenu	Power & Performance OptionsA
PCH-FW Configuration	See submenu	Configure Management Engine Technology Parameters
Trusted Computing	See submenu	Trusted Computing Settings
ACPI Settings	See submenu	System ACPI parameters
SMART settings	See submenu	System SMART Settings
Intel® Bios Guard Technology	See submenu	Enable/Disable Intel BIOS Guard Support
S5 RTC Wake Settings	See submenu	Enable System to wake from S5 using RTC alarm
Intel TXT Information	See submenu	Display Intel TXT Information
Acoustic Management Configuration	See submenu	Options to Enable or Disable Automatic Acoustic Management
AMI Graphic Output Protocol Policy	See submenu	User Selected Monitor Output by Graphic Output protocol
PCI Subsystem Settings	See submenu	PCI Subsystem Settings
USB Configuration	See submenu	USB Configuration Parameters
Network Stack Configuration	See submenu	Network Stack Settings
CSM Configuration	See submenu	Compatibility Support Module (CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc...
NVMe Configuration	See submenu	NVMe Device Options Settings
SDIO Configuration	See submenu	SDIO Configuration Parameters
Main thermal Configuration	See submenu	Main thermal Configuration
LVDS Configuration	See submenu	LVDS Configuration Parameters
SMBIOS Information	See submenu	SMBIOS Information
Embedded Controller	See submenu	Embedded Controller Parameters
T1s Auth Configuration	See submenu	T1s Auth Configuration

4.3.1 Power & performance submenu

Menu Item	Options	Description
CPU – Power management Control	See submenu	Enter the submenu to configure the Power Management Control Options for the CPU
GT – Power management Control	See submenu	Enter the submenu to configure the Power Management Control Options for the GT

4.3.1.1 CPU – Power management Control submenu

Menu Item	Options	Description
Link Speed	Max Battery Max Non-Turbo Performance Turbo Perfomance	Select the performance state that the BIOS will set starting from reset vector.
Intel® SpeedStep™	Disabled / Enabled	Enables or disables Intel® SpeedStep, allowing more than two frequency ranges to be supported.
Race To Halt (RTH)	Disabled / Enabled	Enables or disables Race to Halt feature. RTH will dynamically incease CPU frequency in order to ener pkg C-State faster to reduce overall power.
Intel® Speed Shift Technology	Disabled / Enabled	Enables or disables Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-States.
HDC Control	Disabled / Enabled	This option allows HDC Configuration, which could be enabled by the OS if OS native support is available
Turbo Mode	Disabled / Enabled	Enables or disables processor's Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled)
Config TDP Configurations	See submenu	Config TDP Configurations
C States	Disabled / Enabled	Enables or disables CPU power Management, Allows CPU to go to C States when it's not 100% utilized.

4.3.1.1.1 Config TDP Configurations submenu

Menu Item	Options	Description
Configurable TDP Boot Mode	Nominal Up Down Deactivate	Configurable TDP Mode as Nominal / Up / Down / Deactivate TDP Selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
Configurable TDP Lock	Enabled / Disabled	Configurable TDP Mode Lock sets the Lock bits on Turbo_Activation_Ratio and Config_TDP_Control. Note: when cDTP Lock is enabled, Cutom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
cTDP BIOS Control	Enabled / Disabled	Enables cTDP control via runtime ACPI BIOS methods. This "BIOS only" feature does not require EC or driver support.
Power Limit1	*Numerical Value*	Power Limit 1 in milliWatts, BIOS will round this value to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. When overclocking SKU, the value must be between Max and Min Power Limits (specified by Package_Power_SKU_MSR). For other SKUs, this value must be between Min Power Limit and TDP Limit
Power Limit 2	*Numerical Value*	Power Limit 2 Value in milliWatts, BIOS will round this value to the nearest 1/8W when programming. 0 = no custom override. For 12.50W, enter 12500. The processor applies control policies such that the package power does not exceed this limit.
Power Limit 1 Time Windows	*Numerical Value*	Power Limit 1 Time Windows value in second. The value may vary from 0 to 128. 0= use default value (28 sec). Defines the time window in which TDP value should be maintained.
ConfigTDP Turbo Activation Ratio	0..255	Custom value for Yurbo Activation Ratio. Needs to be configured with valid values from LFM to Max turbo. 0 means don't use custom value.

4.3.1.2 GT – Power management Control submenu

Menu Item	Options	Description
RC6 (Render Standby)	Enabled / Disabled	Permits to enable the render standby features, which allows the on-board graphics entering in standby mode to decrease power consumption
Maximum GT Frequency	Default Max Frequency / 100MHz / 150MHz / 200MHz / 250MHz / 300MHz / 350MHz / 400MHz / 450MHz / 500MHz / 550MHz / 600MHz / 650MHz / 700MHz / 750MHz / 800MHz / 850MHz / 900MHz / 950MHz / 1000MHz / 1050MHz / 1100MHz / 1150MHz / 1200MHz	Sets an user-limit for GT frequency. Choose between 350MHz (RPN) and 1150MHz (RP0). Value outer to this range will be clipped to the min/max supported by the SKU
Disable Turbo GT Frequency	Disabled / Enabled	With Enabled, the Turbo GT Frequency will be disabled. With Disabled, the Turbo GT Frequency will be kept disabled

4.3.2 PCH_FW Configuration submenu

Menu Item	Options	Description
ME State	Enabled / Disabled	When Disabled, the Management Engine (ME) will be put into ME Temporarily Disabled Mode. All the following items will be disabled
Manageability Features State	Enabled / Disabled	Enable/Disable Intel® Manageability feature. NOTE: this option will disable or Enable Manageability Features support in FW. To disable the support, the platform must be in an unprovisioned state first.
AMT BIOS Features	Enabled / Disabled	Only available when Manageability Feature State is Enabled. When disabled, AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup.
AMT Configuration	See submenu	Only available when Manageability Feature State is Enabled. Configures Intel® Active Management Technology Parameters.
ME Unconfig on RTC Clear	Enabled / Disabled	When Disabled, ME will not be unconfigured on RTC Clear
Comms Hub Support	Enabled / Disabled	Enables/Disables the support for Comms Hub
JHI Support	Enabled / Disabled	Enables/Disables Intel® DAL Host Interface Service (JHI)
Core Bios Done Message	Enabled / Disabled	Enables/Disables Core BIOS Done message Sent to NE
Firmware update configuration	See submenu	Configures Management Engine Technology parameters
PTT Configuration	See submenu	Configures PTT

4.3.2.1 AMT Configuration submenu

Menu Item	Options	Description
ASF Support	Enabled/Disabled	Enable or Disable Alert Standard Format Support
USB provisioning of AMT	Enabled/Disabled	Enable or Disable AMT USB provisioning
CIRA Configuration	See Submenu	Configure Remote Assistance Process parameters
ASF Configuration	See Submenu	Only Available when ASF Support is Enabled Configure Alert Standard Format parameters.
Secure Erase Configuration	See Submenu	Only Available when ASF Support is Enabled. Secure Erase Configuration menu.
OEM Flags Settings	See Submenu	Configure OEM Flags
MEBx Resolution Settings	See Submenu	Resolution Settings for MEBx display modes

4.3.2.1.1 CIRA Configuration submenu

Menu Item	Options	Description
Activate Remote Assistance process	Enabled/Disabled	Triggers CIRA boot. Note: Network Access must be activate first from MEBx Setup.
CIRA Timeout	0..255	Only Avaialble when " Activate Remote Assistance process" is set to Enabled. OEM defined timeout for MPS connection to be estabilished. 0 – use the default timeout value (60 seconds) 255 – MEBx wait until the connection is successful.

4.3.2.1.2 ASF Configuration submenu

Menu Item	Options	Description
PET Progress	Enabled/Disabled	Enable or Disable PET Event Progress to receive PET Events
Watchdog	Enabled/Disabled	Enable or Disable the Watchdog Timer.
OS Timer	0..65535	Only Available when "Watchdog" is Enabled. Set OS Watchdog Timer
BIOS Timer	0..65535	Only Available when "Watchdog" is Enabled. Set BIOS Watchdog Timer
ASF Sensors Tabel		Adds ASF Sensor Table into ASF ACPI Table

4.3.2.1.3 Secure Erase Configuration submenu

Menu Item	Options	Description
Secure Erase Mode	Simulated / reals	Change Secure Erase module behaviour: Simulated: Preforms SE flow without erasing SSD Real: Erase SSD
Force Secure Erase	Disabled / Enabled	Force Secure Erase on next boot

4.3.2.1.4 OEM Flags Settings submenu

Menu Item	Options	Description
MEBx hotkey pressed	Disabled / Enabled	OEMFlag Bit 1: Enable automatic MEBx hotkey press.
MEBx Selection Screen	Disabled / Enabled	OEMFlag Bit 2: Enable MEBx selection screen with 2 options: Press 1 to enter ME Configuration Screens Press 2 to initiate a remote connection Note: Network Access must be activate first from MEBx Setup.
Hide Unconfigure ME Confirmation Prompt	Disabled / Enabled	OEMFlag Bit 6: Hide Unconfigure ME confirmation prompt when attempting ME unconfiguration.
MEBx OEM Debug Menu Enable	Disabled / Enabled	OEMFlag Bit 14: Enable OEM debug menu in MEBx,
Unconfigure ME	Disabled / Enabled	OEMFlag Bit 15: Unconfigure ME with resetting MEBx password to default.

4.3.2.1.5 MEBx Resolution Settings submenu

Menu Item	Options	Description
Non-UI Mode Resolution	Auto 80x25 100x31	Resolution for non-UI text mode
UI Mode Resolution	Auto 80x25 100x31	Resolution for UI text mode
Graphics Mode Resolution	Auto 640x480 800x600 1024x768	Resolution for graphics mode.

4.3.2.2 Firmware Update Configuration submenu

Menu Item	Options	Description
ME FW Image Re-Flash	Enabled/Disabled	Enable or Disable Me FW Image Re-Flash function.

4.3.2.3 PTT Configuration submenu

Menu Item	Options	Description
TPM Device Selection	dTPM PTT	Selects TPM device: PTT or dTPM. PTT – enables PTT in SkuMgr dTPM – Disables PTT in SkuMgr. Warning! PTT/dTPM will be disabled and all data saved on it will be lost.

4.3.3 Trusted computing submenu

Menu Item	Options	Description
Security Device Support	Enabled / Disabled	Enables or Disables BIOS support for security device. OS will not show the Security Device. TCG EFI protocol and INT1A interface will not be available. When enabled all the following items will be available.
SHA-1 PCR Bank	Enabled / Disabled	Enables or disables SHA-1 PCR Bank
SHA256 PCR Bank	Enabled / Disabled	Enables or disables SHA256 PCR Bank
Pending Operation	None / TPM Clear	Schedule an Operation for the Security Device. NTE: your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	Enabled / Disabled	Enables or Disabled the Platform Hierarchy
Storage Hierarchy	Enabled / Disabled	Enables or Disabled the Storage Hierarchy
Endorsement Hierarchy	Enabled / Disabled	Enables or Disabled the Endorsement Hierarchy
TPM2.0 UEFI Spec Version	TCG_1_2 TCG_2	Select the TCG Spec Version support. TCG_1_2 is the compatible mode for Windows 8 / Windows 10. TCG 2 supports the new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	1.2 / 1.3	Select to tell OS to support PPI Spec Version 1.2 or 1.3. Please note that some HCK tests might not support 1.3
Device Select	Auto TPM 1.2 TPM 2.0	TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated

4.3.4 ACPI Settings

Menu Item	Options	Description
Enable ACPI Auto Configuration	Disabled / Enabled	Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled
Enable Hibernation	Disabled / Enabled	Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 (Suspend to RAM)	Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy resources	Disabled / Enabled	Enables or Disables Lock of Legacy resources
S3 Video Repost	Disabled / Enabled	Enables or Disables S3 Video Repost

4.3.5 SMART Settings submenu

Menu Item	Options	Description
SMART Self Test	Disabled / Enabled	Runs SMART Self Test on all HDDs during POST.

4.3.6 Intel® BIOS Guard Technology submenu

Menu Item	Options	Description
Intel BIOS Guard Support	Disabled / Enabled	Enables or Disables Intel BIOS Guard Support

4.3.7 S5 RTC Wake Settings submenu

Menu Item	Options	Description
Wake system from S5	Disabled By Every Day By Day of Month	Enables or disables System Wake on Alarm event. The following menu items will appear only when this voice is not set to Disabled
Wake up hour	0..23	Sets the wake up hour in 0..23 format (i.e.,3 means 3am, 15 means 3pm)
Wake up minute	0..59	Sets the wake up minute
Wake up second	0..59	Sets the wake up second
Day of Month	1..31	This item is available only when "Wake system from S5" is set to "By Day of Month". Sets the day of month for Wake on Alarm event. Valid range s from 1 to 31, error checking will be done against month/day/year combinations that are not valid.

4.3.8 Intel TXT Information

Display only screen, Intel TXT information

4.3.9 Acoustic Management Configuration

Options to Enable or Disable Automatic Acoustic Management depends on HDD found connected to the system.

4.3.10 AMI graphic Output Protocol Policy submenu

Menu Item	Options	Description
Output Select	*List of available / connected module s video interfaces*	

4.3.11 PCI Subsystem Settings submenu

Menu Item	Options	Description
BME DMA Mitigation	Disabled / Enabled	Re-enable Bus Master Attribute disabled during PCI enumeration for PCI Bridges after SMM has been locked
Hot- Plug Support	Disabled / Enabled	Globally Enables or Disables Hot-Plug support for the entire System. If System has Hot-Plug capable Slots and this option is set to Enabled, it provides a Setup Screen for selecting resource padding for Hot-Plug

4.3.12 USB configuration submenu

Menu Item	Options	Description
Legacy USB Support	Enabled / Disabled / Auto	Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
XHCI hand-off	Enabled/ Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enabled/ Disabled	Enables or disables USB Mass Storage Driver Support
USB Transfer time-out	1 sec / 5 sec / 10 sec / 20 sec	Sets the time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10 sec / 20 sec / 30 sec / 40 sec	USB mass storage device Start Unit command time-out
Device power-up delay	Auto / Manual	Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor).
Device power-up delay in seconds	[1..40]	Delay range in seconds, in one second increment

4.3.13 Network Stack configuration submenu

Menu Item	Options	Description
Network Stack	Enabled / Disabled	Enables or disables UEFI Network Stack. When enabled, following menu items will appear
Ipv4 PXE Support	Enabled / Disabled	Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created
Ipv4 HTTP Support	Enabled / Disabled	Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created
Ipv6 PXE Support	Enabled / Disabled	Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created
Ipv6 HTTP Support	Enabled / Disabled	Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created
IPSEC certificate	Enabled / Disabled	Support to Enable/Disable IPSEC certificate for Ikev.
PXE boot wait time	[0..5]	Wait time to press ESC key to abort the PXE boot
Media detect count	[1..50]	Number of times that the presence of media will be checked

4.3.14 CSM configuration submenu

Menu Item	Options	Description
CSM Support	Enabled / Disabled	Enables or disables the Compatibility Support Module (CSM) Support. When enabled, the following menu items will appear
GateA20 Active	Upon Request Always	Upon Request: GateA20 can be disabled using BIOS services, Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB.
INT19 Trap Response	Immediate Postponed	BIOS Reaction on INT19 trapping by Option ROM: IMMEDIATE - execute the trap right away; POSTPONED - execute the trap during legacy boot
Boot option filter	UEFI and Legacy Legacy only UEFI only	This option controls Legacy / UEFI ROMs priority
Network	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch UEFI Legacy	Controls the execution of UEFI and Legacy Video OpROM
Other PCI devices	Do not launch UEFI Legacy	Determines the OpROM execution policy for devices other than Network, Storage and Video

4.3.15 NVMe configuration submenu

NVMe Device Options Settings, depend on NVME Devices found in the system.

4.3.16 SDIO configuration submenu

Menu Item	Options	Description
SDIO Access Mode	Auto ADMA SDMA PIO	Auto Option: Access the SD Device in DMA mode if the controller supports it, otherwise in PIO Mode. DMA Option: Access the SD Device in DMA mode ADMA Option: Access the SD Device in Advanced DMA mode PIO Option: Access the SD Device in PIO mode

4.3.17 Main Thermal Configuration submenu

Menu Item	Options	Description
Critical Temperature (°C)	80 / 85 / 90 / 95 / 100 / 105 / 110 / 115 / 120	Above this threshold, an ACPI aware OS will perform a critical shut-down. Allowed range is from 80 to 100, where 120 means disabled.
Passive Cooling Temperature (°C)	60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin lowering the CPU speed. Allowed range is from 60 to 100, where values above Critical Temperature means Disabled.
TC1	0 .. 16	Thermal Constant 1: part of the ACPI Passive Cooling Formula
TC2	0 .. 16	Thermal Constant 2: part of the ACPI Passive Cooling Formula
TSP (seconds)	2 .. 32	Period of temperature sampling when Passive Cooling

4.3.18 LVDS Configuration submenu

Menu Item	Options	Description
LVDS interface	Enabled / Disabled	Enables or Disables the LVDS interface. When enabled all the following parameters will appear
Edid Mode	External / Default / Custom	Select the source (EDID, Extended Display Identification Data) to be used for the internal flat panel. Depending on the setting chosen, only some of the following option or none will appear.
EDID	640x480 / 800x480 / 800x600 / 1024x600/ 1024x768 / 1280x720 / 1280x800/1280x1024 / 1366x768 / 1400x900 / 1600x900/1680x1050 / 1920x1080	Only available when Edid Mode is set to "default". Select a software resolution (EDID settings) to be used for the internal flat panel.
Pixel Clock / 10000	[2500..22400]	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. Allowed range from 2500 (25MHz) to 22400 (224MHz)
Horizontal Active	[1..4095]	Horizontal Addressable Video in pixels, a.k.a. Horizontal resolution (e.g. 1024 on a 1024x768 LFP)
Horizontal Blank	[1..4095]	Horizontal Blanking in pixels, equals to Horizontal Total (Horizontal Active + Horizontal Front Porch + Horizontal Black Porch)
Vertical Active	[1..4095]	Vertical Addressable Video in pixels, a.k.a. Vertical resolution (e.g. 768 on a 1024x768 LFP)
Vertical Blank	[1..4095]	Vertical Blanking in pixels, equals to Vertical Total (Vertical Active + Vertical Front Porch + Vertical Black Porch)
Horizontal Offset	[1..1023]	Horizontal Front Porch in pixels
Horizontal Pulse	[1..1023]	Horizontal Sync Pulse Width in pixels
Vertical Offset	[1..63]	Vertical Front Porch in pixels
Vertical Pulse	[1..63]	Vertical Sync Pulse Width in pixels
Horizontal Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Vertical Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
LFP DE Polarity	Active High Active Low	Data Enable Polarity
LFP V-Sync Polarity	Positive / Negative	Vertical Sync Polarity
LFP H-Sync Polarity	Positive / Negative	Horizontal Sync Polarity

Color Mode	VESA 24bpp / JEIDA 24bpp / 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
Interface	Single Channel / Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LVDS Advanced Options	See Submenu	LVDS Advanced Options Configurations

4.3.18.1 LVDS Advanced options submenu

Menu Item	Options	Description
Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)

4.3.19 SMBIOS Information

Display only screen, shows information about the module and the Carrier board.

4.3.20 Embedded Controller submenu

Menu Item	Options	Description
Hardware Monitor		By selecting this item, and information screen with System parameters will appear
Watchdog configuration	See Submenu	Configures the Embedded Controller's Watchdog Timer
Internal FAN Settings	See Submenu	Sets the parameters for Internal (i.e. on-module) FAN
External FAN/PWM Settings	See Submenu	Sets the parameters for external (i.e. on-carrier FAN
COM–Express GPIO/SD Selection	GPIO / SD Card	Select GPIO or SD Card interface on multiplexed PIN functions
COM-Express GPIO Configurations	See Submenu	Only selectable when GPIO/SD Card Selection is set to GPIO. Configures GPOs management
Reset Causes Handling		By selecting this item, an information screen with the handling of latest resets causes will appear.
Batteryless Operation	Disabled / Enabled	Enable this item in case the CMOS Battery is not present.
Power Fail resume Type	Always ON Always OFF Last State	Specifies what must happen when power is re-applied after a power failure (G3 state). Always ON: the System will boot directly as soon as the power is applied. Always OFF: the system remain in power off State until power button is pressed
LID# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configures the LID_BTN# signal as always open or closed, no matter the pin level, or configures the pin polarity: High = Open (Normal), Low = Open (Inverted)
LID# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	Configures LID_BTN# wake capability (when not forced to Open or Closed). According to the pin configuration, when the LID is open it can cause a system wake from a sleep state.
SLEEP# Wake	Disabled / Enabled	Disable or Enable SLEEP# Wake capability from S3/S4 state.
SMB_ALERT# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	Configures SMB_ALERT# wake capability: when asserted, it can cause the system wake from a sleep state.
GPIO/SD Card Selection	GPIO SD Card	Select GPIO/SD Card multiplexed PIN Function
PEG Lane Strap Configuration	1x16 2x8 1x8 + 2 x4	Allow selecting how the PCI Express Graphics (PEG) x16 lanes must be managed. Allowed configurations are: a single port x16 (default), 2 ports x8 or 1 port x8 plus 2 ports x 4

4.3.20.1 Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Disabled / Enabled	Enables or disables the Watchdog.. When disabled, all following items will disappear.
Event action	System Reset Power Button Pulse None	Action executed at the expiring of the Event time-out.
Reset action	System Reset Power Button Override Raise WDT Signal	Action executed at the expiring of the reset time-out.
Watchdog Delay	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	Minutes before watchdog normal operations start. During delay time-out, a refresh operation will immediately trigger the normal operation.
Event Timeout	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	Time-out minutes that can pass without refresh before triggering the Event Action. A refresh will restart the time-out.
Reset Timeout	1 / 2 / 4 / 8 / 16 / 32 / 64	Time-out minutes that can pass without refresh before triggering the Reset Action, this timer will start counting when event time-out is expired.. A refresh will restart the time-out.

4.3.20.2 Internal FAN Settings submenu

Menu Item	Options	Description
Internal FAN Control	Enabled / Disabled	Disable or Enable Thermal Feedback FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Internal FAN Control" is Enabled Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Internal FAN Control" is Enabled. Select the lowest temperature under which the onboard fan must be OFF.
Temperature Hysteresis	0 .. 10	Only available when "Internal FAN Control" is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when "Internal FAN Control" is Enabled. Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed.
FAN Duty Cycle (%) Above AC0	0 .. 100	Only available when "Internal FAN Control" is Enabled. Use this item to set the Duty Cycle for the fan when the CPU temperature is above AC0 threshold.
Speed Change Duration	0 .. 50	Only available when "Internal FAN Control" is Enabled. Duration in seconds of linear FAN Speed Change.
FAN Duty Cycle	0 .. 100	Only available when "Internal FAN Control" is Disabled. Default FAN Duty Cycle (%).

4.3.20.3 External FAN/PWM Settings submenu

Menu Item	Options	Description
FAN_PWMOUT Type	3-Wire FAN 4-Wire FAN Generic PWM	Specifies if a 3-Wire (Default) or a 4-Wire FAN is connected to FAN_PWMOUT / FAN_TACHOIN signals. Generic PWM has to be used when the signal is not used to drive a FAN.
FAN_PWMOUT frequency	1 .. 60.000	Sets the frequency of the FAN_PWMOUT signal. If fed to a FAN, typical values are 100 for a 3-Wire device and 20.000 for a 4-Wire one.
External FAN Control	Enabled / Disabled	Only available when "External FAN Type" is not set to Generic PWM. Disable or Enable Thermal Feedback FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "External FAN Control" is Enabled Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "External FAN Control" is Enabled. Select the lowest temperature under which the onboard fan must be OFF.
Temperature Hysteresis	0 .. 10	Only available when "External FAN Control" is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when "External FAN Control" is Enabled. Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed.
Speed Change Duration	0 .. 50	Only available when "External FAN Control" is Enabled. Duration in seconds of linear FAN Speed Change.
FAN Duty Cycle (%)	0 .. 100	Only available when "External FAN Type" is not set to Generic PWM and External FAN Control is Disabled. Default FAN Duty Cycle (%)
FAN_PWMOUT Duty Cycle (%)	0 .. 100	Only available when "External FAN Type" is set to Generic PWM. Default FAN_PWMOUT Duty Cycle (%) during boot

4.3.20.4 COM-Express GPIO Configurations submenu

Menu Item	Options	Description
GPO0 GPO1 GPO2 GPO3	Low High Last	Fix the GPOx starting level. Last means no change with respect to the last boot.

4.3.21 Tls Auth Configuration submenu

Menu Item	Options	Description
Server CA Configuration	See Submenu	Press <Enter> to configure Server CA

4.3.21.1 Server CA Configuration submenu

Menu Item	Options	Description
Enroll Cert	See Submenu	By entering this submenu it will be possible to enrol the certificate
Delete Cert	See Submenu	By entering this submenu it will be possible to delete selected certificate

4.3.21.1.1 Enroll Cert submenu

Menu Item	Options	Description
Enroll Cert Using File		This option will open the file explorer, which will allow to select the file containing the Certificate
Cert GUID		This option will allow entering manually the certificate in the format 11111111-2222-3333-4444-1234567890ab
Commit changes and exit		Commit changes and exit
Discard Changes and exit		Discard Changes and exit

4.4 Chipset menu

Menu Item	Options	Description
System Agent (SA) Configuration	See Submenu	System Agent (SA) Parameters
PCH-IO Configuration	See Submenu	PCH Parameters

4.4.1 System Agent (SA) Configuration submenu

Menu Item	Options	Description
Memory Configuration		Memory Configuration Parameters. Visualization only
Graphics Configuration	See Submenu	Graphics Configruation
PEG Port Configuration	See Submenu	PEG Port Options

4.4.1.1 Graphics Configuration submenu

Menu Item	Options	Description
Primary Display	AUTO / IGFX / PEG / PCI	Select which between the IGFX (internal Graphics), PEG or PCI Graphics Device should be the Primary Display
Internal Graphics	Auto / Disabled / Enabled	Keep IGFx Enabled or not, depending on the Setup options
GTT Size	2MB / 4MB / 8MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	128MB / 256MB / 512MB / 1024MB / 2048MB	Use this item to set the total size of Memory that must be left to the GFX Engine
DVMT Pre-Allocated	0M / 32M / 64M / 4M / 8M / 12M / 16M / 20M / 24M / 28M / 32MF7 / 36M / 40M / 44M / 48M / 52M / 56M / 60M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use

4.4.1.2 PEG Port Configuration submenu

All the following items will be replied for all the possible available ports, depending on the settings made in Advanced Menu → Embedded controller Menu → PEG Lane Strap Configuration item (see par. 4.3.20)

Menu Item	Options	Description
Enable Root port	Auto / Disabled / Enabled	Enable or Disable the single Root port
Max Link Speed	Auto / Gen1 / Gen2 / Gen3	Configure PEGx port Max Speed
PEGx Slot Power Limit Value	0..255	Sets the upper limit on power supplied by the slot. Power limit in Watts is calculated by multiplying this value by the Slot Power Limit Scale
PEGx Slot Power Limit Scale	1.0x 0.1x 0.01x 0.001x	Select the Scale used for the Slot Power Limit Value
PEGx Physical Slot Number	0..8191	Sets the physical slot number attached to this Port, the number has to be unique within the chassis.
PEGx Hotplug	Enabled / Disabled	Enable or Disable the PEG Root Port x Hotplug capability, Available only if corresponding PEGx port is not set to Auto

4.4.2 PCH-IO Configuration submenu

Menu Item	Options	Description
PCI Express Configuration	See submenu	PCI Express Configuration Settings
SATA and RST Configuration	See submenu	SATA Devices Options Settings
USB Configuration	See submenu	USB configuration Settings
HD Audio Configuration	See submenu	HD Audio Configuration Settings
SerialIO Configuration	See submenu	Serial IO Configuration Settings
PCH LAN Controller	Enabled / Disabled	Enable or Disable the on-board NIC
Wake on LAN Enable	Enabled Disabled	Only Available when PCH LAN Controller is Enabled. Allows enabling or disabling the LAN capability to wake the system
Serial IRQ Mode	Quiet Continuous	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.
Port 80h redirection	LPC Bus PCIe Bus	Set the destination of Port 80h messages

4.4.2.1 PCI Express Configuration submenu

Menu Item	Options	Description
Compliance Test Mode	Enabled / Disabled	Compliance Mode Enable/Disable
COM Express PCIE0 COM Express PCIE1 COM Express PCIE2 COM Express PCIE3 COM Express PCIE4 COM Express PCIE5 COM Express PCIE6 COM Express PCIE7	See Submenu	Sets the parameters for each single PCI-e Root Port

4.4.2.1.1 PCIE Port #x submenus

Menu Item	Options	Description
COM-Express PCIEx	Enabled / Disabled	Enable or disable each single PCI-e port. When enabled, all following items will appear.
ASPM	Disable / L0s	Disable or Enable PCI Express Active State Power Management
Hot Plug	Enabled / Disabled	Enable/Disable PCI Express Hot Plug capability
Speed	Auto / Gen1 / Gen2 / Gen3	Configure PCIe Speed

4.4.2.2 SATA and RST Configuration submenu

Menu Item	Options	Description
SATA Controller(s)	Enabled / Disabled	Enables or Disables the Chipset SATA controller, which supports the 4 SATA ports available on COM Express connector AB (up to 6.0Gbps supported per port).
SATA Mode Selection	AHCI Intel RST Premium with Intel Optane System Acceleration	Determines how SATA controller operates. Use AHCI for standard SATA functionalities. Use Intel RST Premium (Rapid Store Technology) when RAID functionalities are required
Sata Interrupt Selection	Msix / Msi / Legacy	Select which interrupt will be available to the OS. This option only takes effect is SATA controller is in RAID mode
COM-Express SATA0 COM-Express SATA1 COM-Express SATA2 COM-Express SATA3	Enabled / Disabled	Enable / Disable SATA Port #x
Hot Plug	Enabled / Disabled	This item is available for every SATA Port. If enabled, the corresponding SATA port will be reported as Hot Plug Capable
SATA Device Type	Hard Disk Drive Solid State Drive	Identify if the SATA port is connected to a SSD or HDD

4.4.2.3 USB Configuration submenu

Menu Item	Options	Description
xHCI Compliance Mode	Enable / Disable	Enables or Disable the Compliance Mode.
USB Port Disable Override	Disabled Select per-Pin	Allows enabling or disabling selectively each single USB port from reporting a device connection to the controller.
COM-Express USB_SS0 COM-Express USB_SS1 COM-Express USB_SS2 COM-Express USB_SS3 COM-Express USB0 COM-Express USB1 COM-Express USB2 COM-Express USB3 COM-Express USB4 COM-Express USB5 COM-Express USB6 COM-Express USB7	Disable Enabled	Enables or disables the single USB Port #x. Once disabled, any USB device connected to the corresponding port will not be detected by the BIOS neither by the OS

4.4.2.4 HD Audio Configuration submenu

Menu Item	Options	Description
HD Audio	Disabled / Enabled	Controls the detection of the HD Audio Controller Disabled: the Audio controller will be unconditionally Disabled Enabled: the Audio controller will be unconditionally Enabled
iDisplay Audio	Disabled / Enabled	Available only when "HD Audio" is Enabled Disconnect SDI2 Signal to hide/disable iDisplay Audio Codec

4.4.2.5 Seriallo Configuration submenu

Menu Item	Options	Description
HSUART0 HSUART1	Enabled / Disabled	Enables or Disables the Seriallo Controller
GPIO IRQ Route	IRQ14 / IRQ15	Route all GPIOs to one of the IRQ.

4.5 Security menu

Menu Item	Options	Description
Administrator Password		Set Administrator Password
User Password		Set User Password
Secure Boot	See Submenu	Customizable Secure Boot Settings

4.5.1 Secure Boot submenu

Menu Item	Options	Description
Secure Boot	Enabled / Disabled	Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled.
Secure Boot Mode	Standard / Custom	Set UEFI Secure Boot Mode to Standard Mode or Custom mode. In Custom Mode, Secure Boot Policy variables can be configured by a physically present user without full authentication
Restore Factory Keys		Only accessible when Secure Boot Mode is set to Custom Force System to User Mode. Install Factory default Secure Boot key databases.
Key management	See submenu	Only accessible when Secure Boot Mode is set to Custom Enable expert users to modify Secure Boot Policy variables without full authentication

4.5.1.1 Key Management submenu

Menu Item	Options	Description
Factory Key Provision	Disabled / Enabled	Install factory default Secure Boot Keys after the platform reset and while the System is in Setup Mode
Restore Factory Keys		Force System to User Mode. Install factory Default Secure Boot key databases
Reset to Setup Mode		Delete all Secure Boot key databases from NVRAM
Export Secure Boot variables		Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device
Enrol Efi Image	*File System Image*	Allow the selected image to run in Secure Boot mode. Enrol SHA256 Hash Certificates of a PE Image into Authorized Signature Database (db)
Remove 'UEFI CA' from DB		Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature Database (db)
Restore DB defaults		Restore DB variable to factory defaults
Platform key Key Exchange Keys Authorized Signatures Forbidden Signatures Authorized Timestamps OS Recovery Signatures	Update Append	Enrol factory Defaults or load certificates from a file: 1. Public Key Certificate in: a) EFI_SIGNATURE_LIST b) EFI_CERT_X509 (DER) c) EFI_CERT_RSA2048 (bin) d) EFI_CERT_SHAXX 2. Authenticated UEFI variables 3. EFI PE/COFF Image (SHA256) Key Source: Default, External, Mixed

4.6 Boot menu

Menu Item	Options	Description
Setup Prompt Timeout	0 .. 65535	Number of seconds to wait for setup activation key. 655535 means indefinite waiting.
Bootup NumLock State	On / Off	Select the Keyboard NumLock State at boot
Quiet Boot	Enabled / Disabled	Enables or Disables Quiet Boot options
Fast Boot	Enabled / Disabled	When Fast Boot is enabled, most probes are skipped to reduce time cost during boot
Boot Mode Select	LEGACY UEFI	Select the boot mode between Legacy and UEFI
Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4 Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8 Boot Option #9	Hard Disk CD/DVD SD USB Hard Disk USB CD/DVD USB key USB Floppy USB LAN Network Disabled	Select the system boot order
UEFI Hard Disk BSB priorities	*List of UEFI bootable drives*	Specifies the Boot Device Priority Sequence from available UEFI Hard Disk Drives
UEFI Other Drive BBS Priorities	*List of other UEFI drives*	Specifies the Boot Device Priority Sequence from available UEFI Other Drives

!

Please be aware that by default only UEFI boot is enabled. In this situation, when using legacy MBR drives, the system will not boot from them. To fully enable the boot form legacy drives, it is necessary to set the following items:

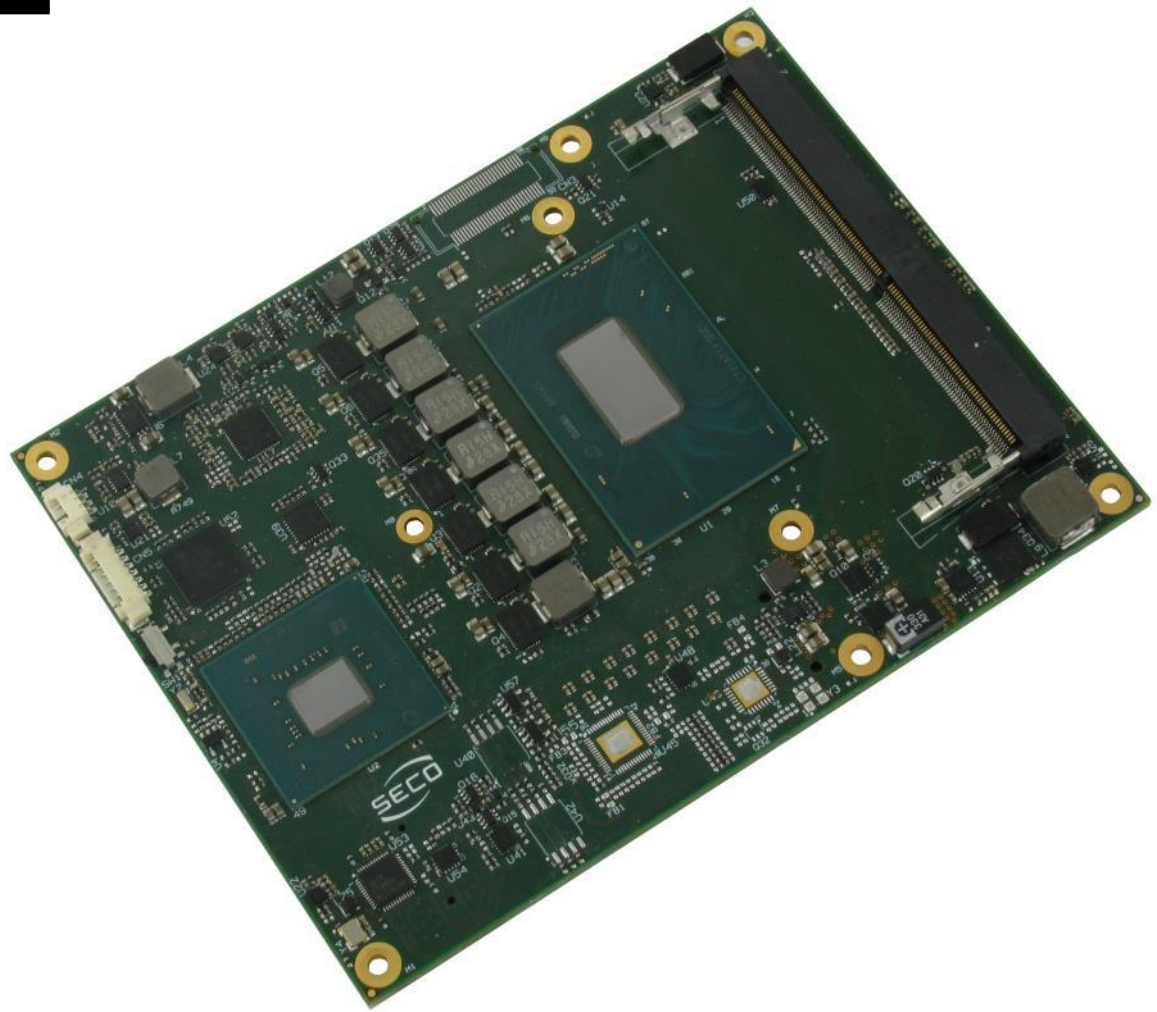
- Boot menu → "Boot mode select": must be set to Legacy
- Advanced menu → CSM Configuration submenu → "CSM support" must be Enabled
- Advanced menu → CSM Configuration submenu → "Video" must be set to Legacy

4.7 Save & Exit menu

Menu Item	Options	Description
Save Changes and Exit		Exit system setup after saving the changes.
Discard Changes and Exit		Exit system setup without saving any changes.
Save Changes and Reset		Reset the system after saving the changes.
Discard Changes and Reset		Reset the system without saving any changes.
Save Changes		Save the changes done so far to any of the setup options.
Discard Changes		Discard the changes done so far to any of the setup options.
Restore Defaults		Restore/Load Default values for all the setup options
Save as User Defaults		Save the changes done so far as User Defaults
Restore User Defaults		Restore the User Defaults to all the setup options
List of EFI boot options		
Launch EFI Shell from filesystem device		Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices

Chapter 5.
Appendices

- Thermal Design



5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-C08-BT6 module, offer to the user very good performances in minimal spaces, therefore allowing the system's minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-C08-BT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-C08-BT6 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions. Please ask SECO for specific ordering codes.

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