# Com express

User Manual


# COMe-B75 CT6

COM-Express™ Type 6 Module with the
AMD Ryzen™ Embedded V1000 Processors

# REVISION HISTORY

| Revision | Date | Note | Rif |
|---|---|---|---|
| 1.0 | 16 October 2018 | First Release | SB |
| 1.1 | 29 October 2018 | Factory restore switch documentation added<br>Memory specifications updated in par. 2.2 only<br>Errors corrected in paragraph 4.3.21.3 | SB |
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Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

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# Chapter 1.
# INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

## 1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

**Warning!**
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

## 1.2 Information and assistance

**What do I have to do if the product is faulty?**

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434

- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

**Note: Please have the following information before asking for technical assistance:**

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

## 1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

## 1.4 Safety

The COMe-B75-CT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

## 1.5 Electrostatic Discharges

The COMe-B75-CT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling a COME-B75-CT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

## 1.6 RoHS compliance

The COMe-B75-CT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

## 1.7 Terminology and definitions

| | |
|---|---|
| ACPI | Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management |
| AHCI | Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface |
| API | Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems |
| BIOS | Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading |
| DDC | Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU) |
| DDR | Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock |
| DDR4 | DDR, 4th generation |
| DP | Display Port, a type of digital video display interface |
| DVI | Digital Visual interface, a type of digital video display interface |
| eDP | embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays |
| GbE | Gigabit Ethernet |
| Gbps | Gigabits per second |
| GT/s | Gigatransfers per second |
| GND | Ground |
| GPI/O | General purpose Input/Output |
| HD Audio | High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality |
| HDMI | High Definition Multimedia Interface, a digital audio and video interface |
| I2C Bus | Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability |
| LPC Bus | Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals |
| LVDS | Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications |
| Mbps | Megabits per second |
| N.A. | Not Applicable |
| N.C. | Not Connected |
| OS | Operating System |
| PCI-e | Peripheral Component Interface Express |
| PSU | Power Supply Unit |

| | |
|---|---|
| PWM | Pulse Width Modulation |
| PWR | Power |
| PXE | Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS |
| SATA | Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks |
| SD | Secure Digital, a memory card type |
| SDHC | Secure Digital Host Controller |
| SDIO | Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on |
| SM Bus | System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like smart batteries and other power supply-related devices |
| SPI | Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line |
| TBM | To be measured |
| TMDS | Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces |
| TTL | Transistor-transistor Logic |
| UEFI | Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface |
| UMA | Unified Memory Architecture, synonym of Integrated Graphics, uses a portion of a computer's system RAM dedicated to graphics rather than using dedicated graphics memory only. |
| USB | Universal Serial Bus |
| V_REF | Voltage reference Pin |
| xHCI | eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports |

## 1.8 Reference specifications

| Reference | Link |
|---|---|
| ACPI | http://www.uefi.org/acpi/specs |
| AHCI | http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html |
| Com Express | https://www.picmg.org/openstandards/com-express/ |
| Com Express Carrier Design Guide | http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf |
| DDC | http://www.vesa.org |
| DP, eDP | http://www.vesa.org |
| Gigabit Ethernet | http://standards.ieee.org/about/get/802/802.3.html |
| HD Audio | http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf |
| HDMI | http://www.hdmi.org/index.aspx |
| I2C | http://cache.nxp.com/documents/user_manual/UM10204.pdf?fsrch=1&sr=5&pageNum=1 |
| LPC Bus | http://www.intel.com/design/chipsets/industry/lpc.htm |
| LVDS | http://www.ti.com/ww/en/analog/interface/lvds.shtml<br>http://www.ti.com/lit/ml/snla187/snla187.pdf |
| PCI Express | http://www.pcisig.com/specifications/pciexpress |
| SATA | https://www.sata-io.org |
| SD Card Association | https://www.sdcard.org |
| SM Bus | http://www.smbus.org/specs |
| UEFI | http://www.uefi.org |
| USB 2.0 | http://www.usb.org/developers/docs/usb20_docs/usb_20_040816.zip |
| USB 3.0 | http://www.usb.org/developers/docs/usb_30_spec_070113.zip |
| xHCI | http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html?wapkw=xhci |
| AMD Ryzen™ Embedded V1000 | https://www.amd.com/en/products/embedded-ryzen-v1000-series |

# Chapter 2.
# OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

## 2.1 Introduction

The COMe-B75-CT6 is a COM Express® type 6, Compact Form Factor, based on the AMD Ryzen™ Embedded V1000 processors. A complete list of processors available is detailed in the next chapter.

All of these SoCs are Dual- or Quad-Core, Dual Thread, offer a 64-bit Instruction set and provide direct access to the memory, which is available on two DDR4 SODIMM memory modules (speed up to 3200). Both ECC and non-ECC memory modules are supported. The total amount of memory available is OS dependant.

All SoCs integrate an AMD Radeon™ Vega x GPU with up to 11 Compute Untis, which offer an advanced 2D and 3D graphic engine, able to manage up to 4 independent displays using the native Digital Display Interfaces (DDIs), the eDP interface and/or the PCI-e Graphics (PEG) x8 interface. On all DDIs, it is possible to support DP++ 1.3, DVI, HDMI 1.4 / 2.0 interfaces. As factory options, it is possible to have also one LVDS interface by using a dedicated bridge placed on native eDP inetrface.

Further graphical possibilities are given by the SoC's PCI Express graphics (PEG) x8 interface. Such an interface can be used as a single PCI-e x8 port or two PCI-e x 4 independent ports.

All the SoCs available on this module offer five PCI-express x 1 Gen 3 ports; four of them are carried out externally, the other port can be used to manage directly a Gigabit Ethernet controller, or carried to an optional PCI-Express switch, which would switch the upstream port to the Ethernet controller and to two further Com Express connector's PCI-e Gen2 ports.

The module functionalities are completed by the Audio HD Interface, 2 x Serial ATA Gen3 channels, 8 USB 2.0 ports, 4 USB 3.0 ports, 2 UARTs, 4 GPIs and 4 GPOs, Real Time Clock, LPC and SM Bus.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.3.0 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available.

Specifically, COMe-B75-CT6 is a COM Express® module, Compact Form factor, Type 6 (95mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilise as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

# 2.2 Technical Specifications

**Processor**

AMD Ryzen™ Embedded **V1807B** with AMD Radeon™ Vega 11 Graphics, Quad Core Dual Thread @ 3.35GHz (3.8 Boost), TDP 35-54W
AMD Ryzen™ Embedded **V1756B** with AMD Radeon™ Vega 5 Graphics, Quad Core Dual Thread @ 3.25GHz (3.6 Boost), TDP 35-54W
AMD Ryzen™ Embedded **V1605B** with AMD Radeon™ Vega 5 Graphics, Quad Core Dual Thread @ 2.0GHz (3.6 Boost), TDP 12-25W
AMD Ryzen™ Embedded **V1208B** with AMD Radeon™ Vega 3 Graphics, Dual Core Dual Thread @ 2.3GHz (3.2 Boost), TDP 12-25W

AMD Ryzen™ Embedded **V1404I** with AMD Radeon™ Vega 3 Graphics, Quad Core / Single Thread, TDP 15W ,Industrial Temperature range

**Memory**

Two SO-DIMM slots supporting DDR4-3200 Single Rank / DDR4-2667 Dual Rank modules (DDR4-2400 with V1605B, V1202B and V1404I).
ECC and non-ECC modules supported.

**Graphics**

AMD Radeon™ Vega GPU with up to 11 Compute Units
4 independent displays supported
DirectX® 12, EGL 1.4, OpenCL™ 2.1, OpenGL® ES 1.1/ 2.x / 3.x (Halti), OpenGL® Next (Vulkan®), OpenGL® 4.6 supported
H.265 (10-bit) decode and 8-bit video encode
VP9 decode

**Video Interfaces**

3 x Digital Display interfaces, supporting DP 1.3, DVI and HDMI 1.4 / 2.0
eDP **or** Single / Dual-Channel 18- / 24- bit LVDS interface

**Video Resolutions**

| | |
|---|---|
| Digital Display interfaces: | up to 4K |
| LVDS: | up to 1920 x 1200 |

**Mass Storage**

2 x S-ATA Gen3 channels

**USB**

8 x USB 2.0 Host Ports
4 x USB 3.0 Host ports

**Networking**

Gigabit Ethernet interface
Intel® I210 or I211 GbE controller

**Audio**

HD Audio interface

**PCI Express**

Up to 4 x PCI-e x1 Gen3 lanes + 2 x PCI-e x1 Gen2 ports
PCI-express Graphics (PEG) x 8 Gen3

**Serial Ports**

2 x UARTs

**Other Interfaces**

I2C bus
LPC Bus
SM Bus
4 x GPI, 4 x GPO
Thermal / FAN management
SPI Interface
Watch Dog timer
Real Time Clock
Power Management Signals

**Power supply voltage:** +12$V_{DC}$ ± 10% and + 5$V_{SB}$ (optional)

**Operating temperature:** 0°C ÷ +60°C (commercial temperature range)**
-40°C÷+85°C (industrial temperature range)**

**Dimensions:** 95 x 95 mm (3.74" x 3.74")

**!** *** Temperatures indicated (minimum and maximum) are those measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated. Please also check paragraph 5.1*

## 2.3 Electrical Specifications

According to COM Express® specifications, the COMe-B75-CT6 board needs to be supplied only with an external +12$V_{DC}$ power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN6 and CN7.

All remaining voltages needed for board's working are generated internally from +12$V_{DC}$ power rail.

### 2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: RUN voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

_SUS: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_SUS

### 2.3.2 Power Consumption

COMe-B75-CT6 module, like all COM Express™ modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Therefore, power consumptions of the board are measured using a CCOMe-965 Carrier board on +12V_RUN power rail that supplies the board. For this reason, the values indicated in the table below are real power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board.

Power consumption in Suspend and Soft-Off States have been measured on +5V_ALW power rail. RTC power consumption has been measured on carrier board's backup battery when the system is not powered (VCC_RTC power rail).

The current consumptions, written in the table of this page, have been measured using the following setup:

- O.S. Windows 10
- 16GB DDR4 (2 x 8GB SO-DIMM DDR4 2400MHz modules, p/n G.SKILL F4-3200C16D-16GRS)
- 256GB SATA Gen3 SSD (p/n SSD370S) connected
- USB mouse and keyboard connected
- HDMI display connected.

Power consumptions common to all SOCs:

| | |
|---|---|
| Suspend to RAM (Typical): | 110mA |
| Soft-Off (Typical) | 67mA |

| Status | SoC V1202B | | | | | |
|---|---|---|---|---|---|---|
| | TDP 12W | | TDP 15W | | TDP 25W | |
| | Average | Peak | Average | Peak | Average | Peak |
| Idle, power saving configuration | 0,567A | 0,863A | 0,534A | 0,904A | 0,558A | 1,068A |
| OS Boot, power saving configuration | 1,606A | 2,927A | 1,585A | 3,045A | 1,574A | 2,977A |
| Video reproduction@ 4K, power saving configuration | 0,984A | 1,500A | 1,050A | 1,645A | 1,048A | 1,605A |
| Internal Stress Test Tool, maximum performance | 2,568A | 3,241A | 2,723A | 3,705A | 3,392A | 3,770A |

| Status | SoC V1605B | | | | | |
|---|---|---|---|---|---|---|
| | TDP 12W | | TDP 15W | | TDP 25W | |
| | Average | Peak | Average | Peak | Average | Peak |
| Idle, power saving configuration | 0,524A | 0,635A | 0,528A | 0,866A | 0,552A | 0,882A |
| OS Boot, power saving configuration | 1,672A | 3,052A | 1,742A | 3,010A | 1,755A | 3,293A |
| Video reproduction@ 4K, power saving configuration | 0,852A | 1,295A | 0,819A | 1,326A | 0,865A | 1,393A |
| Internal Stress Test Tool, maximum performance | 2,837A | 3,330A | 3,083A | 4,010A | 3,363A | 4,274A |

| Status | SoC V1756B | | | | | |
|---|---|---|---|---|---|---|
| | TDP 35W | | TDP 45W | | TDP 54W | |
| | Average | Peak | Average | Peak | Average | Peak |
| Idle, power saving configuration | TBM | TBM | TBM | TBM | TBM | TBM |
| OS Boot, power saving configuration | TBM | TBM | TBM | TBM | TBM | TBM |
| Video reproduction@ 4K, power saving configuration | TBM | TBM | TBM | TBM | TBM | TBM |
| Internal Stress Test Tool, maximum performance | TBM | TBM | TBM | TBM | TBM | TBM |

| Status | SoC V1807B | | | | | |
|---|---|---|---|---|---|---|
| | TDP 35W | | TDP 45W | | TDP 54W | |
| | Average | Peak | Average | Peak | Average | Peak |
| Idle, power saving configuration | 0,561A | 1,076A | 0,546A | 1,102A | 0,550A | 1,128A |
| OS Boot, power saving configuration | 1,734A | 4,295A | 1,772A | 5,210A | 2,014A | 5,177A |
| Video reproduction@ 4K, power saving configuration | 1,035A | 1,480A | 1,076A | 1,553A | 1,079A | 1,627A |
| Internal Stress Test Tool, maximum performance | 4,528A | 6,333A | 4,739A | 6,861A | 5,096A | 6,858A |

## 2.4 Mechanical Specifications

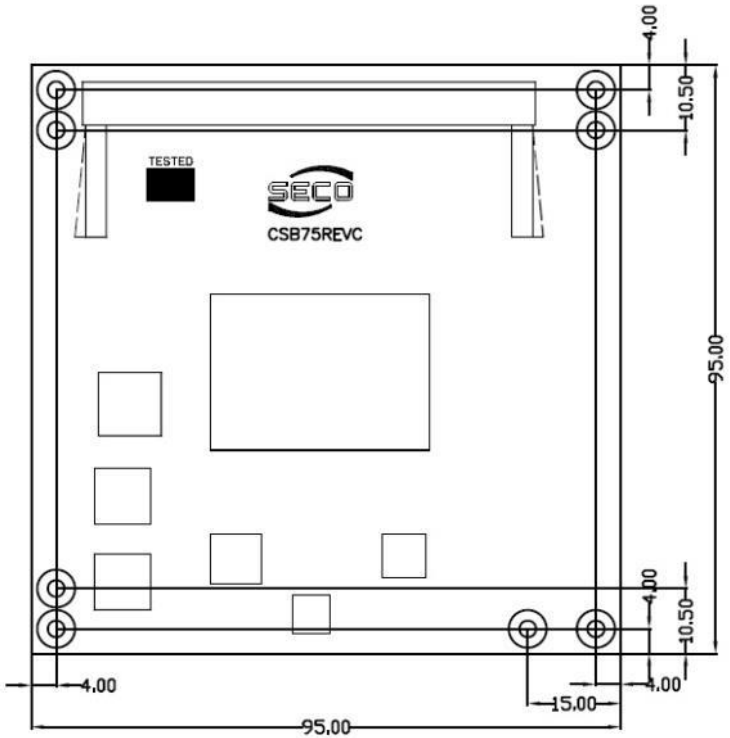
The COMe-B75-CT6 is a COM Express board, Compact form Factor type; therefore its dimensions are 95 mm x 95 mm (3.74” x 3.74”).

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

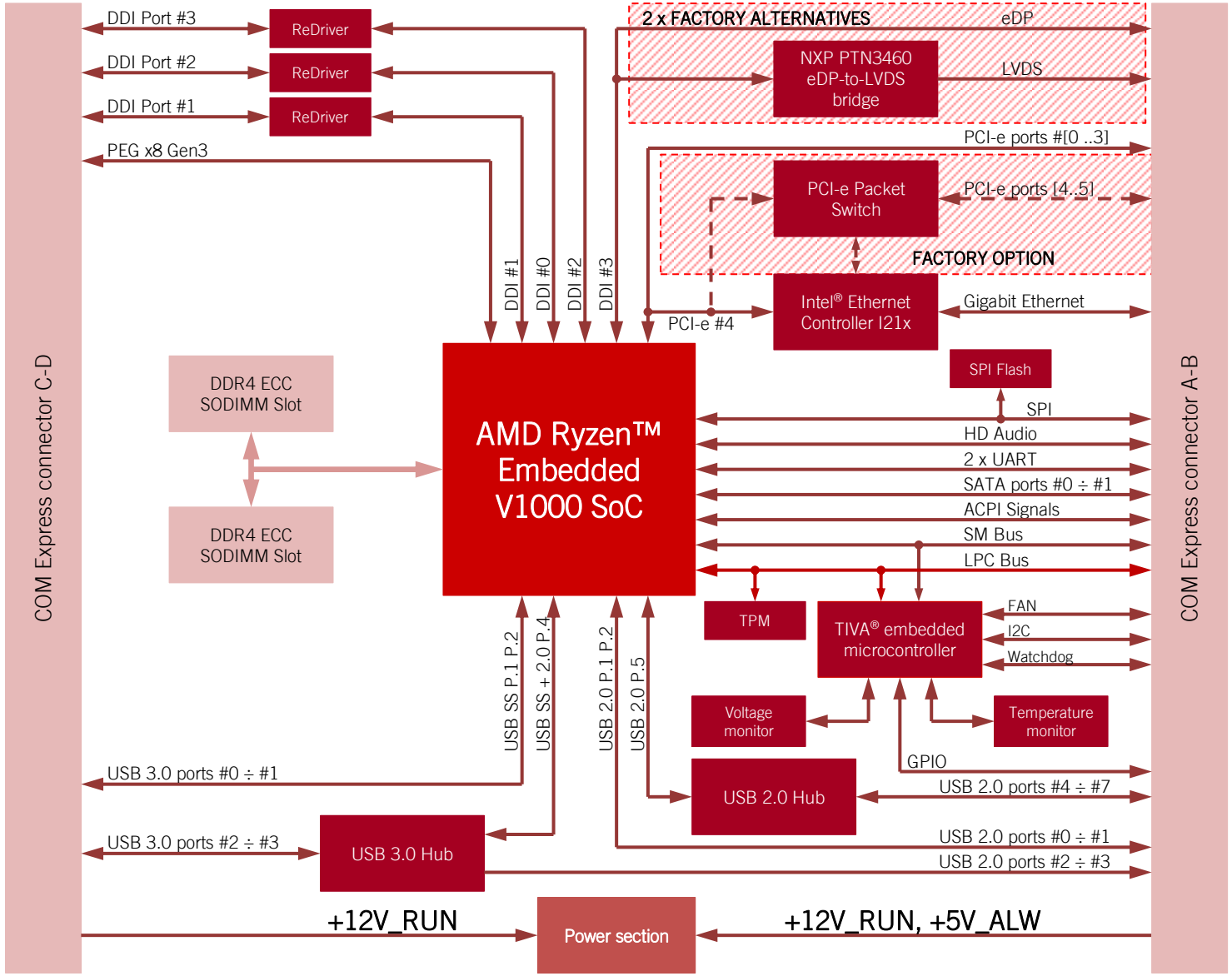
According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector’s height is chosen, in designing a custom carrier board please remember that the SO-DIMM connector placed on the bottom side of COMe-B75-CT6 will have a maximum height of 4mm.

This value must be kept in high consideration when choosing the carrier board plugs’ height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.



# 2.5 Block Diagram



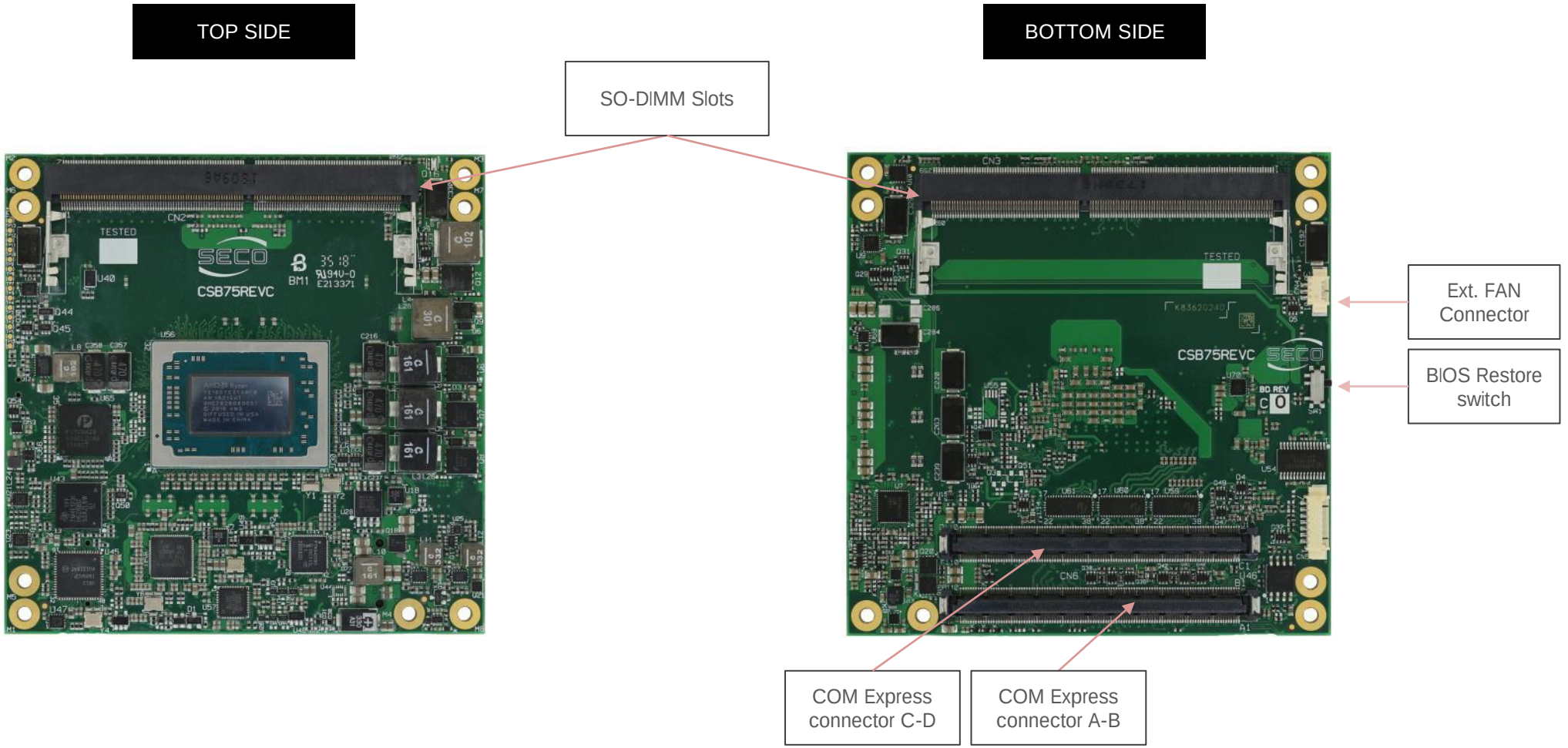
# Chapter 3.
# CONNECTORS

- Introduction
- Connectors description

# 3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.



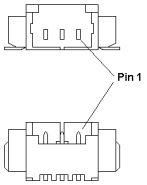
# 3.2 Connectors description

## 3.2.1 FAN Connector

| FAN Connector – CN4 | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | FAN_POWER |
| 3 | FAN_TACHO_IN |

Depending on the usage model of COMe-B75-CT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12$V_{DC}$ FAN.

FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.




Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_RUN derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_RUN electrical level signal with 10kΩ pull-up resistor.

## 3.2.2 SO-DIMM DDR4 Slots

CPUs used on the COMe-B75-CT6 board provide support to DDR4 SO-DIMM memory modules. Both ECC and non-ECC modules are supported.

V1807B and V1756B can support up to DDR-3200 Single Rank modules or DDR4-2667 Dual Rank SO-DIMM modules, while V1605B and V1202B can support up to DDR4-2400 DO-DIMM modules.

For use of this memories, on board there are two SO-DIMM DDR4 slots.

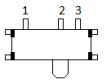
The socket placed on top side (CN2) is type LOTES p/n ADDR0208-P003A or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications.

The socket placed on bottom side (CN3) is type LOTES p/n ADDR0205-P003A or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support to dual channel memories.

## 3.2.3 BIOS Restore switch

In some cases, a wrong configuration of BIOS parameters could lead the module in an unusable state (i.e. no video output, all USB HID devices disabled).

For these cases, on the module it has been placed a 3-way switch which can be used to restore the BIOS to factory default configuration. To do so, it is necessary to place the contact of the switch in 1-2 position, then turn on the module, wait until the board resets itself then turn off the module. The contact MUST be now placed back to 2-3 position.




During normal use, the contact MUST be always placed in 2-3 position.

### 3.2.4 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-B75-CT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

| COM Express® Connector AB - CN6 | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | ROW A | | | ROW B | | |
| SIGNAL GROUP | Type | Pin name | Pin nr. | Pin nr. | Pin name | Type | SIGNAL GROUP |
| | PWR | GND | A1 | B1 | GND | PWR | |
| GBE | I/O | GBE0_MDI3- | A2 | B2 | GBE0_ACT# | O | GBE |
| GBE | I/O | GBE0_MDI3+ | A3 | B3 | LPC_FRAME# | O | LPC |
| GBE | O | GBE0_LINK100# | A4 | B4 | LPC_AD0 | I/O | LPC |
| GBE | O | GBE0_LINK1000# | A5 | B5 | LPC_AD1 | I/O | LPC |
| GBE | I/O | GBE0_MDI2- | A6 | B6 | LPC_AD2 | I/O | LPC |
| GBE | I/O | GBE0_MDI2+ | A7 | B7 | LPC_AD3 | I/O | LPC |
| GBE | O | GBE0_LINK# | A8 | B8 | LPC_DRQ0# | I | LPC |
| GBE | I/O | GBE0_MDI1- | A9 | B9 | N.C. | N.A. | |
| GBE | I/O | GBE0_MDI1+ | A10 | B10 | LPC_CLK | O | LPC |
| | PWR | GND | A11 | B11 | GND | PWR | |
| GBE | I/O | GBE0_MDI0- | A12 | B12 | PWRBTN# | I | PWR_MGMT |
| GBE | I/O | GBE0_MDI0+ | A13 | B13 | SMB_CK | I/O | SMBUS |
| | N.A. | N.C. | A14 | B14 | SMB_DAT | I/O | SMBUS |
| PWR_MGMT | O | SUS_S3# | A15 | B15 | SMB_ALERT# | I | SMBUS |
| SATA | O | SATA0_TX+ | A16 | B16 | SATA1_TX+ | O | SATA |
| SATA | O | SATA0_TX- | A17 | B17 | SATA1_TX- | O | SATA |
| PWR_MGMT | O | SUS_S4# | A18 | B18 | SUS_STAT# | O | PWR_MGMT |
| SATA | I | SATA0_RX+ | A19 | B19 | SATA1_RX+ | I | SATA |
| SATA | I | SATA0_RX- | A20 | B20 | SATA1_RX- | I | SATA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | PWR | GND | A21 | B21 | GND | PWR | |
| | N.A. | N.C. | A22 | B22 | N.C. | N.A. | |
| | N.A. | N.C. | A23 | B23 | N.C. | N.A. | |
| PWR_MGMT | O | SUS_S5# | A24 | B24 | PWR_OK | I | PWR_MGMT |
| | N.A. | N.C. | A25 | B25 | N.C. | N.A. | |
| | N.A. | N.C. | A26 | B26 | N.C. | N.A. | |
| PWR_MGMT | I | BATLOW# | A27 | B27 | WDT | O | MISC |
| SATA | O | SATA_ACT# | A28 | B28 | N.C. | N.A. | |
| AUDIO | O | HDA_SYNC | A29 | B29 | HDA_SDIN1 | I/O | AUDIO |
| AUDIO | O | HDA_RST# | A30 | B30 | HDA_SDIN0 | I/O | AUDIO |
| | PWR | GND | A31 | B31 | GND | PWR | |
| AUDIO | I/O | HDA_BITCLK | A32 | B32 | SPKR | O | MISC |
| AUDIO | O | HDA_SDOUT | A33 | B33 | I2C_CK | I/O | I2C |
| SPI | I | BIOS_DIS0# | A34 | B34 | I2C_DAT | I/O | I2C |
| MISC | O | THRMTRIP# | A35 | B35 | THRM# | I | MISC |
| USB | I/O | USB6- | A36 | B36 | USB7- | I/O | USB |
| USB | I/O | USB6+ | A37 | B37 | USB7+ | I/O | USB |
| USB | I | USB_6_7_OC# | A38 | B38 | USB_4_5_OC# | I | USB |
| USB | I/O | USB4- | A39 | B39 | USB5- | I/O | USB |
| USB | I/O | USB4+ | A40 | B40 | USB5+ | I/O | USB |
| | PWR | GND | A41 | B41 | GND | PWR | |
| USB | I/O | USB2- | A42 | B42 | USB3- | I/O | USB |
| USB | I/O | USB2+ | A43 | B43 | USB3+ | I/O | USB |
| USB | I | USB_2_3_OC# | A44 | B44 | USB_0_1_OC# | I | USB |
| USB | I/O | USB0- | A45 | B45 | USB1- | I/O | USB |
| USB | I/O | USB0+ | A46 | B46 | USB1+ | I/O | USB |
| | PWR | VCC_RTC | A47 | B47 | N.C. | N.A. | |
| | N.A. | N.C. | A48 | B48 | N.C. | N.A. | |
| GBE | O | GBE_SPD | A49 | B49 | SYS_RESET# | I | PWR_MGMT |
| LPC | I/O | LPC_SERIRQ | A50 | B50 | CB_RESET# | O | PWR_MGMT |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | PWR | GND | A51 | B51 | GND | PWR | |
| PCIE | O | PCIE_TX5+ | A52 | B52 | PCIE_RX5+ | I | PCIE |
| PCIE | O | PCIE_TX5- | A53 | B53 | PCIE_RX5- | I | PCIE |
| GPIO | I | GPI0 | A54 | B54 | GPO1 | O | GPIO |
| PCIE | O | PCIE_TX4+ | A55 | B55 | PCIE_RX4+ | I | PCIE |
| PCIE | O | PCIE_TX4- | A56 | B56 | PCIE_RX4- | I | PCIE |
| | PWR | GND | A57 | B57 | GPO2 | O | GPIO |
| PCIE | O | PCIE_TX3+ | A58 | B58 | PCIE_RX3+ | I | PCIE |
| PCIE | O | PCIE_TX3- | A59 | B59 | PCIE_RX3- | I | PCIE |
| | PWR | GND | A60 | B60 | GND | PWR | |
| PCIE | O | PCIE_TX2+ | A61 | B61 | PCIE_RX2+ | I | PCIE |
| PCIE | O | PCIE_TX2- | A62 | B62 | PCIE_RX2- | I | PCIE |
| GPIO | I | GPI1 | A63 | B63 | GPO3 | O | GPIO |
| PCIE | O | PCIE_TX1+ | A64 | B64 | PCIE_RX1+ | I | PCIE |
| PCIE | O | PCIE_TX1- | A65 | B65 | PCIE_RX1- | I | PCIE |
| | PWR | GND | A66 | B66 | WAKE0# | I | PWR_MGMT |
| GPIO | I | GPI2 | A67 | B67 | WAKE1# | I | PWR_MGMT |
| PCIE | O | PCIE_TX0+ | A68 | B68 | PCIE_RX0+ | I | PCIE |
| PCIE | O | PCIE_TX0- | A69 | B69 | PCIE_RX0- | I | PCIE |
| | PWR | GND | A70 | B70 | GND | PWR | |
| eDP/LVDS | O | eDP_TX2+ / LVDS_A0+ | A71 | B71 | LVDS_B0+ | O | LVDS |
| eDP/LVDS | O | eDP_TX2- / LVDS_A0- | A72 | B72 | LVDS_B0- | O | LVDS |
| eDP/LVDS | O | eDP_TX1+ / LVDS_A1+ | A73 | B73 | LVDS_B1+ | O | LVDS |
| eDP/LVDS | O | eDP_TX1- / LVDS_A1- | A74 | B74 | LVDS_B1- | O | LVDS |
| eDP/LVDS | O | eDP_TX0+ / LVDS_A2+ | A75 | B75 | LVDS_B2+ | O | LVDS |
| eDP/LVDS | O | eDP_TX0- / LVDS_A2- | A76 | B76 | LVDS_B2- | O | LVDS |
| eDP/LVDS | O | eDP_VDD_EN / LVDS_VDD_EN | A77 | B77 | LVDS_B3+ | O | LVDS |
| LVDS | O | LVDS_A3+ | A78 | B78 | LVDS_B3- | O | LVDS |
| LVDS | O | LVDS_A3- | A79 | B79 | eDP_BKLT_EN / LVDS_BKLT_EN | O | eDP/LVDS |
| | PWR | GND | A80 | B80 | GND | PWR | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| eDP/LVDS | O | eDP_TX3+ / LVDS_A_CK+ | A81 | B81 | LVDS_B_CK+ | O | LVDS |
| eDP/LVDS | O | eDP_TX3- / LVDS_A_CK- | A82 | B82 | LVDS_B_CK- | O | LVDS |
| eDP/LVDS | I/O | eDP_AUX+ / LVDS_I2C_CK | A83 | B83 | eDP_BKLT_CTRL/LVDS_BKLT_CTRL | O | eDP/LVDS |
| eDP/LVDS | I/O | eDP_AUX- / LVDS_I2C_DAT | A84 | B84 | VCC_5V_SBY | PWR | |
| GPIO | I | GPI3 | A85 | B85 | VCC_5V_SBY | PWR | |
| | N.A. | RSVD | A86 | B86 | VCC_5V_SBY | PWR | |
| eDP | I | eDP_HPD | A87 | B87 | VCC_5V_SBY | PWR | |
| PCIE | O | PCIE_CK_REF+ | A88 | B88 | BIOS_DIS1# | I | SPI |
| PCIE | O | PCIE_CK_REF- | A89 | B89 | N.C. | N.A. | |
| | PWR | GND | A90 | B90 | GND | PWR | |
| SPI | O | SPI_POWER | A91 | B91 | N.C. | N.A. | |
| SPI | I | SPI_MISO | A92 | B92 | N.C. | N.A. | |
| GPIO | O | GPO0 | A93 | B93 | N.C. | N.A. | |
| SPI | O | SPI_CLK | A94 | B94 | N.C. | N.A. | |
| SPI | O | SPI_MOSI | A95 | B95 | N.C. | N.A. | |
| MISC | I | TPM_PP | A96 | B96 | N.C. | N.A. | |
| TYPE | N.A. | Type10#: N.C. | A97 | B97 | SPI_CS# | O | SPI |
| SERIAL | O | SER0_TX | B75 | B98 | RSVD | N.A. | |
| SERIAL | I | SER0_RX | A99 | B99 | RSVD | N.A. | |
| | PWR | GND | A100 | B100 | GND | PWR | |
| SERIAL | O | SER1_TX | A101 | B101 | FAN_PWMOUT | O | MISC |
| SERIAL | I | SER1_RX | A102 | B102 | FAN_TACHIN | I | MISC |
| PWR_MGMT | I | LID# | A103 | B103 | SLEEP# | I | PWR_MGMT |
| | PWR | VCC_12V | A104 | B104 | VCC_12V | PWR | |
| | PWR | VCC_12V | A105 | B105 | VCC_12V | PWR | |
| | PWR | VCC_12V | A106 | B106 | VCC_12V | PWR | |
| | PWR | VCC_12V | A107 | B107 | VCC_12V | PWR | |
| | PWR | VCC_12V | A108 | B108 | VCC_12V | PWR | |
| | PWR | VCC_12V | A109 | B109 | VCC_12V | PWR | |
| | PWR | GND | A110 | B110 | GND | PWR | |

| COM Express® Connector CD – CN6 | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | ROW C | | | ROW D | | |
| SIGNAL GROUP | Type | Pin name | Pin nr. | Pin nr. | Pin name | Type | SIGNAL GROUP |
| | PWR | GND | C1 | D1 | GND | PWR | |
| | PWR | GND | C2 | D2 | GND | PWR | |
| USB | I | USB_SSRX0- | C3 | D3 | USB_SSTX0- | O | USB |
| USB | I | USB_SSRX0+ | C4 | D4 | USB_SSTX0+ | O | USB |
| | PWR | GND | C5 | D5 | GND | PWR | |
| USB | I | USB_SSRX1- | C6 | D6 | USB_SSTX1- | O | USB |
| USB | I | USB_SSRX1+ | C7 | D7 | USB_SSTX1+ | O | USB |
| | PWR | GND | C8 | D8 | GND | PWR | |
| USB | I | USB_SSRX2- | C9 | D9 | USB_SSTX2- | O | USB |
| USB | I | USB_SSRX2+ | C10 | D10 | USB_SSTX2+ | O | USB |
| | PWR | GND | C11 | D11 | GND | PWR | |
| USB | I | USB_SSRX3- | C12 | D12 | USB_SSTX3- | O | USB |
| USB | I | USB_SSRX3+ | C13 | D13 | USB_SSTX3+ | O | USB |
| | PWR | GND | C14 | D14 | GND | PWR | |
| | N.A. | N.C. | C15 | D15 | DDI1_CTRLCLK_AUX+ | I/O | DDI |
| | N.A. | N.C. | C16 | D16 | DDI1_CTRLDATA_AUX- | I/O | DDI |
| | N.A. | RSVD | C17 | D17 | RSVD | N.A. | |
| | N.A. | RSVD | C18 | D18 | RSVD | N.A. | |
| | N.A. | N.C. | C19 | D19 | N.C. | N.A. | |
| | N.A. | N.C. | C20 | D20 | N.C. | N.A. | |
| | PWR | GND | C21 | D21 | GND | PWR | |
| | N.A. | N.C. | C22 | D22 | N.C. | N.A. | |
| | N.A. | N.C. | C23 | D23 | N.C. | N.A. | |
| DDI | I | DDI1_HPD | C24 | D24 | RSVD | N.A. | |
| | N.A. | N.C. | C25 | D25 | RSVD | N.A. | |
| | N.A. | N.C. | C26 | D26 | DDI1_PAIR0+ | O | DDI |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | N.A. | RSVD | C27 | D27 | DDI1_PAIR0- | O | DDI |
| | N.A. | RSVD | C28 | D28 | RSVD | N.A. | |
| | N.A. | N.C. | C29 | D29 | DDI1_PAIR1+ | O | DDI |
| | N.A. | N.C. | C30 | D30 | DDI1_PAIR1- | O | DDI |
| | PWR | GND | C31 | D31 | GND | PWR | |
| DDI | I/O | DDI2_CTRLCLK_AUX+ | C32 | D32 | DDI1_PAIR2+ | O | DDI |
| DDI | I/O | DDI2_CTRLDATA_AUX- | C33 | D33 | DDI1_PAIR2- | O | DDI |
| DDI | I | DDI2_DDC_AUX_SEL | C34 | D34 | DDI1_DDC_AUX_SEL | I | DDI |
| | N.A. | RSVD | C35 | D35 | RSVD | N.A. | |
| DDI | I/O | DDI3_CTRLCLK_AUX+ | C36 | D36 | DDI1_PAIR3+ | O | DDI |
| DDI | I/O | DDI3_CTRLDATA_AUX- | C37 | D37 | DDI1_PAIR3- | O | DDI |
| DDI | I | DDI3_DDC_AUX_SEL | C38 | D38 | RSVD | N.A. | |
| DDI | O | DDI3_PAIR0+ | C39 | D39 | DDI2_PAIR0+ | O | DDI |
| DDI | O | DDI3_PAIR0- | C40 | D40 | DDI2_PAIR0- | O | DDI |
| | PWR | GND | C41 | D41 | GND | PWR | |
| DDI | O | DDI3_PAIR1+ | C42 | D42 | DDI2_PAIR1+ | O | DDI |
| DDI | O | DDI3_PAIR1- | C43 | D43 | DDI2_PAIR1- | O | DDI |
| DDI | I | DDI3_HPD | C44 | D44 | DDI2_HPD | I | DDI |
| | N.A. | RSVD | C45 | D45 | RSVD | N.A. | |
| DDI | O | DDI3_PAIR2+ | C46 | D46 | DDI2_PAIR2+ | O | DDI |
| DDI | O | DDI3_PAIR2- | C47 | D47 | DDI2_PAIR2- | O | DDI |
| | N.A. | RSVD | C48 | D48 | RSVD | N.A. | |
| DDI | O | DDI3_PAIR3+ | C49 | D49 | DDI2_PAIR3+ | O | DDI |
| DDI | O | DDI3_PAIR3- | C50 | D50 | DDI2_PAIR3- | O | DDI |
| | PWR | GND | C51 | D51 | GND | PWR | |
| PEG | I | PEG_RX0+ | C52 | D52 | PEG_TX0+ | O | PEG |
| PEG | I | PEG_RX0- | C53 | D53 | PEG_TX0- | O | PEG |
| TYPE | N.A. | TYPE0#: N.C. | C54 | D54 | N.C. | N.A. | |
| PEG | I | PEG_RX1+ | C55 | D55 | PEG_TX1+ | O | PEG |
| PEG | I | PEG_RX1- | C56 | D56 | PEG_TX1- | O | PEG |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TYPE | N.A. | TYPE1#: N.C. | C57 | D57 | TYPE2#: GND | N.A. | TYPE |
| PEG | I | PEG_RX2+ | C58 | D58 | PEG_TX2+ | O | PEG |
| PEG | I | PEG_RX2- | C59 | D59 | PEG_TX2- | O | PEG |
| | PWR | GND | C60 | D60 | GND | PWR | |
| PEG | I | PEG_RX3+ | C61 | D61 | PEG_TX3+ | O | PEG |
| PEG | I | PEG_RX3- | C62 | D62 | PEG_TX3- | O | PEG |
| | N.A. | RSVD | C63 | D63 | RSVD | N.A. | |
| | N.A. | RSVD | C64 | D64 | RSVD | N.A. | |
| PEG | I | PEG_RX4+ | C65 | D65 | PEG_TX4+ | O | PEG |
| PEG | I | PEG_RX4- | C66 | D66 | PEG_TX4- | O | PEG |
| | N.A. | RSVD | C67 | D67 | GND | PWR | |
| PEG | I | PEG_RX5+ | C68 | D68 | PEG_TX5+ | O | PEG |
| PEG | I | PEG_RX5- | C69 | D69 | PEG_TX5- | O | PEG |
| | PWR | GND | C70 | D70 | GND | PWR | |
| PEG | I | PEG_RX6+ | C71 | D71 | PEG_TX6+ | O | PEG |
| PEG | I | PEG_RX6- | C72 | D72 | PEG_TX6- | O | PEG |
| | PWR | GND | C73 | D73 | GND | PWR | |
| PEG | I | PEG_RX7+ | C74 | D74 | PEG_TX7+ | O | PEG |
| PEG | I | PEG_RX7- | C75 | D75 | PEG_TX7- | O | PEG |
| | PWR | GND | C76 | D76 | GND | PWR | |
| | N.A. | RSVD | C77 | D77 | RSVD | N.A. | |
| | N.A. | N.C. | C78 | D78 | N.C. | N.A. | |
| | N.A. | N.C. | C79 | D79 | N.C. | N.A. | |
| | PWR | GND | C80 | D80 | GND | PWR | |
| | N.A. | N.C. | C81 | D81 | N.C. | N.A. | |
| | N.A. | N.C. | C82 | D82 | N.C. | N.A. | |
| | N.A. | RSVD | C83 | D83 | RSVD | N.A. | |
| | PWR | GND | C84 | D84 | GND | PWR | |
| | N.A. | N.C. | C85 | D85 | N.C. | N.A. | |
| | N.A. | N.C. | C86 | D86 | N.C. | N.A. | |

| | | | | | |
|---|---|---|---|---|---|
| PWR | GND | C87 | D87 | GND | PWR |
| N.A. | N.C. | C88 | D88 | N.C. | N.A. |
| N.A. | N.C. | C89 | D89 | N.C. | N.A. |
| PWR | GND | C90 | D90 | GND | PWR |
| N.A. | N.C. | C91 | D91 | N.C. | N.A. |
| N.A. | N.C. | C92 | D92 | N.C. | N.A. |
| PWR | GND | C93 | D93 | GND | PWR |
| N.A. | N.C. | C94 | D94 | N.C. | N.A. |
| N.A. | N.C. | C95 | D95 | N.C. | N.A. |
| PWR | GND | C96 | D96 | GND | PWR |
| N.A. | RSVD | C97 | D97 | RSVD | N.A. |
| N.A. | N.C. | C98 | D98 | N.C. | N.A. |
| N.A. | N.C. | C99 | D99 | N.C. | N.A. |
| PWR | GND | C100 | D100 | GND | PWR |
| N.A. | N.C. | C101 | D101 | N.C. | N.A. |
| N.A. | N.C. | C102 | D102 | N.C. | N.A. |
| PWR | GND | C103 | D103 | GND | PWR |
| PWR | VCC_12V | C104 | D104 | VCC_12V | PWR |
| PWR | VCC_12V | C105 | D105 | VCC_12V | PWR |
| PWR | VCC_12V | C106 | D106 | VCC_12V | PWR |
| PWR | VCC_12V | C107 | D107 | VCC_12V | PWR |
| PWR | VCC_12V | C108 | D108 | VCC_12V | PWR |
| PWR | VCC_12V | C109 | D109 | VCC_12V | PWR |
| PWR | GND | C110 | D110 | GND | PWR |

### 3.2.4.1 *Audio interface signals*

The COMe-B75-CT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard. Up to 2 HD audio codecs on the carrier board can be supported.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the AMD HD audio controller, output from the module to the Carrier board, electrical level +3.3V_RUN.

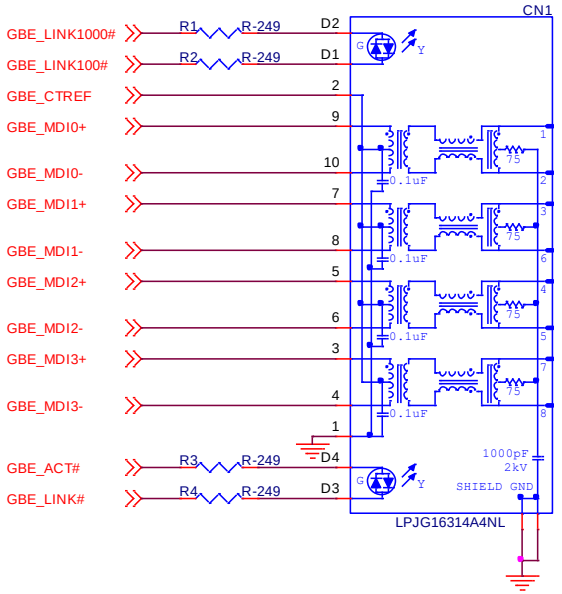
HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_SDIN[0..1]: HD Audio Serial Data In signal. Inputs to the module from the Codec(s) placed on the Carrier board, electrical level +3.3V_RUN.

The first four signals have to be connected to all the HD Audio codecs present on the carrier board. For each Codec, only one HDA_SDIN signal must be used. Please refer to the chosen Codecs' Reference Design Guide for correct implementation of audio section on the carrier board.

### 3.2.4.2 *Gigabit Ethernet signals*

The Gigabit Ethernet interface is realised, on COMe-B75-CT6 module, using an Intel® I210/I211 Gigabit Ethernet controller, which is interfaced to the SoC through the General Purpose PCI-express port #4 or through the PCI-express Packet switch port #3, depending on the factory option purchased.




Here following the signals involved in Gigabit Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE_SPD: Ethernet Controller Software Defined Pin. Directly connected to the Intel® I210/I211 SDP0 pin

+3.3V_LAN is derived from +3.3V_ALW power rail through a 120Ω ferrite bead.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic provided in the previous page as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector.

Intel® I210/I211 Gigabit Ethernet controllers, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

#### *3.2.4.3 S-ATA signals*

The AMD Ryzen™ Embedded V1000 processors offer two S-ATA Gen3 interfaces, which are all carried out on COM Express® connector AB.

All SATA ports support 1.5 Gbps, 3.0 Gbps and 6.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. +3.3V_RUN Active Low output signal with 10kΩ pull-up resistor.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors.

#### *3.2.4.4 PCI Express interface signals*

COMe-B75-CT6 can offer externally up to six PCI Express lanes, which are managed directly by the AMD Ryzen™ Embedded V1000 processors.

These interfaces can be managed only as single PCI-e x1 lanes.

PCI express Gen3 (8 GT/s) is supported an PCI-e ports #0 ..#3, while PCI-e ports #4 and #5 (available only with the PCI-e switch mounted) are Gen 2.

Here following the signals involved in PCI express management.

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #0.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #0.

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #1.

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #1.

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #2.

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #2.

PCIE3_TX+/PCIE3_TX-: PCI Express lane #3, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #3.

PCIE3_RX+/PCIE3_RX-: PCI Express lane #3, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #3.

PCIE4_TX+/PCIE4_TX-: PCI Express lane #4, Transmitting Output Differential pair. Connected to the PCI Express Packet switch port #1, if mounted.

PCIE4_RX+/PCIE4_RX-: PCI Express lane #4, Receiving Input Differential pair. Connected to the PCI Express Packet switch port #1, if mounted.

PCIE5_TX+/PCIE5_TX-: PCI Express lane #5, Transmitting Output Differential pair. Connected to the PCI Express Packet switch port #2, if mounted.

PCIE5_RX+/PCIE5_RX-: PCI Express lane #5, Receiving Input Differential pair. Connected to the PCI Express Packet switch port #2, if mounted.

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are seven different PCI express lanes and one PEG. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer should be used to replicate the reference clock to all the devices.

PCI Express ports from # 0 to #3 can be grouped to work as a single PCI-e x4 port, or two PCI-e x2 ports, or (one PCI-e x2 + 2x PCI-e x1) ports. This can be done via BIOS settings (please check par.4.3.9).

### 3.2.4.5 PEG interface signals

In addition to the six PCI express lanes, described in the previous paragraph, the COMe-B75-CT6 module offer a PCI-Express x8 graphics interface (PEG), which can be used for connection of external graphics cards. Such an interface is directly managed by the AMD Ryzen™ Embedded V1000 processors.

PCI express Gen3 is supported on PEG interface.

Here following the signals involved in PEG management.

PEG_TX[0..7]+/PEG_TX[0..7]-: PCI Express Graphics lane #0 ÷ #7, Transmitting Output Differential pairs.

PEG_RX[0..7]+/PEG_RX[0..7]-: PCI Express Graphics lane #0 ÷ #7, Receiving Output Differential pairs.

This PEG port can be configured to work as a single PCI-e x8 port or two PCI-e x4 ports (in that case, lanes #0÷#3 would be used for the first port, GFX#0, while lanes #4÷#7 would be used for the second port, GFX #1). This configuration can be done via BIOS settings (please check par.4.3.9).

### 3.2.4.6 USB interface signals

The AMD Ryzen™ Embedded V1000 processors embed two USB controllers, which allow, on COMe-B75-CT6 module, implementing four Superspeed ports (i.e. USB 3.0 compliant) and eight USB 1.x / 2.0 Host ports.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB0+/USB0-: Universal Serial Bus Port #0 bidirectional differential pair, managed by the SoC's USB Controller #0 (Port #1).

USB1+/USB1-: Universal Serial Bus Port #1 bidirectional differential pair, managed by the SoC's USB Controller #0 (Port #2).

USB2+/USB2-: Universal Serial Bus Port #2 bidirectional differential pair, managed by the USB 3.0 Hub Downstream port #1

USB3+/USB3-: Universal Serial Bus Port #3 bidirectional differential pair, managed by the USB 3.0 Hub Downstream port #2.

USB4+/USB4-: Universal Serial Bus Port #4 bidirectional differential pair, managed by the USB 2.0 Hub Downstream port #4.

USB5+/USB5-: Universal Serial Bus Port #5 bidirectional differential pair, managed by the USB 2.0 Hub Downstream port #2.

USB6+/USB6-: Universal Serial Bus Port #6 bidirectional differential pair, managed by the USB 2.0 Hub Downstream port #3.

USB7+/USB7-: Universal Serial Bus Port #7 bidirectional differential pair, managed by the USB 2.0 Hub Downstream port #1.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by the SoC's USB Controller #0 (Port #1).

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by the SoC's USB Controller #0 (Port #1).

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair; it is managed by the SoC's USB Controller #0 (Port #2).

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair; it is managed by the SoC's USB Controller #0 (Port #2).

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair; it is managed by the USB 3.0 Hub Downstream port #1.

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair; it is managed by the USB 3.0 Hub Downstream port #1.

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair; it is managed by the USB 3.0 Hub Downstream port #2.

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair; it is managed by the USB 3.0 Hub Downstream port #2.

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-B75-CT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-B75-CT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-B75-CT6 module.

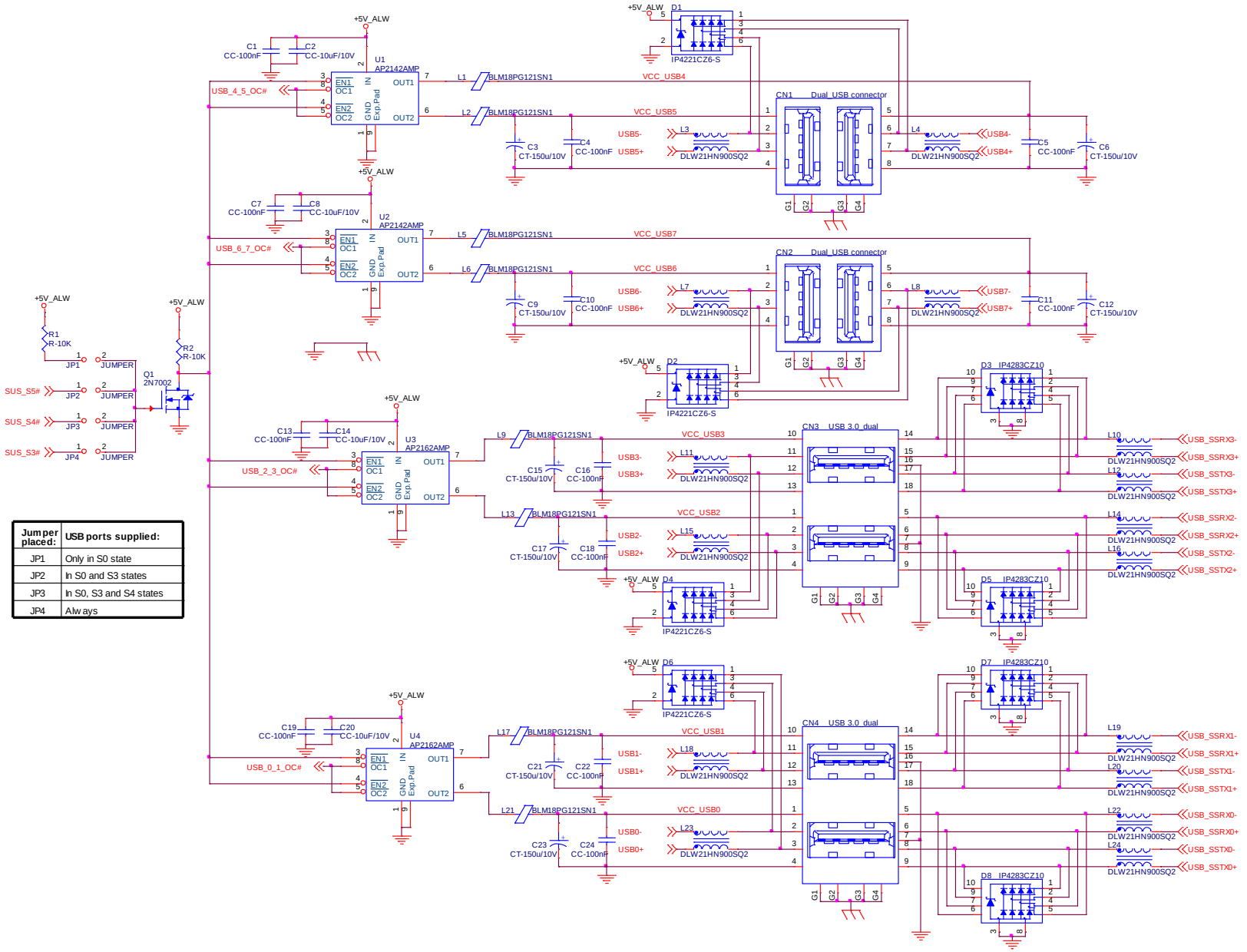
USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-B75-CT6 module.

100nF AC series decoupling capacitors are placed on each transmitting line of USB Super speed differential pairs.

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and 3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).




| Jumper placed: | USB ports supplied: |
|---|---|
| JP1 | Only in S0 state |
| JP2 | In S0 and S3 states |
| JP3 | In S0, S3 and S4 states |
| JP4 | Always |

### *3.2.4.7 LVDS Flat Panel signals*

The AMD Ryzen™ Embedded V1000 processors offer four native Digital Display interfaces, which can support Display Port, embedded Display Port, DVI, or HDMI interfaces. The LVDS interface, which is frequently used in many application fields, is not directly supported by these SoCs.

For this reason, as a factory option, COMe-B75-CT6 modules can be equipped with an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for AMD Ryzen™ Embedded V1000 processors, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins there can be the LVDS first channel **or** eDP interface.
>
> When placing an order of COMe-B75-CT6 modules, please take care of specifying if it is necessary LVDS interface or eDP interface.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: Panel Power Enable signal, electrical level +3.3V_RUN with a 10kΩ pull-down resistor. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: Panel Backlight Enable signal, electrical level +3.3V_RUN with a 10kΩ pull-down resistor. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +3.3V_RUN electrical level output.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN.

#### *3.2.4.8 Embedded Display Port (eDP) signals*

As described in the previous paragraph, the AMD Ryzen™ Embedded V1000 processors offer four Digital Display Interfaces.

As a factory option, one of these interfaces (DDI3) can be switched toward COM Express connector AB. When the board is not configured with the eDP-to-LVDS bridge, then the switched DDI interface supports eDP displays. Depending on the number of eDP lanes used (1, 2 or 4) it is possible to support the higher resolution displays.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1.

eDP_TX2+/eDP_TX2-: eDP channel differential data pair #2.

eDP_TX3+/eDP_TX3-: eDP channel differential data pair #3.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_RUN electrical level input with 100KΩ pull-down resistor.

eDP_VDD_EN: Panel Power Enable signal, electrical level +3.3V_RUN with a 10kΩ pull-down resistor. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: Panel Backlight Enable signal, electrical level +3.3V_RUN with a 10kΩ pull-down resistor. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +3.3V_RUN electrical level output.

#### 3.2.4.9 LPC interface signals

According to COM Express® specifications rel. 3.0, on the on COM Express connector AB there are 9 pins that are used for implementation of Low Pin Count (LPC) Bus interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_RUN electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_RUN electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_DRQ0#: LPC Serial DMA request, +3.3V_RUN electrical level input signals, active low. This signal is used to request DMA or bus master access.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_RUN electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_RUN electrical level. This signal is used only by peripherals requiring Interrupt support.

Although COM Express® specifications rel. 3.0 foresee that LPC and eSPI interfaces can share the same pins, on COMe-B75-CT6 module only LPC interface is supported

#### 3.2.4.10 SPI interface signals

The AMD Ryzen™ Embedded V1000 processors offer also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of Serial Flash devices. Please be aware that this interface should be used exclusively to support platform firmware (BIOS).

Signals involved with SPI management are the following:

SPI_CS#: SPI Chip select, active low output signal, +1.8V_S voltage level with 100kΩ pull-up resistor.

SPI_MISO: SPI Master In Slave Out, Input to COM Express® module from SPI devices embedded on the Carrier Board. +1.8V_ALW voltage level with 10kΩ pull-up resistor.

SPI_MOSI: SPI Master Out Slave In, Output from COM Express® module to SPI devices embedded on the Carrier Board. +1.8V_ALW voltage level.

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. +1.8V_ALW voltage level with 10kΩ pull-up resistor. Clock frequencies up to 66MHz are supported.

SPI_POWER: Power Supply Output for carrier board's SPI devices. +1.8V_S voltage level.

BIOS_DIS[0..1]#: BIOS Disable strap input, electrical level +3.3V_ALW with 10kΩ pull-up resistor. These two signals are inputs of the COM Express® Module, that on the carrier board can be left floating or pulled down in order to select which SPI Flash device has to be used for module's boot. Please refer to table 4.13 of COM Express® Module Base Specifications rel. 2.1 for the meaning of possible configurations of these two signals.

### *3.2.4.11 Digital Display interfaces*

The AMD Radeon™ VEGA GPUs, embedded inside the AMD Ryzen™ Embedded V1000 processors, offer four Digital Display Interfaces, which can support DP, eDP, DVI and/or HDMI interfaces.

DDI ports #0, #1 and #2 are always carried out to COM Express connector CD, while DDI port #3 can be used to implement, on COM Express connector AB, the LVDS interface or the eDP interface (see also paragraphs 3.2.4.7and 3.2.4.8).

The DDI ports can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

| Digital Display Interfaces - Pin multiplexing | | | | | |
|---|---|---|---|---|---|
| | | Multimode Display Port mode | | TMDS (HDMI/DVI) mode | |
| Pin nr. | Pin name | Signal | Description | Signal | Description |
| D26 | DDI1_PAIR0+ | DP1_LANE0+ | DP1 Differential pair #0 non-inverting line | TMDS1_DATA2+ | TMDS1 Differential pair #2 non-inverting line |
| D27 | DDI1_PAIR0- | DP1_LANE0- | DP1 Differential pair #0 inverting line | TMDS1_DATA2- | TMDS1 Differential pair #2 inverting line |
| D29 | DDI1_PAIR1+ | DP1_LANE1+ | DP1 Differential pair #1 non-inverting line | TMDS1_DATA1+ | TMDS1 Differential pair #1 non-inverting line |
| D30 | DDI1_PAIR1- | DP1_LANE1- | DP1 Differential pair #1 inverting line | TMDS1_DATA1- | TMDS1 Differential pair #1 inverting line |
| D32 | DDI1_PAIR2+ | DP1_LANE2+ | DP1 Differential pair #2 non-inverting line | TMDS1_DATA0+ | TMDS1 Differential pair #0 non-inverting line |
| D33 | DDI1_PAIR2- | DP1_LANE2- | DP1 Differential pair #2 inverting line | TMDS1_DATA0- | TMDS1 Differential pair #0 inverting line |
| D36 | DDI1_PAIR3+ | DP1_LANE3+ | DP1 Differential pair #3 non-inverting line | TMDS1_CLK+ | TMDS1 Differential clock non-inverting line |
| D37 | DDI1_PAIR3- | DP1_LANE3- | DP1 Differential pair #3 inverting line | TMDS1_CLK- | TMDS1 Differential clock inverting line |
| C24 | DDI1_HPD | DP1_HPD | DP1 Hot Plug Detect signal | HDMI1_HPD | HDMI #1 Hot Plug Detect signal |
| D15 | DDI1_CTRLCLK_AUX+ | DP1_AUX+ | DP1 Auxiliary channel non-inverting line | HDMI1_CTRLCLK | DDC Clock line for HDMI panel #1. |
| D16 | DDI1_CTRLDATA_AUX- | DP1_AUX- | DP1 Auxiliary channel inverting line | HDMI1_CTRLDATA | DDC Data line for HDMI panel #1. |
| D34 | DDI1_DDC_AUX_SEL | DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface | | | |
| D39 | DDI2_PAIR0+ | DP2_LANE0+ | DP2 Differential pair #0 non-inverting line | TMDS2_DATA2+ | TMDS2 Differential pair #2 non-inverting line |
| D40 | DDI2_PAIR0- | DP2_LANE0- | DP2 Differential pair #0 inverting line | TMDS2_DATA2- | TMDS2 Differential pair #2 inverting line |

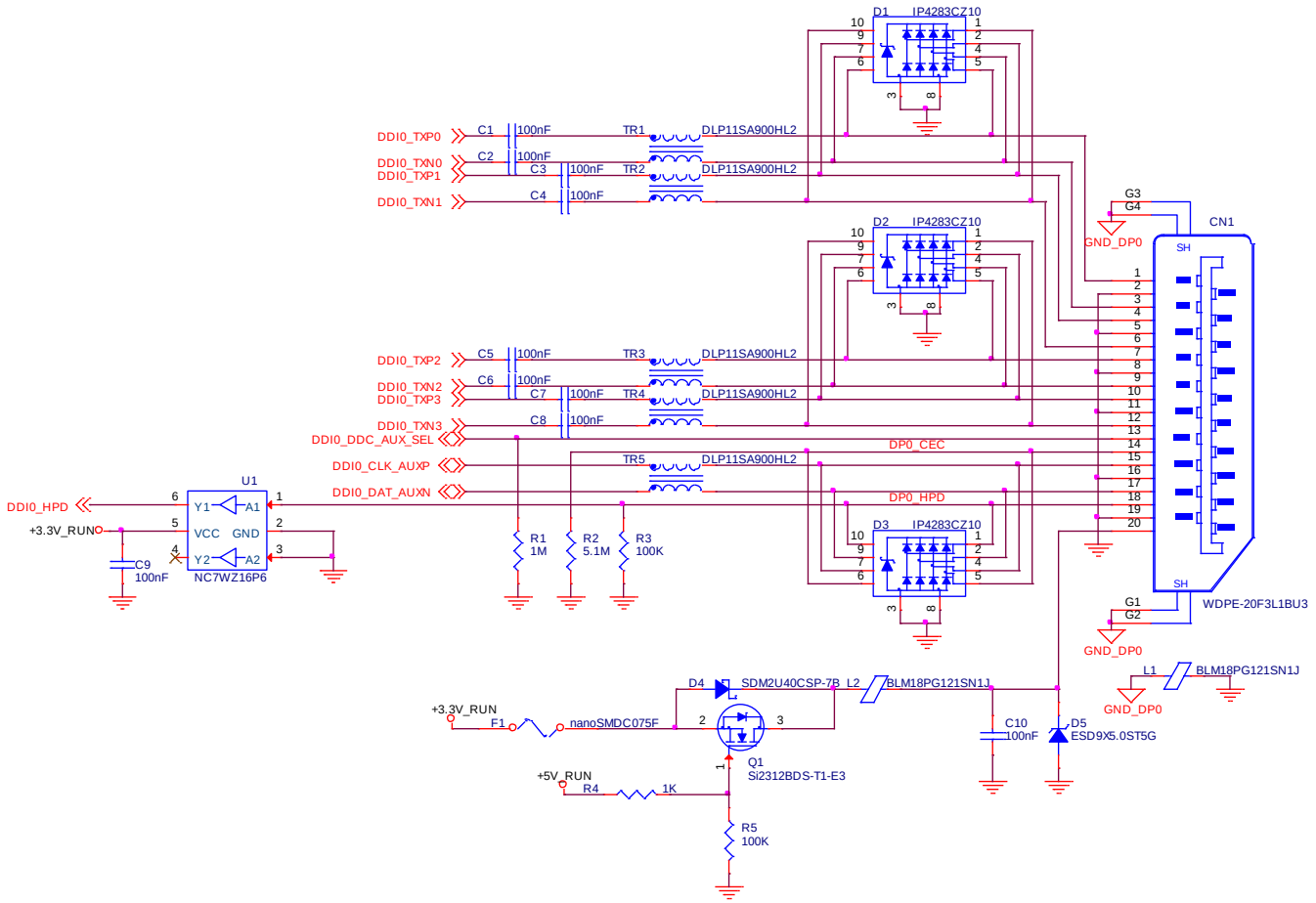
| | | | | | |
|---|---|---|---|---|---|
| D42 | DDI2_PAIR1+ | DP2_LANE1+ | DP2 Differential pair #1 non-inverting line | TMDS2_DATA1+ | TMDS2 Differential pair #1 non-inverting line |
| D43 | DDI2_PAIR1- | DP2_LANE1- | DP2 Differential pair #1 inverting line | TMDS2_DATA1- | TMDS2 Differential pair #1 inverting line |
| D46 | DDI2_PAIR2+ | DP2_LANE2+ | DP2 Differential pair #2 non-inverting line | TMDS2_DATA0+ | TMDS2 Differential pair #0 non-inverting line |
| D47 | DDI2_PAIR2- | DP2_LANE2- | DP2 Differential pair #2 inverting line | TMDS2_DATA0- | TMDS2 Differential pair #0 inverting line |
| D49 | DDI2_PAIR3+ | DP2_LANE3+ | DP2 Differential pair #3 non-inverting line | TMDS2_CLK+ | TMDS2 Differential clock non-inverting line |
| D50 | DDI2_PAIR3- | DP2_LANE3- | DP2 Differential pair #3 inverting line | TMDS2_CLK- | TMDS2 Differential clock inverting line |
| D44 | DDI2_HPD | DP2_HPD | DP2 Hot Plug Detect signal | HDMI2_HPD | HDMI #2 Hot Plug Detect signal |
| C32 | DDI2_CTRLCLK_AUX+ | DP2_AUX+ | DP2 Auxiliary channel non-inverting line | HDMI2_CTRLCLK | DDC Clock line for HDMI panel #2.. |
| C33 | DDI2_CTRLDATA_AUX- | DP2_AUX- | DP2 Auxiliary channel inverting line | HDMI2_CTRLDATA | DDC Data line for HDMI panel #2. |
| C34 | DDI2_DDC_AUX_SEL | DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface | | | |
| C39 | DDI3_PAIR0+ | DP3_LANE0+ | DP3 Differential pair #0 non-inverting line | TMDS3_DATA2+ | TMDS3 Differential pair #2 non-inverting line |
| C40 | DDI3_PAIR0- | DP3_LANE0- | DP3 Differential pair #0 inverting line | TMDS3_DATA2- | TMDS3 Differential pair #2 inverting line |
| C42 | DDI3_PAIR1+ | DP3_LANE1+ | DP3 Differential pair #1 non-inverting line | TMDS3_DATA1+ | TMDS3 Differential pair #1 non-inverting line |
| C43 | DDI3_PAIR1- | DP3_LANE1- | DP3 Differential pair #1 inverting line | TMDS3_DATA1- | TMDS3 Differential pair #1 inverting line |
| C46 | DDI3_PAIR2+ | DP3_LANE2+ | DP3 Differential pair #2 non-inverting line | TMDS3_DATA0+ | TMDS3 Differential pair #0 non-inverting line |
| C47 | DDI3_PAIR2- | DP3_LANE2- | DP3 Differential pair #2 inverting line | TMDS3_DATA0- | TMDS3 Differential pair #0 inverting line |
| C49 | DDI3_PAIR3+ | DP3_LANE3+ | DP3 Differential pair #3 non-inverting line | TMDS3_CLK+ | TMDS3 Differential clock non-inverting line |
| C50 | DDI3_PAIR3- | DP3_LANE3- | DP3 Differential pair #3 inverting line | TMDS3_CLK- | TMDS3 Differential clock inverting line |
| C44 | DDI3_HPD | DP3_HPD | DP3 Hot Plug Detect signal | HDMI3_HPD | HDMI #3 Hot Plug Detect signal |
| C36 | DDI3_CTRLCLK_AUX+ | DP3_AUX+ | DP3 Auxiliary channel non-inverting line | HDMI3_CTRLCLK | DDC Clock line for HDMI panel #3. |
| C37 | DDI3_CTRLDATA_AUX- | DP3_AUX- | DP3 Auxiliary channel inverting line | HDMI3_CTRLDATA | DDC Data line for HDMI panel #3. |
| C38 | DDI3_DDC_AUX_SEL | DDI#3 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface | | | |

All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are active high inputs with 100KΩ pull-down resistors. According to COM Express specifications, the carrier board must provide for Hot Plug Detect signal's buffering in order to prevent back feeding of power in the event that the monitor is powered up when the Carrier Board is powered down

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

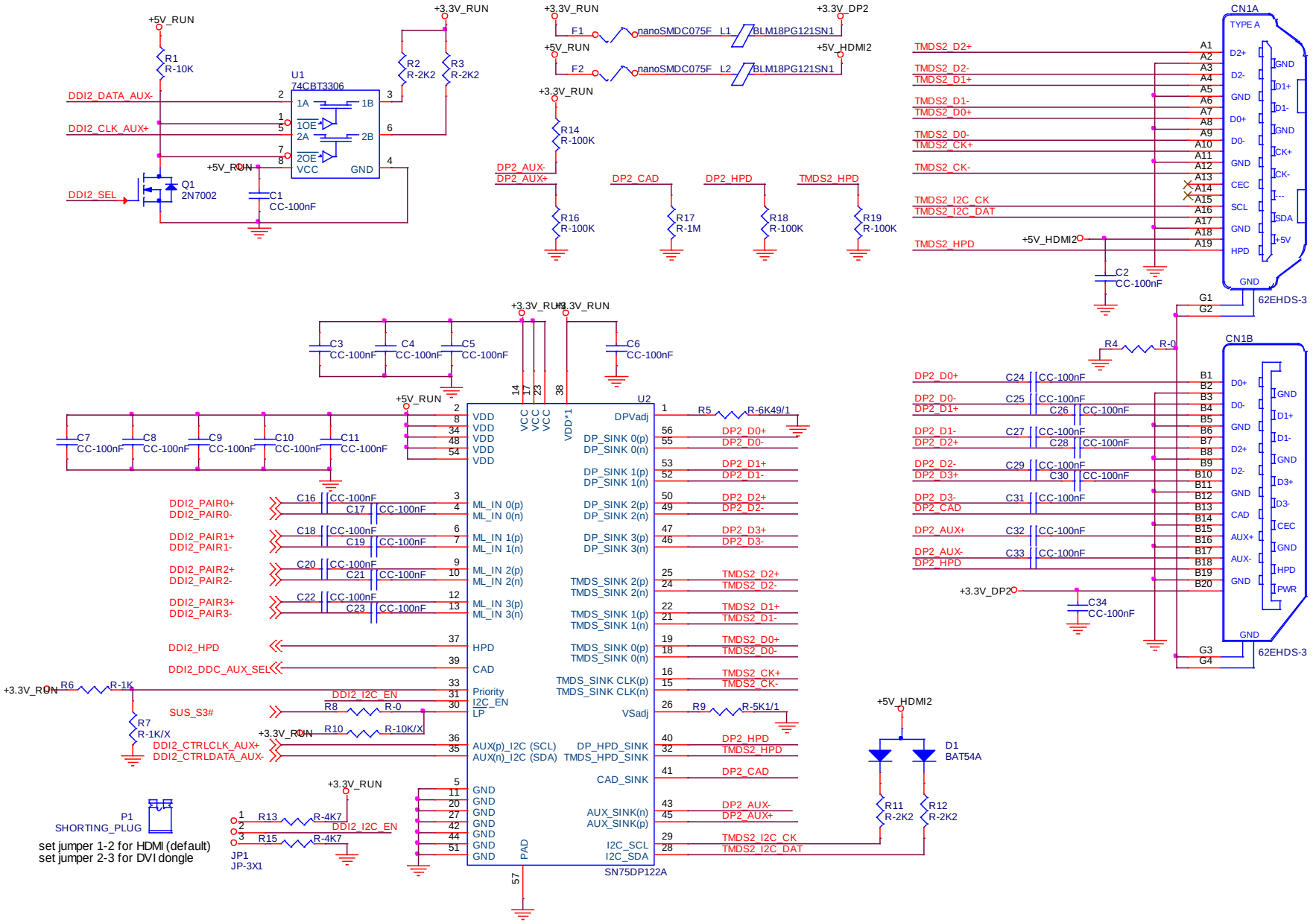
In the next page, an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #1, but any DDI interface can be used.




The example schematics in the following page, instead, shows the implementation (using DDI interface #2, but any DDI can be used for this purpose) of a double connector DP++ and HDMI, managed using a DisplayPort 1:2 Switch with Integrated TMDS Translator, which provides to TMDS voltage level shifter for HDMI/DVI connection.

By implementing such a schematic, the module can configure itself automatically to work with external HDMI/DVI or multimode Display Port interfaces, depending on the cable connected. In case both an HDMI and a DP are connected, the HDMI interface will take priority automatically. This order can be changed by removing resistor R6 and mounting resistor R7.

The jumper JP1 is used to enable or disable switch's I2C internal registers, for use of TMDS interface, respectively, for HDMI or DVI displays.


+5V_RUN
+3.3V_RUN
+3.3V_DP2
+5V_HDMI2
R1 R-10K
R2 R-2K2
R3 R-2K2
U1 74CBT3306
DDI2_DATA_AUX-
DDI2_CLK_AUX+
DDI2_SEL
Q1 2N7002
C1 CC-100nF
F1 nanoSMDC075F L1 BLM18PG121SN1
F2 nanoSMDC075F L2 BLM18PG121SN1
R14 R-100K
R16 R-100K
R17 R-1M
R18 R-100K
R19 R-100K
DP2_AUX-
DP2_AUX+
DP2_CAD
DP2_HPD
TMDS2_HPD
CN1A
TYPE A
TMDS2_D2+
TMDS2_D2-
TMDS2_D1+
TMDS2_D1-
TMDS2_D0+
TMDS2_D0-
TMDS2_CK+
TMDS2_CK-
TMDS2_I2C_CK
TMDS2_I2C_DAT
C2 CC-100nF
62EHDS-3
C3 CC-100nF
C4 CC-100nF
C5 CC-100nF
C6 CC-100nF
U2
SN75DP122A
C7 CC-100nF
C8 CC-100nF
C9 CC-100nF
C10 CC-100nF
C11 CC-100nF
R4 R-0
CN1B
C24 CC-100nF
C25 CC-100nF
C26 CC-100nF
C27 CC-100nF
C28 CC-100nF
C29 CC-100nF
C30 CC-100nF
C31 CC-100nF
C32 CC-100nF
C33 CC-100nF
C34 CC-100nF
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_HPD
DDI2_DDC_AUX_SEL
SUS_S3#
DDI2_I2C_EN
DDI2_CTRLCLK_AUX+
DDI2_CTRLDATA_AUX-
R5 R-6K49/1
R6 R-1K
R7 R-1K/X
R8 R-0
R9 R-5K1/1
R10 R-10K/X
D1 BAT54A
R11 R-2K2
R12 R-2K2
R13 R-4K7
R15 R-4K7
P1 SHORTING_PLUG
JP1 JP-3X1
set jumper 1-2 for HDMI (default)
set jumper 2-3 for DVI dongle

### *3.2.4.12 Serial Port interface signals*

According to COM Express® Rel. 3.0 specifications, since the COMe-B75-CT6 is a Type 6 module, it can offer two High Speed UART (HS UARTs) interfaces, which are managed by the AMD SoC.

Here following the signals related to UART interface:

SER0_TX: HS UART Interface #0, Serial data Transmit (output) line, 3.3V_RUN electrical level.

SER0_RX: HS UART Interface #0, Serial data Receive (input) line, 3.3V_RUN electrical level with a 47kΩ pull-up resistor.

SER1_TX: HS UART Interface #1, Serial data Transmit (output) line, 3.3V_RUN electrical level.

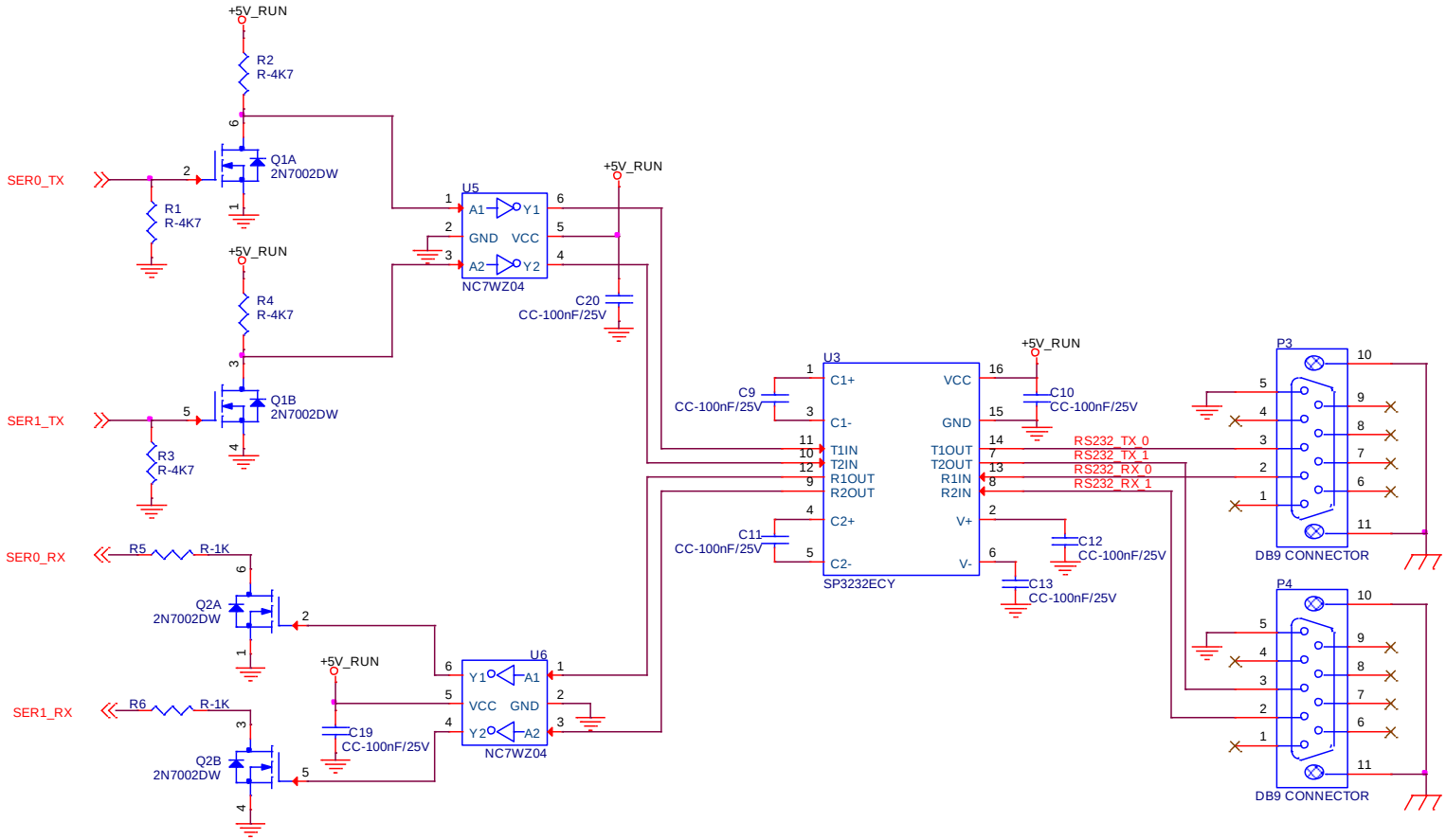
SER1_RX: HS UART Interface #1, Serial data Receive (input) line, 3.3V_RUN electrical level with a 47kΩ pull-up resistor.

In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to +12$V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then Schottky-diodes have been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the next page shows an example of implementation of RS-232 transceiver for the Carrier board.

> **!** Please be aware that the UARTs offered by the AMD SoCs are HS UARTs and not standard (legacy) COM ports.
>
> Linux is able to manage them anyway, while Windows recognizes these interfaces as HS UART devices, not as legacy COM ports. This means that using Windows it is necessary to use specific drivers for the devices connected, it is not possible to use them using standard communication software like Tera Term, Putty…




### *3.2.4.13 I2C interface signals*

This interface is managed by the embedded microcontroller.

Signals involved are the following

I2C_CK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

### 3.2.4.14 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-B75-CT6 module.

SPKR: Speaker output, +3.3V_RUN voltage signal, managed by the AMD Ryzen™ Embedded V1000 processors.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_RUN voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWM_OUT*: PWM output for FAN speed management, +3.3V_RUN voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHIN*: External FAN Tachometer Input. +3.3V_RUN voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence pin. This signal is used to indicate Physical Presence to the optional TPM device onboard. It is an active high input signal.

THRM#: Thermal Alarm Input. Active Low signal, +3.3V_RUN voltage with 10kΩ pull-up resistor, managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_RUN voltage output signal. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the SoC began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

### 3.2.4.15 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_ALW voltage signal with 4k7Ω pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_ALW voltage signal with 4k7Ω pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the COMe-B75-CT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_RUN voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is needed.

PWR_OK: Power Good Input, +3.3V_RUN active high signal with 100kΩ pull-up resistor. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_RUN electrical voltage signal with 10kΩ pull-up resistor. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S4#: connected to SUS_S5# (see below).

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S4 (Suspend to Disk) or S5 (Soft Off) power states.

WAKE0#: PCI Express Wake Input, active low +3.3V_ALW electrical voltage signal with 10kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_ALW electrical voltage signal with 2k2Ω pull-up resistor. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to LID# and SLEEP# inputs were dedicated to +12$V_{IN}$ power rail. Protection circuitry has been added on LID# and SLEEP# so that they are +12V Tolerant. This has been made in order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then

#### *3.2.4.16 SMBus signals*

This interface is managed by the AMD Ryzen™ Embedded V1000 processors' I2C Controller #2.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 4k7Ω pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 4k7Ω pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_ALW with a 10kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

#### *3.2.4.17 GPIO/SDIO interface signals*

According to COM Express® specifications rel. 3.0, there are 8 pins that can be used as General Purpose Inputs and Outputs **OR** as a SDIO interface.

The AMD Ryzen™ Embedded V1000 processors share the SD Card interface with the LPC Bus, which is used to communicate with the Embedded controller.

For this reason, the COMe-B75-CT6 module use these pins only for the connection of four General Purpose Inputs and four General Purpose Outputs, which are managed though the embedded microcontroller.

Signals involved are the following:

GPI[0÷3]: General Purpose Inputs, electrical level +3.3V_ALW with 10kΩ pull-up resistor each.

GPO[0÷3]: General Purpose Outputs, electrical level +3.3V_ALW with 10kΩ pull-down resistor each.

### 3.2.5 BOOT Strap Signals

Configuration straps are signals that, during system reset, are set as inputs (independently by their behaviour during normal operations) in order to allow the proper configuration of the processor For this reason, on COMe-B75-CT6 are placed the pull-up or pull-down resistors that are necessary to configure the board properly.

The customer must avoid to place, on the carrier board, pull-up or pull-down resistors on signals that are used as strap signal, since it could result in malfunctions of COMe-B75-CT6 module.

The following signals are used as configuration straps by COMe-B75-CT6 module at system reset.

SPI_CLK: pin A94 of connector AB. Used to enable the internal Clock generator for SPI. Signal at +1.8V_ALW voltage level with 10kΩ pull-up resistor

SYS_RESET #: pin B49 of connector AB. Used to enable normal power up / reset mode. Signal at +3.3V_ALW voltage level with a 47kΩ pull-up resistor.

# Chapter 4.
# BIOS SETUP

- Aptio setup Utility
- Main menu
- Advanced menu
- Chipset menu
- Security menu
- Boot menu
- Save & Exit menu

# 4.1 Aptio setup Utility

Basic setup of the board can be done using American Megatrends, Inc. “Aptio Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to Aptio Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “SCU” icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

| | |
|---|---|
| ← / → | Navigate between various setup screens (Main, Advanced, Security, Power, Boot...) |
| ↑ / ↓ | Select a setup item or a submenu |
| + / - | + and - keys allows to change the field value of highlighted menu item |
| <F1> | The <F1> key allows displaying the General Help screen. |
| <F2> | Previous Values |
| <F3> | <F3> key allows loading Optimised Defaults for the board. After pressing <F3> BIOS Setup utility will request for a confirmation, before loading such default values. By pressing <ESC> key, this function will be aborted |
| <F4> | <F4> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted |
| <ESC> | <Esc> key allows discarding any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted |
| <ENTER> | <Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow displaying the setup sub- screens. |

It is possible to reset the UEFI BIOS Setup to Factory Defaults by using the dedicated switch available on module. Please check par. 3.2.3.

## 4.2 Main menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

### 4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

**Note:** The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

# 4.3 Advanced menu

| Menu Item | Options | Description |
|---|---|---|
| AMD CBS | See submenu | AMD CDS Setup Page |
| AMD PBS | See submenu | AMD PBS Setup Page |
| Intel® I210 Gigabit Network Connection – *MAC Address* | See submenu | Configure Gigabit Ethernet device parameters. |
| Battery Failure manager | See submenu | Sets the action to be performed in case of battery failure |
| Trusted Computing | See submenu | Trusted Computing Settings |
| TPM Configuration | See submenu | TPM Selection |
| ACPI Settings | See submenu | System ACPI parameters |
| SATA presence | See submenu | SATA devices Configuration |
| DXIO Settings | See submenu | PEG, PCIE and DDI Lanes configuration |
| S5 RTC Wake Settings | See submenu | Enable System to wake from S5 using RTC alarm |
| Serial Port Console Redirection | See submenu | Serial Port Console redirection |
| CPU Configuration | See submenu | CPU Configuration Parameters |
| AMI Graphic Output Protocol Policy | See submenu | User Selected Monitor Output by Graphic Output protocol |
| PCI Subsystem Settings | See submenu | PCI Subsystem Settings |
| Network Stack Configuration | See submenu | Network Stack Settings |
| CSM Configuration | See submenu | Compatibility Support Module (CSM) Configuration: Enable/Disable, Option ROM execution Settings, etc... |
| NVMe Configuration | See submenu | NVMe Device Options Settings |
| USB Configuration | See submenu | USB Configuration Parameters |
| Main Thermal Configuration | See submenu | Main thermal Configuration |
| SMBIOS Information | See submenu | SMBIOS Information |
| Embedded Controller | See submenu | Embedded Controller Parameters |

### 4.3.1 AMD CBS submenu

| Menu Item | Options | Description |
|---|---|---|
| NBIO Common options | See submenu | NorthBridge IO Configuration Options |
| FCH Common options | See submenu | Firmware Controller Hub Configuration options |

#### *4.3.1.1 NBIO Common Options submenu*

| Menu Item | Options | Description |
|---|---|---|
| GFX Configuration | See submenu | GFX Configuration options |
| IOMMU | Auto / Disabled / Enabled | Enable or disable the support for IOMMU (IO Memory Management Unit. Also known as AMD Virtualization™ Technology). |
| PSPP Policy | Disabled<br>Performance<br>Balanced-high<br>Balanced-Low<br>Power Saving<br>Auto | PCIe Speed Power policy: the processor can dynamically support the changing to the link frequency due to changes in system configuration and power policy. |
| System Configuration | 12W POR Configuration/<br>15W POR Configuration/<br>25W POR Configuration/<br>35W POR Configuration/<br>45W POR Configuration/<br>54W POR Configuration/<br>Auto | Allows selecting the Power Scheme configuration for the CPU.<br>Warning: by selecting a precise configuration, may cause the system to hang, as some System Configurations may not be supported by your OPN. |
| Audio Codecs | All Enabled<br>SDIN0 only<br>All Disabled | Disable/Enable Audio Codecs input signals SDINx |

#### 4.3.1.1.1 GFX Configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| Integrated Graphics Controller | Auto / Disabled / Forces | Enable Integrated Graphics Controller. If disabled, all the remaining options will disappear |
| UMA Mode | Auto / UMA_Specified / UMA_Auto | Only available when Integrated Graphics Controller is set to “Forces”. Allows setting the Unified Memory Architecture (UMA) Frame Buffer Size or Display Resolution |
| UMA Version | Legacy / Non-Legacy / Hybrid Secure / Auto | Only available when Integrated Graphics Controller is set to “Forces”. Sets the supported UMA compatibility. |
| UMA Frame Buffer Size | Auto / 256M / 384M / 512M / 768M / 1G / 2G / 3G / 4G / 8G / 16G | Only available when “UMA Mode” is set to UMA_Specified.<br>Sets UMA Frame Buffer Size |
| Display Resolution | 1920X1080 and below / 2560x1600 / 3840x2160 / Auto | Only available when “UMA Mode” is set to UMA_Auto.<br>Sets Display Resolution |
| Integrated HD Audio Controller | Auto / Disabled / Enabled | Enables or disabled integrated HD Audio Controller |

### *4.3.1.2 FCH Common Options submenu*

| Menu Item | Options | Description |
|---|---|---|
| SATA Configuration Options | See submenu | SATA Configuration Options |
| Uart Configuration Options | See submenu | Uart Configuration Options |

#### 4.3.1.2.1 SATA Configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| SATA Controller | Auto / Disabled / Enabled | Enable or Disable on-chip SATA controller |
| SATA Mode | AHCI<br>AHCI as ID 0x7904<br>Auto<br>RAID | Only available when SATA Controller is set to “Enabled”. Select on-chip SATA Type |

#### 4.3.1.2.2 Uart Configuration Options submenu

| Menu Item | Options | Description |
|---|---|---|
| SER1 Enable<br>SER0 Enable | Auto<br>Disabled<br>Enabled | Enable or Disable SER0 and SER1 ports available on COM Express connector AB. |

### 4.3.2 AMD PBS submenu

| Menu Item | Options | Description |
|---|---|---|
| AMD Firmware Version | | Opens an information page with all details about the Firmware |
| Primary Video Adaptor | Int. Graphics (IGD)<br>Ext. Graphics (PEG) | Allows to select if Internal Graphics controller (IGD) or external PCI-e Graphic Controller x8 (PEG) should be used as a Primary display |

### 4.3.3 Intel® I210 Gigabit Network Connection – *Mac* Address submenu

| Menu Item | Options | Description |
|---|---|---|
| NIC Configuration | See submenu | Allows configuring the network device port |
| Blink LEDs | 0..15 | Blink LEDs for a duration up to 15 seconds |

#### *4.3.3.1 NIC Configuration submenu*

| Menu Item | Options | Description |
|---|---|---|
| Link Speed | Auto Negotiated<br>10 Mbps Half<br>10 Mbps Full<br>100 Mbps Half<br>100 Mbps Full | Specifies the port speed used for the selected boot protocol |
| Wake On LAN | Disabled / Enabled | Enables or Disabled powering on the system via LVAN. Please note that configuring Wake On LAN in the OS does not change the value of this setting, but overrides the behavior of Wake on LAN in OS-controlled power states. |

### 4.3.4 Battery Failure Manager submenu

| Menu Item | Options | Description |
|---|---|---|
| Battery Failure Action | None<br>Restore Defaults<br>Restore NVRAM | Sets the action that must be done when a backup battery failure occurs.<br>None: no action<br>Restore defaults: restore BIOS factory default, preserving the password(s)<br>Reset NVRAM: restore all factory defaults, clearing also the password(s) |

### 4.3.5 Trusted computing submenu

| Menu Item | Options | Description |
|---|---|---|
| Security Device Support | Disabled / Enabled | Enables or Disables BIOS Support for security devices. OS will not show Security Device, TCG EFI protocol and INT1A interface will not be available.<br>When disabled, all following items will disappear. |
| Pending operation | None<br>TPM Clear | Schedule an operation for the Security Device. Note: your computer will reboot during restart in order to change the State of Security Device. |
| Platform Hierarchy | Disabled / Enabled | Enable or Disable Platform Hierarchy |
| Storage Hierarchy | Disabled / Enabled | Enable or Disable Storage Hierarchy |
| Endorsement Hierarchy | Disabled / Enabled | Enable or Disable Endorsement Hierarchy |
| TPM2.0 UEFI Spec Version | TCG_1_2<br>TCG_2 | Select the TCG2 Spec version Support.<br>TCG_1_2 is the compatible mode for Windows 8 and Windows 10<br>TCG_2 supports the new TCG2 protocol and event format for Windows 10 and later |
| Physical Presence Spec Version | 1.2 / 1.3 | Tells the OS to support PPI Spec version 1.2 or 1.3. Note that some HCK tests might not support 1.3 |
| Device Select | Auto<br>TPM 1.2<br>TPM 2.0 | TPM 1.2 will restrict the support to TPM 1.2 devices only, TPM 2.0 will restrict the support to TPM 2.0 devices only, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated |

### 4.3.6 TPM selection submenu

| Menu Item | Options | Description |
|---|---|---|
| TPM selection | AMD CPU fTPM<br>LPC TPM | Allows to choose whether using AMD processor Firmware TPM or use onboard (optional) LPC TPM |

### 4.3.7 ACPI Settings

| Menu Item | Options | Description |
|---|---|---|
| Enable ACPI Auto Configuration | Disabled / Enabled | Enables or Disables BIOS ACPI Auto Configuration. The following menu items will appear only when this menu item is Disabled |
| Enable Hibernation | Disabled / Enabled | Enables or disables system ability to Hybernate (OS/S4 Sleep State). This option may be not effective with some OS. |
| ACPI Sleep State | Suspend Disabled<br>S3 (Suspend to RAM) | Select the highest ACPI Sleep state the system will enter when the SUSPEND button is pressed. |
| Lock Legacy resources | Disabled / Enabled | Enables or Disables Lock of Legacy resources |

### 4.3.8 SATA presence submenu

| Menu Item | Options | Description |
|---|---|---|
| SATA Port 0<br>SATA Port 1 | | Shows information related to eventual devices connected to SATA ports 0 or 1. |

### 4.3.9 DXIO Settings submenu

| Menu Item | Options | Description |
|---|---|---|
| DDI Port | See submenu | Allows enabling and configuring the single DDI ports |
| PEG lanes aggregation | 1x8<br>2 x4 | Allow selecting how the PCI Express Graphics (PEG) x16 lanes must be managed. Allowed configurations are: a single port x8 (default) or 2 ports x4 |
| PEG Port | See submenu | Allows enabling and configuring the PEG port(s) |
| PCIe lanes aggregation | x1x1x1x1<br>x2x1x1<br>x2x2<br>x4 | Allow selecting how the SOC's PCI Express lanes #0.. #3 must be managed. Allowed configurations are: a single port x4, 2 ports x2, 1 port x2 + 2 ports x1 or 4 ports x1 |
| PCI-E Port | See submenu | Allows enabling and configuring the PCI-e ports |

#### 4.3.9.1 DDI Port submenu

| Menu Item | Options | Description |
|---|---|---|
| DDI 0 State<br>DDI 1 State<br>DDI 2 State | Disabled<br>Enabled | Enable or Disable DDI ports 0, 1 and 2. |
| eDP/LVDS State | Disabled<br>Enabled<br>Force DP | Disable or enable eDP or LVDS Port (which one is available depends on module configuration) |

#### 4.3.9.2 PEG Port submenu

| Menu Item | Options | Description |
|---|---|---|
| PEG0 port<br>PEG1 port | Enabled / Disabled | Enable or disable each single PEG port (PEG port 1 will be available only in case PEG is managed as 2 PEG x4 ports). When enabled, all following items will appear. |
| ASPM Mode Control | Disable / L0s Entry | Disable or Enable PCI Express Active State Power Management |
| Link Speed | PCIe Gen1<br>PCIe Gen2<br>Max Speed<br>Auto | Configures NB Root Port PCIe Link Speed, which can however be overwritten by PSPP Settings |
| Hot Plug Mode Control | Auto<br>Disabled<br>Hotplug Basic<br>Hotplug Server<br>Hotplug Enhanced<br>Hotplug Inboard | PCI Express Root Port Hot Plug Mode Control |

#### *4.3.9.3 PCI-E Port submenu*

| Menu Item | Options | Description |
|---|---|---|
| PCIE0 port<br>PCIE1 port<br>PCIE2 port<br>PCIE3 port<br>PCIE4/5 ports + Internal LAN | Enabled / Disabled | Enable or disable each single PCIE port (the ports effectively shown will depend on the Link aggregation).<br>PCIE ports 4 and 5 can only be enabled or disabled at a same time, along with the Internal LAN.<br>When enabled, all following items will appear. |
| ASPM Mode Control | Disable / L0s Entry | Disable or Enable PCI Express Active State Power Management |
| Link Speed | PCIe Gen1<br>PCIe Gen2<br>Max Speed<br>Auto | Configures NB Root Port PCIe Link Speed, which can however be overwritten by PSPP Settings |
| Hot Plug Mode Control | Auto<br>Disabled<br>Hotplug Basic<br>Hotplug Server<br>Hotplug Enhanced<br>Hotplug Inboard | PCI Express Root Port Hot Plug Mode Control |

### 4.3.10 S5 RTC Wake Settings submenu

| Menu Item | Options | Description |
|---|---|---|
| Wake system from S5 | Disabled<br>By Every Day<br>By Day of Month | Enables or disables System Wake on Alarm event.<br>The following menu items will appear only when this voice is not set to Disabled |
| Wake up hour | 0..23 | Sets the wake up hour in 0..23 format (i.e.,3 means 3am, 15 means 3pm) |
| Wake up minute | 0..59 | Sets the wake up minute |
| Wake up second | 0..59 | Sets the wake up second |
| Day of Month | 1..31 | This item is available only when “Wake system from S5” is set to “By Day of Month”.<br>Sets the day of month for Wake on Alarm event. Valid range s from 1 to 31, error checking will be done against month/day/year combinations that are not valid. |

### 4.3.11 Serial Port Console Redirection submenu

| Menu Item | Options | Description |
|---|---|---|
| Console Redirection | Enabled / Disabled | Enable or disable Console redirection. This can be done both on Serial Port 0 and Serial Port 1 and for Windows Emergency Management Services (EMS) console. |
| Console Redirection Settings | See submenu | When any of the Serial port Console Redirections is enabled, this submenu will appear |

#### *4.3.11.1 Console Redirection Settings submenus*

| Menu Item | Options | Description |
|---|---|---|
| Terminal Type | VT_100 / VT_100+ / VT_UTF8 / ANSI | Set Console Redirection terminal type |
| Bits per second | 115200 / 57600 / 38400 / 19200 / 9600 | Set Console Redirection baud rate |
| Data Bits | 7 / 8 | Set Console Redirection data bits |
| Parity | None / Even / Odd / Mark / Space | Set Console Redirection parity bits |
| Stop Bits | 1 / 2 | Set Console Redirection stop bits |
| Flow Control | None<br>Hardware RTS/CTS | Set Console Redirection flow control type |
| VT-UTF8 Combo Key Support | Enabled / Disabled | Enable or Disable VT-UTF8 Combination Key Support for ANSI/VT100 terminals |
| Recorder Mode | Enabled / Disabled | With this mode enabled only text will be sent. This is to capture Terminal data. |
| Resolution 100x31 | Enabled / Disabled | Enables or disables extended terminal resolution |
| Putty Keypad | VT100 / Linux / XTermr6 / SCO / ESCN / VT400 | Select FunctionKey and KeyPad on Putty |

### 4.3.12 CPU configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| PSS Support | Enabled / Disabled | Enable/disable the generation of ACPU _PCC, _PSS and _PCT objects |
| PPC Adjustment | PState 0 | Only Available when PSS Support is enabled |
| NX Mode | Enabled / Disabled | Enables or Disables No-execute Page Protection Function |
| SVM Mode | Enabled / Disabled | Enables or disables CPU Virtualization |
| PSTATE Adjustment | PState 0 / Pstate 1 / Pstate 2 / Pstate 3 / Pstate 4 / Pstate 5 / Pstate 6 / Pstate 7 | Provide to adjust startup P-state level |
| CPB Mode | Enabled / Disabled | Enables or disables CPB |
| C6 Mode | Enabled / Disabled | Enables or disables C6 |
| Node 0 Information | | Opens an information page with the Memory Information details related to Node 0 |

### 4.3.13 AMI graphic Output Protocol Policy submenu

| Menu Item | Options | Description |
|---|---|---|
| Output Select | *List of available / connected module's video interfaces* | |

### 4.3.14 PCI Subsystem Settings submenu

| Menu Item | Options | Description |
|---|---|---|
| Above 4G Decoding | | Globally Enabled or Disabled 64-bitcapable Devices to be decoded in Address Space above 4GB (only if system supports 64-bit PCI Decoding). |
| SR-IOV Support | Disabled / Enabled | If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support. |
| BME DMA Mitigation | Disabled / Enabled | Re-enable Bus Master Attribute disabled during PCI enumeration for PCI Bridges after SMM has been locked |

### 4.3.15 Network Stack configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| Network Stack | Enabled / Disabled | Enables or disables UEFI Network Stack. When enabled, following menu items will appear |
| Ipv4 PXE Support | Enabled / Disabled | Enables or disables IPV4 PXE Boot Support. If disabled, IPV4 PXE boot option will not be created |
| Ipv4 HTTP Support | Enabled / Disabled | Enables or disables IPV4 HTTP Boot Support. If disabled, IPV4 HTTP boot option will not be created |
| Ipv6 PXE Support | Enabled / Disabled | Enables or disables IPV6 PXE Boot Support. If disabled, Ipv6 PXE boot option will not be created |
| Ipv6 HTTP Support | Enabled / Disabled | Enables or disables IPV6 HTTP Boot Support. If disabled, Ipv6 HTTP boot option will not be created |
| IPSEC certificate | Enabled / Disabled | Support to Enable/Disable IPSEC certificate for Ikev. |
| PXE boot wait time | [0..5] | Wait time to press ESC key to abort the PXE boot |
| Media detect count | [1..50] | Number of times that the presence of media will be checked |

### 4.3.16 CSM configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| CSM Support | Enabled / Disabled | Enables or disables the Compatibility Support Module (CSM) Support. When enabled, the following menu items will appear |
| GateA20 Active | Upon Request<br>Always | Upon Request: GateA20 can be disabled using BIOS services,<br>Always: do not allow disabling GateA20; this option is useful when any RT code is executed above 1MB. |
| INT19 Trap Response | Immediate<br>Postponed | BIOS Reaction on INT19 trapping by Option ROM:<br>IMMEDIATE - execute the trap right away;<br>POSTPONED - execute the trap during legacy boot |
| Boot option filter | UEFI and Legacy<br>Legacy only<br>UEFI only | This option controls Legacy / UEFI ROMs priority |
| Network | Do not launch<br>UEFI<br>Legacy | Controls the execution of UEFI and Legacy PXE OpROM |
| Storage | Do not launch<br>UEFI<br>Legacy | Controls the execution of UEFI and Legacy Storage OpROM |
| Video | Do not launch<br>UEFI<br>Legacy | Controls the execution of UEFI and Legacy Video OpROM |
| Other PCI devices | Do not launch<br>UEFI<br>Legacy | Determines the OpROM execution policy for devices other than Network, Storage and Video |

### 4.3.17 NVMe configuration submenu

NVMe Device Options Settings, depend on NVMe Devices found in the system.

### 4.3.18 USB configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| Legacy USB Support | Enabled / Disabled / Auto | Enables Legacy USB Support. AUTO Option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications. |
| XHCI hand-off | Enabled/ Disabled | This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver. |
| USB Mass Storage Driver Support | Enabled/ Disabled | Enables or disables USB Mass Storage Driver Support |
| USB Transfer time-out | 1 sec / 5 sec / 10 sec / 20 sec | Sets the time-out value for Control, Bulk and Interrupt transfers |
| Device reset time-out | 10 sec / 20 sec / 30 sec / 40 sec | USB mass storage device Start Unit command time-out |
| Device power-up delay | Auto / Manual | Sets the maximum time that the device will take before it properly reports itself to the Host controller. 'Auto' uses the default vale (for a Root port it is 100ms, for a Hub port the delay is taken from the Hub descriptor). |
| Device power-up delay in seconds | [1..40] | Delay range in seconds, in one second increment |

### 4.3.19 Main Thermal Configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| Critical Temperature (°C) | 80 .. 100 | Above this threshold, an ACPI aware OS will perform a critical shut-down. Allowed range is from 80 to 100, where 100 means disabled. |
| Passive Cooling Temperature (°C) | 75 .. 90 | This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin lowering the CPU speed. Allowed range is from 75 to 90, where values above Critical Temperature means Disabled. |

### 4.3.20 SMBIOS Information

Display only screen, shows information about the module and the Carrier board.

### 4.3.21 Embedded Controller submenu

| Menu Item | Options | Description |
|---|---|---|
| Hardware Monitor | | By selecting this item, an information screen with System parameters will appear |
| Watchdog configuration | See Submenu | Configures the Embedded Controller's Watchdog Timer |
| Internal FAN Settings | See Submenu | Sets the parameters for Internal (i.e. on-module) FAN |
| External FAN/PWM Settings | See Submenu | Sets the parameters for external (i.e. on-carrier FAN |
| COM- Express GPIO Configurations | See Submenu | Configures GPOs management |
| Reset Causes Handling | | By selecting this item, an information screen with the handling of latest resets causes will appear. |
| Boot with battery low | Normal<br>Force S5 | When this item is set to Normal, BATLOW# signal will be ignored. When set to Force S5, the system is not allowed to leave S5 state until BATLOW# signal is asserted. |
| Batteryless Operation | Disabled / Enabled | Enable this item in case the CMOS Battery is not present. |
| Power Fail resume Type | Always ON<br>Always OFF<br>Last State | Specifies what must happen when power is re-applied after a power failure (G3 state).<br>Always ON: the System will boot directly as soon as the power is applied.<br>Always OFF: the system remain in power off State until power button is pressed |
| LID# Configuration | Force Open<br>Force Closed<br>Normal Polarity<br>Inverted Polarity | Configures the LID_BTN# signal as always open or closed, no matter the pin level, or configures the pin polarity: High = Open (Normal), Low = Open (Inverted) |
| LID_BTN# Wake Configuration | No Wake<br>Only From S3<br>Wake From S3/S4/S5 | Configures LID_BTN# wake capability (when not forced to Open or Closed). According to the pin configuration, when the LID is open it can cause a system wake from a sleep state. |
| SLEEP# Wake | Disabled / Enabled | Disable or Enable SLEEP# Wake capability from S3/S4 state. |
| SMB_ALERT# Wake Configuration | No Wake<br>Only From S3<br>Wake From S3/S4/S5 | Configures SMB_ALERT# wake capability: when asserted, it can cause the system wake from a sleep state. |

#### *4.3.21.1 Watchdog Configuration submenu*

| Menu Item | Options | Description |
|---|---|---|
| Watchdog Status | Disabled / Enabled | Enables or disables the Watchdog. When diabled, all following items will disappear |
| Event action | Raisw WDT Signal<br>Power Button Pulse<br>None | Action executed at the expiring of the Event time-out. |
| Reset action | System Reset<br>Power Button Override<br>Raise WDT Signal | Action executed at the expiring of the reset time-out. |
| Watchdog Delay | 0 / 1 / 2 / 4 / 8 / 16 / 32 / 64 | Minutes before watchdog normal operations start. During delay time-out, a refresh operation will immediately trigger the normal operation. |
| Event Timeout | 0 / 1 / 2 / 4 / 8 / 16 / 32 / 64 | Time-out minutes that can pass without refresh before triggering the Event Action. A refresh will restart the time-out. |
| Reset Timeout | 1 / 2 / 4 / 8 / 16 / 32 / 64 | Time-out minutes that can pass without refresh before triggering the Reset Action, this timer will start counting when event time-out is expired.. A refresh will restart the time-out. |

#### *4.3.21.2 Internal FAN Settings submenu*

| Menu Item | Options | Description |
|---|---|---|
| Internal FAN Control | Enabled / Disabled | Disable or Enable Thermal Feedback FAN Control |
| AC0 Temperature (°C) | 70 / 75 / 80 / 85 / 90 / 95 / 100 | Only available when "Internal FAN Control" is Enabled<br>Select the highest temperature above which the onboard fan must work always at Full Speed |
| AC1 Temperature (°C) | 5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 | Only available when "Internal FAN Control" is Enabled.<br>Select the lowest temperature under which the onboard fan must be OFF. |
| Temperature Hysteresis | 0 .. 10 | Only available when "Internal FAN Control" is Enabled.<br>Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations. |
| FAN Duty Cycle (%) Above AC1 | 0 .. 100 | Only available when "Internal FAN Control" is Enabled.<br>Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed. |
| FAN Duty Cycle (%) Above AC0 | 0 .. 100 | Only available when "Internal FAN Control" is Enabled.<br>Use this item to set the Duty Cycle for the fan when the CPU temperature is above AC0 threshold. |
| Speed Change Duration | 0 .. 50 | Only available when "Internal FAN Control" is Enabled.<br>Duration in seconds of linear FAN Speed Change. |
| FAN Duty Cycle | 0 .. 100 | Only available when "Internal FAN Control" is Disabled.<br>Default FAN Duty Cycle (%). |

#### *4.3.21.3 External FAN/PWM Settings submenu*

| Menu Item | Options | Description |
|---|---|---|
| FAN_PWMOUT Device Type | 3-Wire FAN<br>4-Wire FAN<br>Generic PWM | Specifies if a 3-Wire (Default) or a 4-Wire FAN is connected to FAN_PWMOUT / FAN_TACHOIN signals. Generic PWM has to be used when the signal is not used to drive a FAN. |
| FAN_PWMOUT frequency | 1 .. 60.000 | Sets the frequency of the FAN_PWMOUT signal. If fed to a FAN, typical values are 100 for a 3-Wire device and 20.000 for a 4-Wire one. |
| External FAN Control | 0 .. 100 | Only available when “External FAN Type” is not set to Generic PWM.<br>Disable or Enable Thermal Feedback FAN Control |
| AC0 Temperature (°C) | 70 / 75 / 80 / 85 / 90 / 95 / 100 | Only available when “External FAN Control” is Enabled<br>Select the highest temperature above which the external fan must work always at Full Speed |
| AC1 Temperature (°C) | 5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 | Only available when “External FAN Control” is Enabled.<br>Select the lowest temperature under which the external fan must be OFF. |
| Temperature Hysteresis | 0 .. 10 | Only available when “External FAN Control” is Enabled.<br>Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations. |
| FAN Duty Cycle (%) Above AC1 | 0 .. 100 | Only available when “External FAN Control” is Enabled.<br>Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed. |
| Speed Change Duration | 0 .. 50 | Only available when “External FAN Control” is Enabled.<br>Duration in seconds of linear FAN Speed Change. |
| FAN Duty Cycle (%) | 0 .. 100 | Only available when “FAN_PWMOUT Device Type” is not set to Generic PWM and External FAN Control is Disabled.<br>Default FAN Duty Cycle (%) |
| FAN_PWMOUT Duty Cycle (%) | 0 .. 100 | Only available when “FAN_PWMOUT Device Type” is set to Generic PWM.<br>Default FAN_PWMOUT Duty Cycle (%) during boot |

#### *4.3.21.4 COM-Express GPIO Configurations submenu*

| Menu Item | Options | Description |
|---|---|---|
| GPO0<br>GPO1<br>GPO2<br>GPO3 | Low<br>High<br>Last | Fix the GPOx starting level. Last means no change with respect to the last boot. |

# 4.4 Chipset menu

| Menu Item | Options | Description |
|---|---|---|
| South Bridge | See Submenu | South Bridge Parameters |
| North Bridge | See Submenu | North Bridge Parameters |

## 4.4.1 South Bridge Configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| SB USB Configuration | See submenu | USB configuration Settings |

### *4.4.1.1 SB USB Configuration submenu*

| Menu Item | Options | Description |
|---|---|---|
| COM-Express USB 0<br>COM-Express USB 1<br>COM-Express USB2/USB3<br>COM-Express USB4/5/6/7 | Enabled / Disabled | Enables or Disables every USB Port / group of USB ports. |
| USB OverCurrent | Enabled / Disabled | Enables or Disables USB OverCurrent Signals |

## 4.4.2 North Bridge Configuration submenu

| Menu Item | Options | Description |
|---|---|---|
| Memory Configuration | See submenu | Memory configuration Settings |
| Socket 0 Configuration<br>Socket 1 Configuration | | By selecting this item, an information screen with all information related to the memory module plugged in Socket #x will appear |

#### *4.4.2.1 Memory Configuration submenu*

| Menu Item | Options | Description |
|---|---|---|
| Memory Clock | Auto / 1333MHz / 1600MHz / 1866MHz/ 2133MHz / 2400MHz | This option allows the user to select different memory clocks. Default value is 800MHz |
| Bank Interleaving | Enabled / Disabled | Enables or disables memory bank interleaving |
| Channel Interleaving | Enabled / Disabled | Enables or disables memory channel interleaving |
| Memory Clear | Enabled / Disabled | Enables or disables memory clear function |

# 4.5 Security menu

| Menu Item | Options | Description |
|---|---|---|
| Administrator Password | | Set Administrator Password |
| User Password | | Set User Password (possible only if also Administrator Password has been set) |
| Secure Boot | See Submenu | Customizable Secure Boot Settings |

## 4.5.1 Secure Boot submenu

| Menu Item | Options | Description |
|---|---|---|
| Secure Boot | Enabled / Disabled | Secure Boot is activated when the Platform Key (PK) is enrolled, System Mode is User/Deployed and CSM function is disabled. |
| Secure Boot Customization | Standard / Custom | Set UEFI Secure Boot Mode to Standard Mode or Custom mode. In Custom Mode, Secure Boot Policy variables can be configured by a physically present user without full authentication |
| Restore Factory Keys | | Only accessible when Secure Boot Mode is set to Custom<br>Force System to User Mode. Install Factory default Secure Boot key databases. |
| Reset to Setup Mode | | Delete all Secure Boot key databases from NVRAM |
| Key management | See submenu | Only accessible when Secure Boot Mode is set to Custom<br>Enable expert users to modify Secure Boot Policy variables without full authentication |

#### *4.5.1.1 Key Management submenu*

| Menu Item | Options | Description |
|---|---|---|
| Factory Key Provision | Disabled / Enabled | Install factory default Secure Boot Keys after the platform reset and while the System is in Setup Mode |
| Restore Factory Keys | | Force System to User Mode. Install factory Default Secure Boot key databases |
| Reset to Setup Mode | | Delete all Secure Boot key databases from NVRAM |
| Export Secure Boot variables | | Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device |
| Enrol Efi Image | *File System Image* | Allow the selected image to run in Secure Boot mode. Enrol SHA256 Hash Certificates of a PE Image into Authorized Signature Database (db) |
| Remove 'UEFI CA' from DB | | Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature Database (db) |
| Restore DB defaults | | Restore DB variable to factory defaults |
| Platform key<br>Key Exchange Keys<br>Authorized Signatures<br>Forbidden Signatures<br>Authorized Timestamps<br>OS Recovery Signatures | Details<br>Export<br>Update<br>Delete | Enrol factory Defaults or load certificates from a file:<br>1. Public Key Certificate in:<br>a) EFI_SIGNATURE_LIST<br>b) EFI_CERT_X509 (DER)<br>c) EFI_CERT_RSA2048 (bin)<br>d) EFI_CERT_SHAXX<br>2. Authenticated UEFI variables<br>3. EFI PE/COFF Image (SHA256)<br>Key Source:<br>Factory, External, Mixed |

# 4.6 Boot menu

| Menu Item | Options | Description |
|---|---|---|
| Setup Prompt Timeout | 0 .. 65535 | Number of seconds to wait for setup activation key. 655535 means indefinite waiting. |
| Bootup NumLock State | On / Off | Select the Keyboard NumLock State at boot |
| Quiet Boot | Enabled / Disabled | Enables or Disables Quiet Boot options |
| Fast Boot | Enabled / Disabled | When Fast Boot is enabled, most probes are skipped to reduce time cost during boot |
| New Boot Option Policy | Default<br>Place First<br>Place Last | Controls the placement of newly detected UEFI boot devices |
| Boot Mode Select | LEGACY<br>UEFI | Select the boot mode between Legacy and UEFI |
| Boot Option #1<br>Boot Option #2<br>Boot Option #3<br>Boot Option #4<br>Boot Option #5<br>Boot Option #6 | Hard Disk<br>CD/DVD<br>SD<br>USB Device<br>Network<br>Other Device: ubuntu<br>Disabled | Select the system boot order |

**!**

Please be aware that by deault only UEFI boot is enabled. In this situation, when using legacy MBR drives, the system will not boot from them. To fully enable the boot form legacy drives, it is necessary to set the following items:

- Boot menu → “Boot mode select”: must be set to Legacy
- Advanced menu → CSM Configuration submenu → “CSM support” must be Enabled
- Advanced menu → CSM Configuration submenu → “Video” must be set to Legacy

# 4.7 Save & Exit menu

| Menu Item | Options | Description |
|---|---|---|
| Save Changes and Exit | | Exit system setup after saving the changes. |
| Discard Changes and Exit | | Exit system setup without saving any changes. |
| Save Changes and Reset | | Reset the system after saving the changes. |
| Discard Changes and Reset | | Reset the system without saving any changes. |
| Save Changes | | Save the changes done so far to any of the setup options. |
| Discard Changes | | Discard the changes done so far to any of the setup options. |
| Restore Defaults | | Restore/Load Default values for all the setup options |
| Save as User Defaults | | Save the changes done so far as User Defaults |
| Restore User Defaults | | Restore the User Defaults to all the setup options |
| *List of EFI boot options* | | |
| Launch EFI Shell from filesystem device | | Attempt to Launch the EFI Shell application (Shell.efi) from one of the available filesystem devices |

# Chapter 5.
# Appendices

- Thermal Design

# 5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-B75-CT6 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-B75-CT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-B75-CT6 specific heatspreaders and active heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

| Ordering Code | Description |
|---|---|
| MB75-DISS-1-PK | COMe-B75-CT6 Heat Spreader (passive) – packaged |
| MB75-DISS-3-PK | COMe-B75-CT6 Heat Sink (active) – packaged |

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