Com express

User Manual

COMe-A98 CT6

COM-Express™ Type 6 Module with the
AMD Embedded 3rd Generation
R-Series or G-Series SoC-I Platforms

www.seco.com

REVISION HISTORY

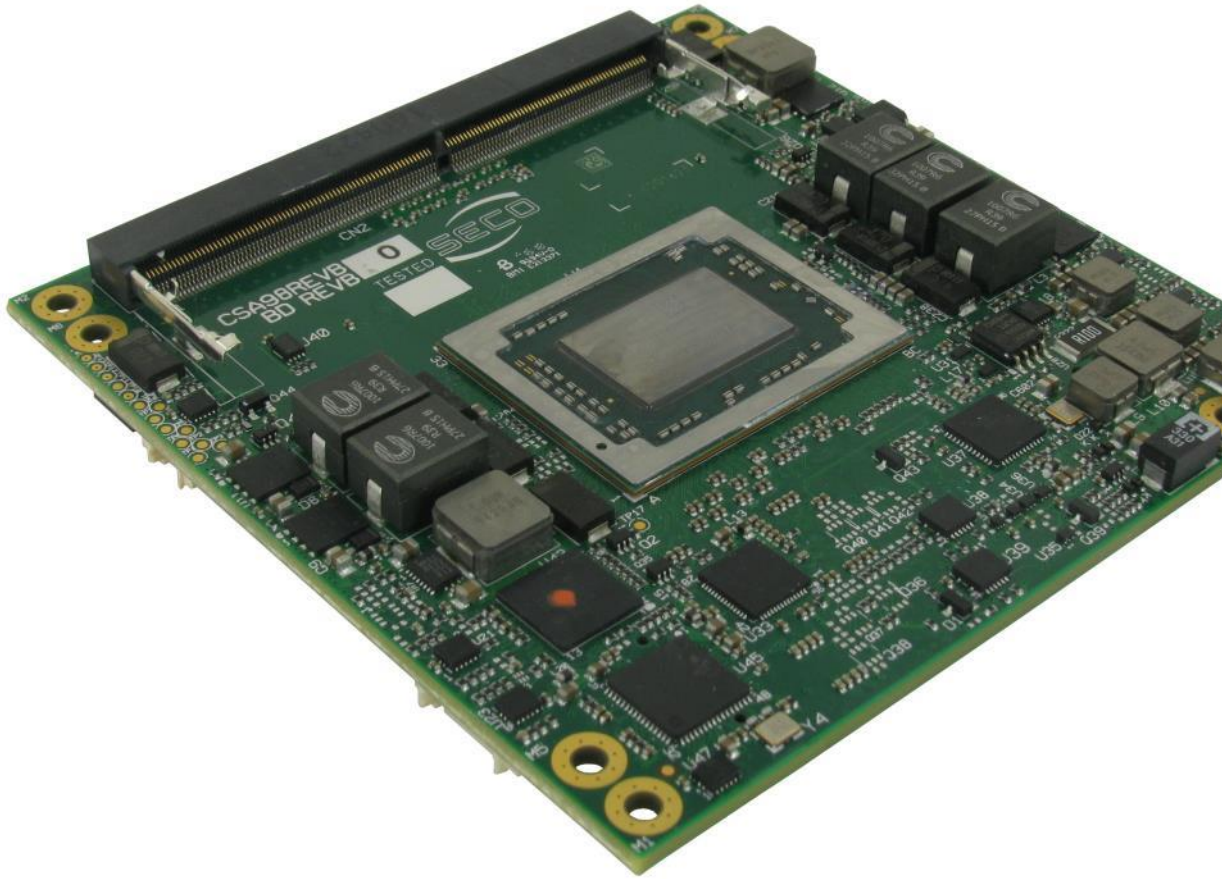
Revision	Date	Note	Rif
1.0	26th July 2016	First Release	SB
1.1	15th November 2016	Introduced G-Series SoC-I support; removed UART support Bios Section updated	SB
1.2	22nd November 2016	PCI-e speed specifications corrected on paragraph 3.2.3.4 and 3.2.3.5	SB
1.3	20th December 2016	Max memory speed supported corrected	SB
1.4	18th January 2017	Block diagram correction	SB
1.5	9th June 2017	HS-UART support added Power consumption and inrush current paragraphs updated Mechanical dimensions drawing corrected DP-to-VGA bridge p/n changed (affects only modules with PCB rev.C or higher) BIOS Section updated. Thermal Design section updated	SB
1.6	26th October 2018	Terminology and Definitions section updated Power rail names changed, reference schematics updated BIOS Section updated	SB

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required). Our team is ready to assist you.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The COMe-A98-CT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The COMe-A98-CT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a COME-A98-CT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The COMe-A98-CT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR4	DDR, 4th generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GT/s	Gigatransfers per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable
N.C.	Not Connected

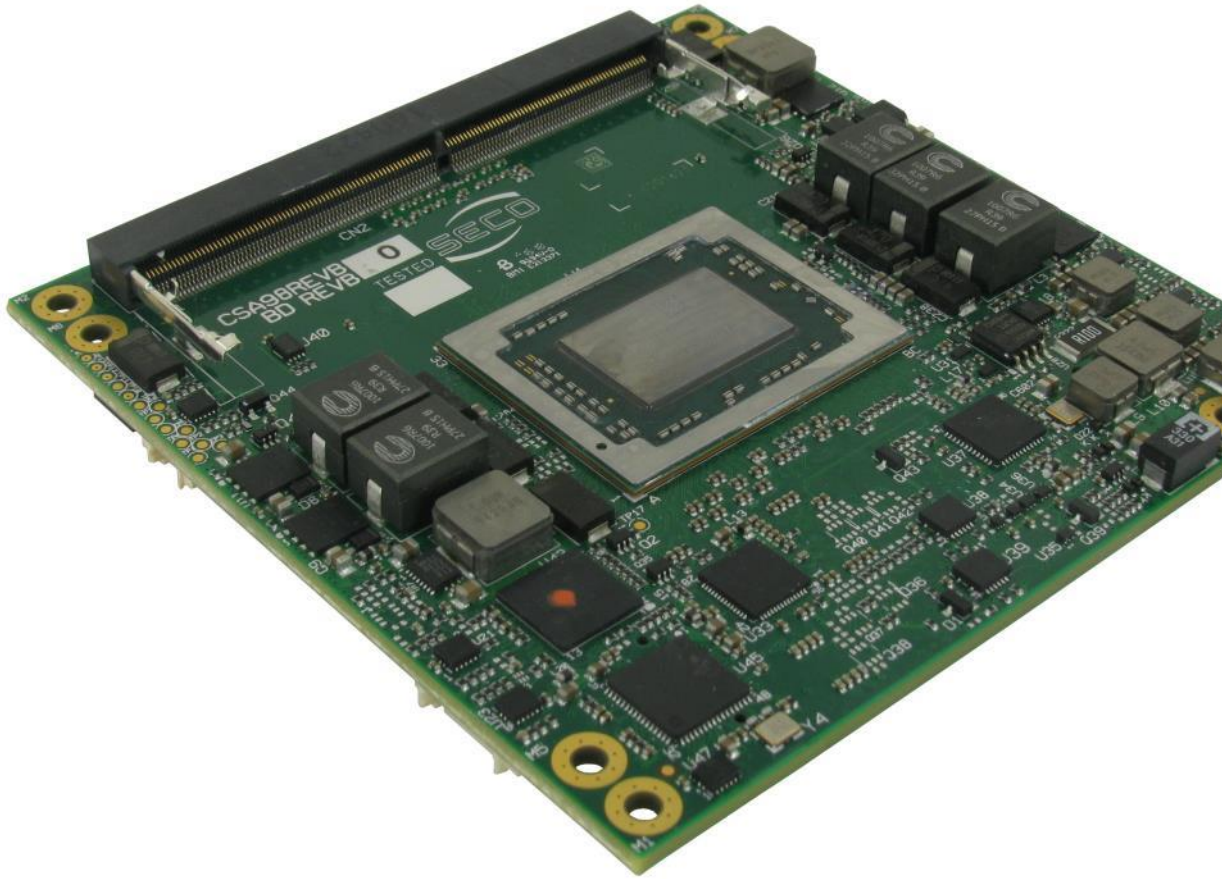
OS	Operating System
PCI-e	Peripheral Component Interface Express
PCR	Platform Component Register. Component of TPM which allows secure storage and reporting of security relevant metrics.
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like smart batteries and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TPM	Trusted Platform Module, international standard for secure cryptography
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage Reference
VGA	Video Graphics Array. An analog computer display standard, commonly referred to also as CRT.
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

1.8 Reference specifications

Reference	Link
ACPI	http://www.uefi.org/acpi/specs
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com Express	https://www.picmg.org/openstandards/com-express/
Com Express Carrier Design Guide	http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://cache.nxp.com/documents/user_manual/UM10204.pdf?fsrch=1&sr=5&pageNum=1
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org
SM Bus	http://www.smbus.org/specs
UEFI	http://www.uefi.org
USB 2.0	http://www.usb.org/developers/docs/usb20_docs/usb_20_040816.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
xHCI	http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html?wapkw=xhci
AMD R-Series Processors	http://www.amd.com/en-us/products/embedded/processors/r-series#
AMD G-Series SoC I family	http://www.amd.com/Documents/I-Family-Product-Brief.pdf

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

The COMe-A98-CT6 is a COM Express® type 6, Compact Form Factor, based on the AMD embedded 3rd Generation R-Series (“Merlin Flacon”) of System On Chips (SoCs), or alternatively 3rd Generation G-Series SoC-l (“Brown Falcon”). A complete list of processors available is detailed in the next chapter.

All of these SoCs are Dual- or Quad-Core, offer a 64-bit Instruction set and provide direct access to the memory, which is available on two SODIMM DDR4 memory modules, with the support of frequencies up to 2133MHz. Both ECC and non-ECC memory modules are supported. The total amount of memory available is OS dependant.

All SoCs integrate an AMD Radeon GPU, 3rd Generation Graphics Core Next, which offer an advanced 2D and 3D graphic engine, able to manage up to 3 independent displays using the native Digital Display Interfaces (DDIs). On all DDIs, it is possible to support DP++, DVI/HDMI and eDP interfaces. As factory options, it is possible to have also one LVDS and/or one VGA interface by using dedicated bridges. Both the implementation of the LVDS interface and of the VGA interface would exclude one DDI interface each. Since the G-Series “Brown Falcon” SoC-l has only two DDI interfaces, the modules equipped with that SoC cannot offer neither eDP nor LVDS interface.

Further graphical possibilities are given by the SoC’s PCI Express graphics (PEG) x8 interface. Such an interface can be used as a single PCI-e x8 port or two PCI-e x 4 independent ports. The G-Series SoC-l, instead, offers only a PEG x4 interface

All the SoCs available on this module offer four PCI-express x 1 Gen 3 ports; three of them are carried out externally, the other port is used to manage a Gigabit Ethernet controller.

The SoCs functionalities are completed by the Audio HD Interface, 2 x Serial ATA Gen3 channels, 8 USB 2.0 ports, 4 USB 3.0 ports, SD interface (shared with 4 GPIs and 4 GPOs managed by the embedded microcontroller), Real Time Clock, LPC and SM Bus.

Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.2.1 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available.

Specifically, COMe-A98-CT6 is a COM Express® module, Compact Form factor, Type 6 (95mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilise as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

SoC

AMD RX-421BD, Quad Core @ 2.1GHz (3.4GHz Max), TDP 35W
AMD RX-418GD, Quad Core @ 1.8 GHz (3.2GHz Max), TDP 35W
AMD RX-216GD, Dual Core @ 1.6 GHz (3.0GHz Max), TDP 15W
AMD RX-416GD, Dual Core @ 1.6 GHz (2.0GHz Max), TDP 15W, Industrial Temperature range
AMD GX-217GI, Dual Core @1.7GHz (2.0GHz Max), TDP 15W

Memory

Two SO-DIMM slots supporting DDR4 ECC / non-ECC modules up to 2133MHz (up to 1600MHz with GX217GI)

Graphics

AMD Radeon 3rd -Generation Graphics Core Next (GCN)
- AMD RX-421BD - Radeon™ R7
- AMD RX-418GD, RX-416GD - Radeon™ R6
- AMD RX-216GD - Radeon™ R5
- AMD GX-217GI - Radeon™ R6E

Up to 3 independent displays supported (up to 2 with GX217GI)
DirectX® 12 supported
Unified Video Decode (UVD) 6 (4K H.265 and H.264 decode)
Video Coding Engine (VCE) 3.1 (4K H.264 encode)

Video Interfaces

Up to 3 x Digital Display interfaces, supporting DP 1.2, DVI and HDMI 1.4 / 2.0
Optional VGA interface (excludes one DDI Port)
Optional eDP **or** Single / Dual-Channel 18- / 24- bit LVDS interface (R-Series SoCs only, excludes one DDI Port)
PCI-express Graphics (PEG) x 8 (x4 with GX217GI)

Video Resolutions

Digital Display interfaces:	up to 3840 x 2160
LVDS, VGA:	up to 1920 x 1200

Mass Storage

2 x S-ATA Gen3 channels
SD Interface shared with GPI/Os

USB

8 x USB 2.0 Host Ports
4 x USB 3.0 Host ports

Networking

Gigabit Ethernet interface
Intel® I210 or I211 GbE controller

Audio

HD Audio interface

PCI Express

3 x PCI-e x1 lanes

Serial Ports

2 x HS UARTs

Other Interfaces

2 x Express Card interfaces
I2C bus
LPC Bus
SM Bus
4 x GPI, 4 x GPO (interface shared with SD)
Thermal / FAN management
SPI Interface
Watch Dog timer
Real Time Clock
Platform Security Processor (PSP)
Power Management Signals

Power supply voltage: +12V_{DC} ± 10% and + 5V_{SB} (optional)

Operating temperature: 0°C ÷ +60°C (commercial temperature range)**
-40°C÷+85°C (industrial temperature range)**

Dimensions: 95 x 95 mm (3.74" x 3.74")

! *** Temperatures indicated (minimum and maximum) are those measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to COM Express® specifications, the COMe-A98-CT6 board needs to be supplied only with an external +12V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN6 and CN7.

All remaining voltages needed for board's working are generated internally from +12V_{DC} power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: RUN voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

_SUS: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_SUS

2.3.2 Power Consumption

COMe-A98-CT6 module, like all COM Express™ modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Therefore, power consumptions of the board are measured using a CCOMe-965 Carrier board on the VCC_12V power rail that supplies the board. For this reason, the values indicated in the table below are real power consumptions of the board, and are independent from those of the peripherals connected to the Carrier Board. For the measurement, it has been used a Keysight DC Power Analyzer mod. N6705C

Power consumption in Suspend and Soft-Off States has been measured on VCC_5V_SBY power rail. RTC power consumption has been measured on carrier board's backup battery when the system is not powered (VCC_RTC power rail).

The current consumptions, written in the table of the next page, have been measured with the following setup:

- O.S. Windows 10 Professional 64-Bit
- BIOS 1.02 RC 11
- 8GB DDR4 (2 x 4GB SO-DIMM DDR4 2133MHz modules, p/n Corsair CMS08GX4M2A2133C15)
- 64GB SATA SSD (p/n Trascend TS64GSSD320) connected
- USB mouse and keyboard connected
- HDMI display Hanns.G HZ281 connected (not during 4K video reproduction)
- HDMI display DELL P2415Q connected (only during 4K video reproduction)
- PSU CORSAIR mod. VS560

Status	SOC									
	RX-421BD		RX-418GD		RX-216GD		RX-416GD		GX-217GI	
	Average	Peak	Average	Peak	Average	Peak	Average	Peak	Average	Peak
Idle, power saving configuration	0.292A	0.527A	0.241A	0.312A	0.228A	0.329A	0.236A	0.484A	0.256A	0.349A
OS Boot, power saving configuration	1.360A	4.852A	1.462A	5.747A	1.329A	2.721A	1.514A	2.938A	1.366A	2.514A
Video reproduction@720p, power saving configuration	0.510A	1.479A	0.508A	1.509A	0.423A	1.300A	0.556A	1.823A	0.533A	1.544A
Video reproduction@1080p, power saving configuration	0.717A	1.806A	0.701A	1.710A	0.498A	1.887A	0.843A	2.107A	0.766A	1.850A
Video reproduction@4K, power saving configuration	1.805A	3.951A	2.181A	3.237A	1.388A	2.479A	1.574A	2.824A	1.383A	2.403A
Internal Stress Test Tool, maximum performance	4.058A	5.067A	4.020A	5.893A	1.600A	2.509A	2.292A	3.124A	1.651A	2.656A
Suspend to RAM (typical)	108mA									
Soft Off (typical)	78mA									
RTC Power consumption (typical)	3.65µA									

2.3.3 Inrush Current

In the following table are shown the inrush current relative to the total current drawn by COMe-A98-CT6 module on VCC_12V and VCC_5V_SBY power rails, using an ATX Power Supply CORSAIR mod. VS560.

Inrush current measurements are made using a Digital Oscilloscope Keysight DSO-X 2022A. Please be aware that the maximum input current depends directly on the voltage rise time of the PSU used

These inrush currents have been measured using the same setup described in the previous paragraph.

Status	SoC				
	RX-421BD	RX-418GD	RX-216GD	RX-416GD	GX-217GI
VCC_12V Peak Current at Power On (AT Mode)	2.300 A	2.175 A	1.300 A	1.200 A	1.275 A
VCC_5V_SBY Peak Current at Power On (ATX Mode)	0.869 A	0.881 A	0.450 A	0.481 A	0.519 A

2.4 Mechanical Specifications

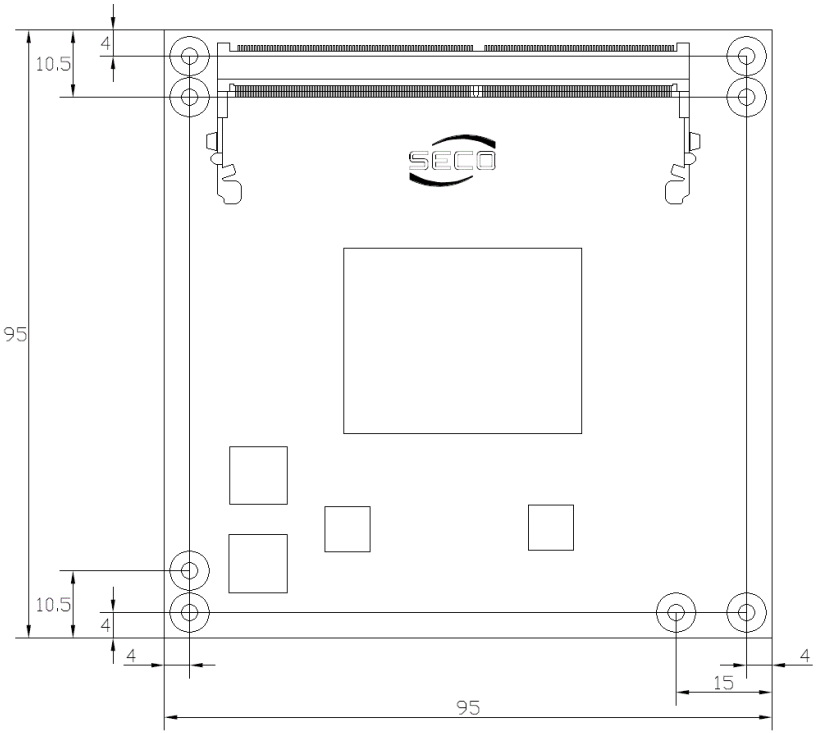
The COMe-A98-CT6 is a COM Express board, Compact form Factor type; therefore its dimensions are 95 mm x 95 mm (3.74” x 3.74”).

Printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector’s height is chosen, in designing a custom carrier board please remember that the SO-DIMM connector placed on the bottom side of COMe-A98-CT6 will have a maximum height of 4mm.

This value must be kept in high consideration when choosing the carrier board plugs’ height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.



2.5 Block Diagram R-Series SoCs

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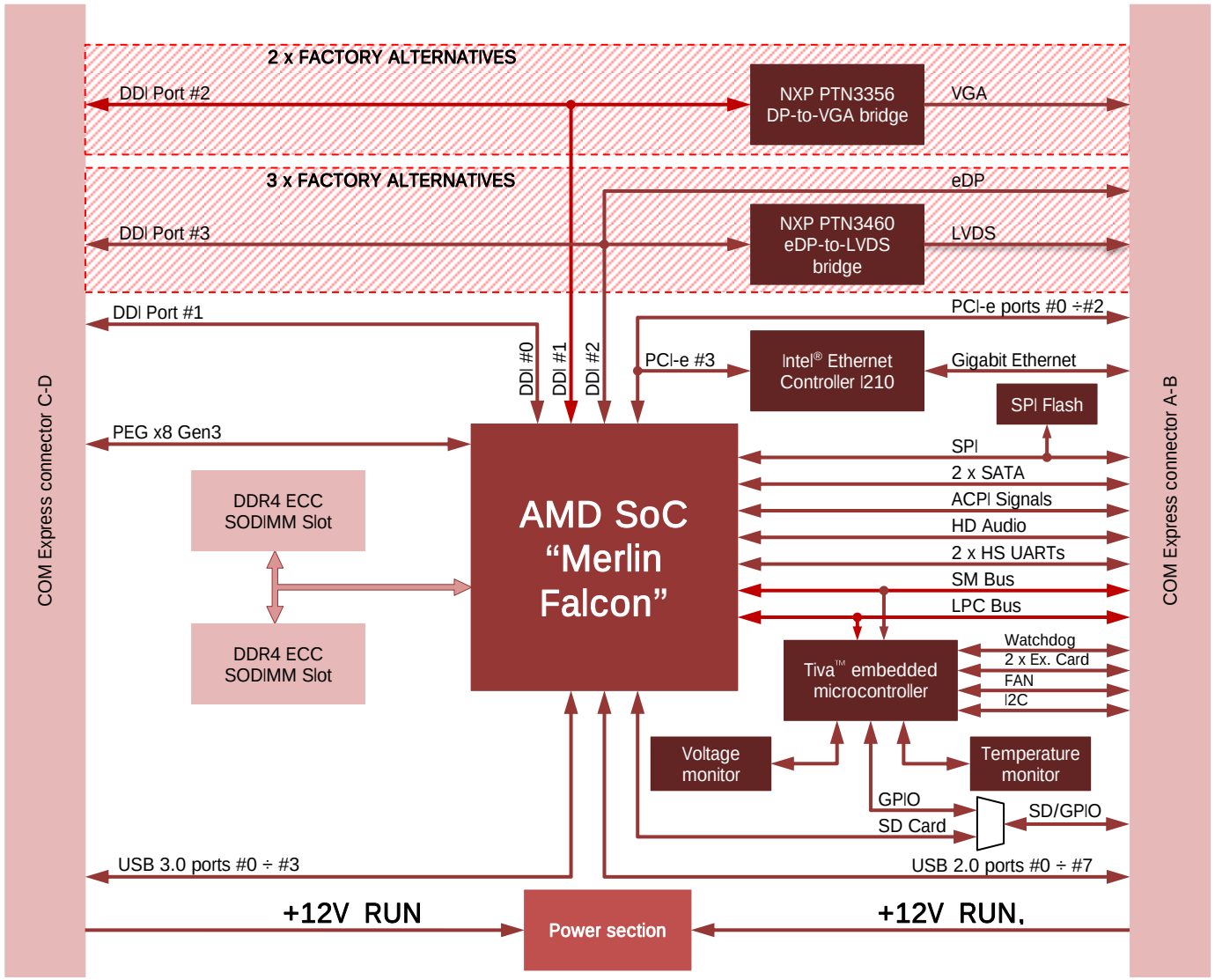
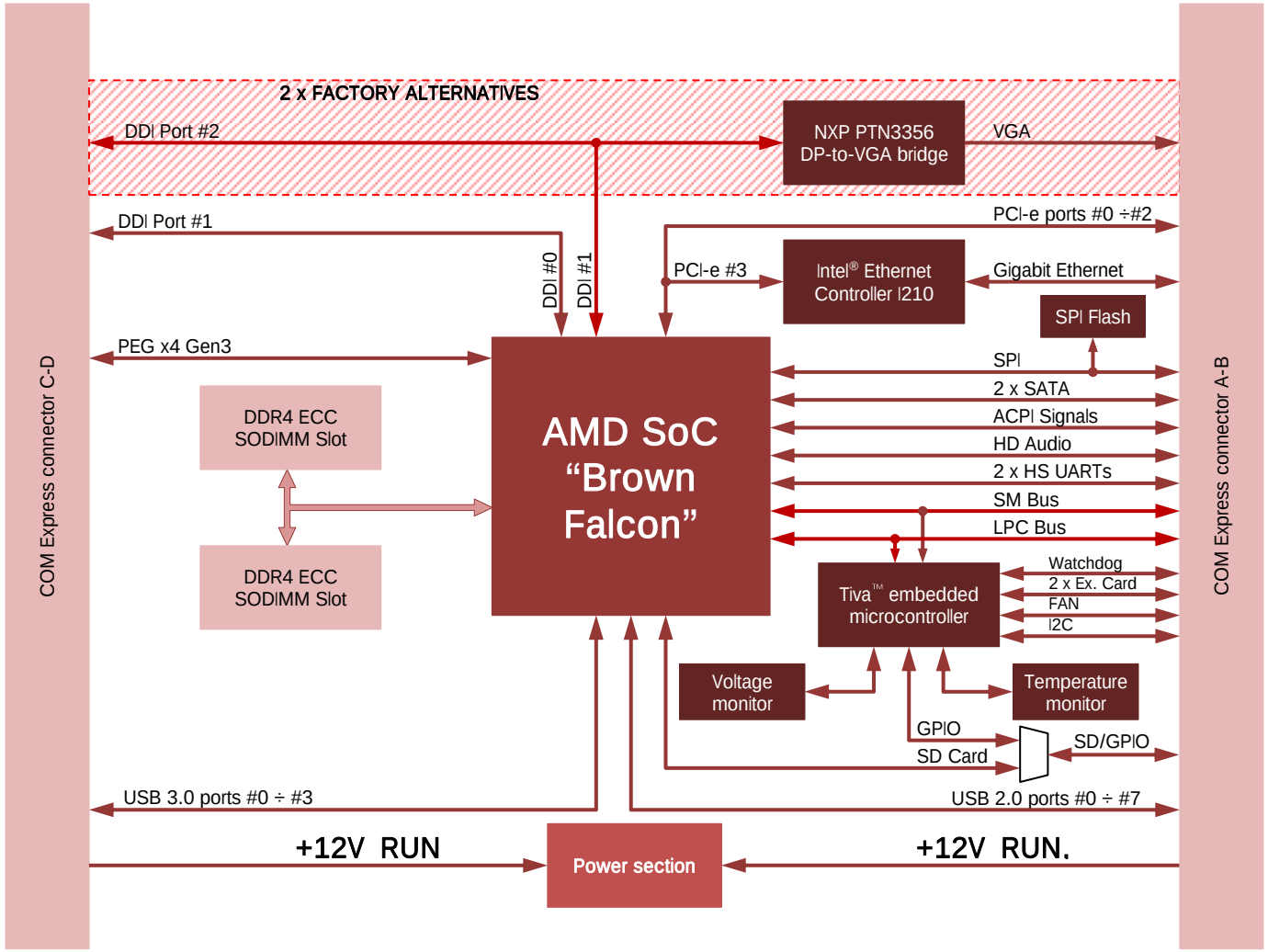
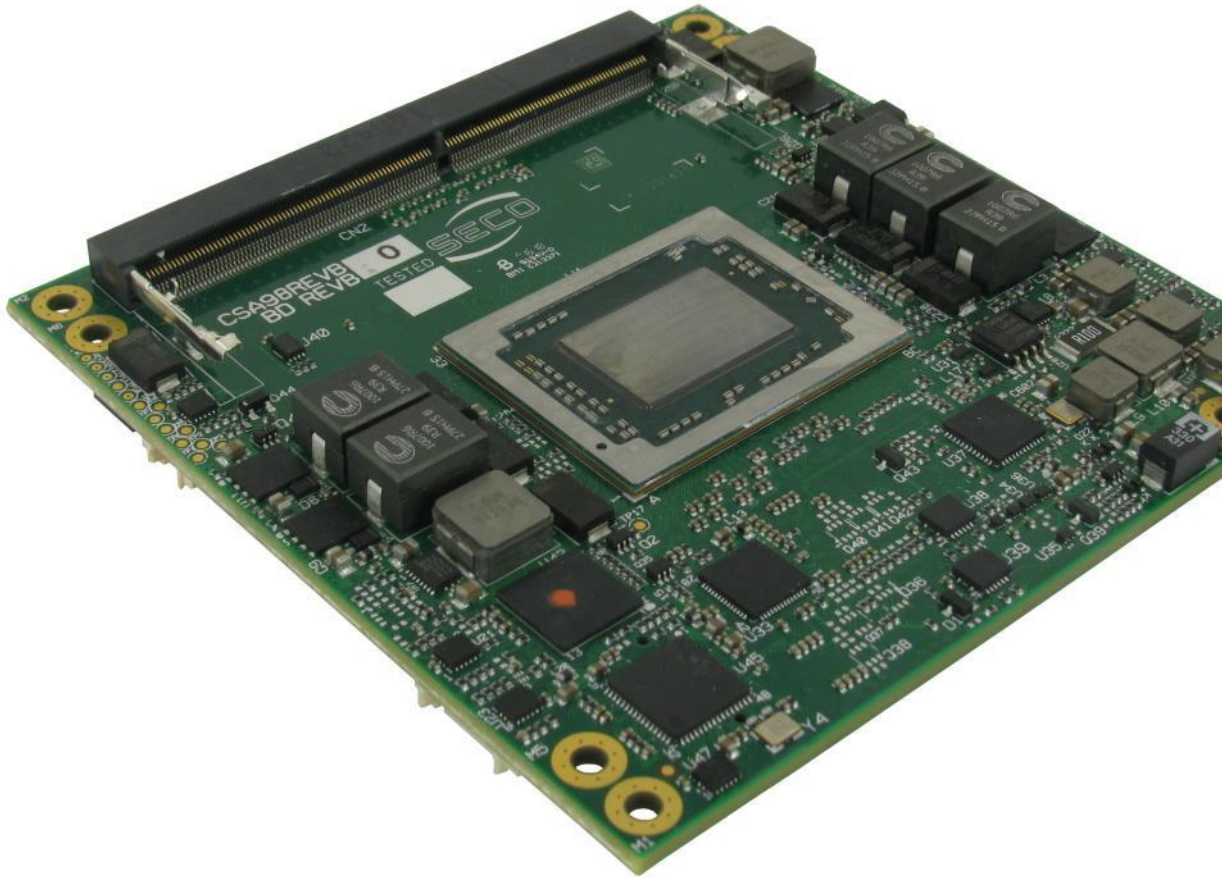


2.6 Block Diagram G-Series SoC-I



Chapter 3.
CONNECTORS

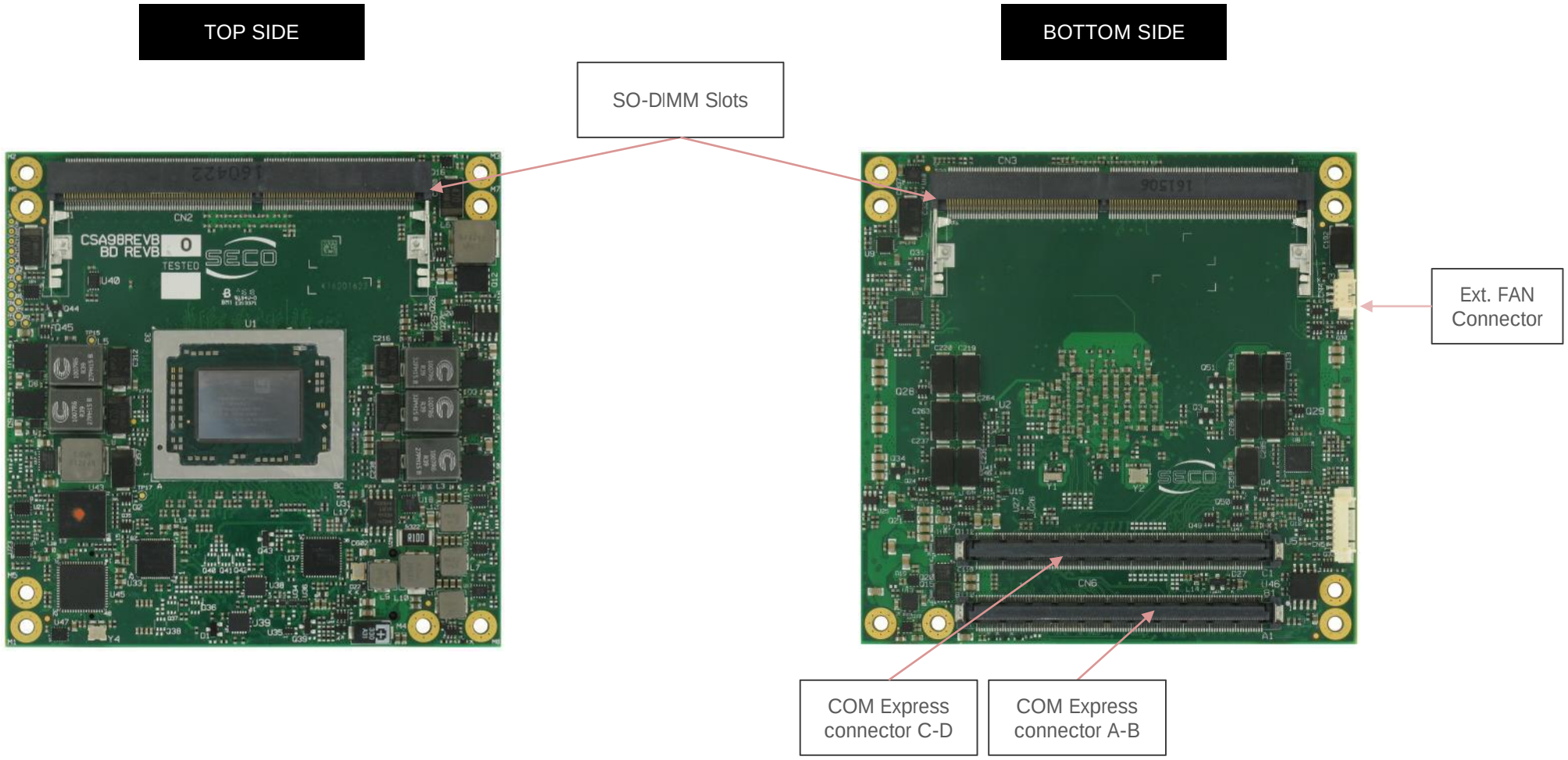
- Introduction
- Connectors description



3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.



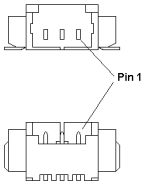
3.2 Connectors description

3.2.1 FAN Connector

FAN Connector – CN4	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of COMe-A98-CT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12V_{DC} FAN.

FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0371 or equivalent, with pinout shown in the table on the left.



Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_RUN derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_RUN electrical level signal with 10kΩ pull-up resistor.

3.2.2 SO-DIMM DDR4 Slots

CPUs used on the COMe-A98-CT6 board provide support to 2133MHz DDR4 SO-DIMM memory modules. Both ECC and non-ECC modules are supported.

For use of this memories, on board there are two SO-DIMM DDR4 slots.

The socket placed on top side (CN2) is type LOTES p/n ADDR0208-P003A or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications.

The socket placed on bottom side (CN3) is type LOTES p/n ADDR0205-P003A or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support to dual channel memories.

3.2.3 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-A98-CT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

COM Express® Connector AB - CN6							
		ROW A			ROW B		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	A1	B1	GND	PWR	
GBE	I/O	GBE0_MDI3-	A2	B2	GBE0_ACT#	O	GBE
GBE	I/O	GBE0_MDI3+	A3	B3	LPC_FRAME#	O	LPC
GBE	O	GBE0_LINK100#	A4	B4	LPC_AD0	I/O	LPC
GBE	O	GBE0_LINK1000#	A5	B5	LPC_AD1	I/O	LPC
GBE	I/O	GBE0_MDI2-	A6	B6	LPC_AD2	I/O	LPC
GBE	I/O	GBE0_MDI2+	A7	B7	LPC_AD3	I/O	LPC
GBE	O	GBE0_LINK#	A8	B8	LPC_DRQ0#	I	LPC
GBE	I/O	GBE0_MDI1-	A9	B9	N.C.	N.A.	
GBE	I/O	GBE0_MDI1+	A10	B10	LPC_CLK	O	LPC
	PWR	GND	A11	B11	GND	PWR	
GBE	I/O	GBE0_MDI0-	A12	B12	PWRBTN#	I	PWR_MGMT
GBE	I/O	GBE0_MDI0+	A13	B13	SMB_CK	I/O	SMBUS
	N.A.	N.C.	A14	B14	SMB_DAT	I/O	SMBUS
PWR_MGMT	O	SUS_S3#	A15	B15	SMB_ALERT#	I	SMBUS
SATA	O	SATA0_TX+	A16	B16	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	A17	B17	SATA1_TX-	O	SATA
PWR_MGMT	O	SUS_S5#	A18	B18	SUS_STAT#	O	PWR_MGMT
SATA	I	SATA0_RX+	A19	B19	SATA1_RX+	I	SATA
SATA	I	SATA0_RX-	A20	B20	SATA1_RX-	I	SATA

	PWR	GND	A21	B21	GND	PWR	
	N.A.	N.C.	A22	B22	N.C.	N.A.	
	N.A.	N.C.	A23	B23	N.C.	N.A.	
PWR_MGMT	O	SUS_S5#	A24	B24	PWR_OK	I	PWR_MGMT
	N.A.	N.C.	A25	B25	N.C.	N.A.	
	N.A.	N.C.	A26	B26	N.C.	N.A.	
PWR_MGMT	I	BATLOW#	A27	B27	WDT	O	MISC
SATA	O	SATA_ACT#	A28	B28	N.C.	N.A.	
AUDIO	O	HDA_SYNC	A29	B29	HDA_SDIN1	I/O	AUDIO
AUDIO	O	HDA_RST#	A30	B30	HDA_SDIN0	I/O	AUDIO
	PWR	GND	A31	B31	GND	PWR	
AUDIO	I/O	HDA_BITCLK	A32	B32	SPKR	O	MISC
AUDIO	O	HDA_SDOUT	A33	B33	I2C_CK	I/O	I2C
SPI	I	BIOS_DIS0#	A34	B34	I2C_DAT	I/O	I2C
MISC	O	THRMTRIP#	A35	B35	THRM#	I	MISC
USB	I/O	USB6-	A36	B36	USB7-	I/O	USB
USB	I/O	USB6+	A37	B37	USB7+	I/O	USB
USB	I	USB_6_7_OC#	A38	B38	USB_4_5_OC#	I	USB
USB	I/O	USB4-	A39	B39	USB5-	I/O	USB
USB	I/O	USB4+	A40	B40	USB5+	I/O	USB
	PWR	GND	A41	B41	GND	PWR	
USB	I/O	USB2-	A42	B42	USB3-	I/O	USB
USB	I/O	USB2+	A43	B43	USB3+	I/O	USB
USB	I	USB_2_3_OC#	A44	B44	USB_0_1_OC#	I	USB
USB	I/O	USB0-	A45	B45	USB1-	I/O	USB
USB	I/O	USB0+	A46	B46	USB1+	I/O	USB
	PWR	VCC_RTC	A47	B47	EXCD1_PERST#	O	EXCD
EXCD	O	EXCD0_PERST#	A48	B48	EXCD1_CPPE#	I	EXCD
EXCD	I	EXCD0_CPPE#	A49	B49	SYS_RESET#	I	PWR_MGMT
LPC	I/O	LPC_SERIRQ	A50	B50	CB_RESET#	O	PWR_MGMT

	PWR	GND	A51	B51	GND	PWR	
	N.A.	N.C.	A52	B52	N.C.	N.A.	
	N.A.	N.C.	A53	B53	N.C.	N.A.	
GPIO	I	GPI0	A54	B54	GPO1	O	GPIO
	N.A.	N.C.	A55	B55	N.C.	N.A.	
	N.A.	N.C.	A56	B56	N.C.	N.A.	
	PWR	GND	A57	B57	GPO2	O	GPIO
	N.A.	N.C.	A58	B58	N.C.	N.A.	
	N.A.	N.C.	A59	B59	N.C.	N.A.	
	PWR	GND	A60	B60	GND	PWR	
PCIE	O	PCIE_TX2+	A61	B61	PCIE_RX2+	I	PCIE
PCIE	O	PCIE_TX2-	A62	B62	PCIE_RX2-	I	PCIE
GPIO	I	GPI1	A63	B63	GPO3	O	GPIO
PCIE	O	PCIE_TX1+	A64	B64	PCIE_RX1+	I	PCIE
PCIE	O	PCIE_TX1-	A65	B65	PCIE_RX1-	I	PCIE
	PWR	GND	A66	B66	WAKE0#	I	PWR_MGMT
GPIO	I	GPI2	A67	B67	WAKE1#	I	PWR_MGMT
PCIE	O	PCIE_TX0+	A68	B68	PCIE_RX0+	I	PCIE
PCIE	O	PCIE_TX0-	A69	B69	PCIE_RX0-	I	PCIE
	PWR	GND	A70	B70	GND	PWR	
eDP/LVDS	O	eDP_TX2+ / LVDS_A0+	A71	B71	LVDS_B0+	O	LVDS
eDP/LVDS	O	eDP_TX2- / LVDS_A0-	A72	B72	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP_TX1+ / LVDS_A1+	A73	B73	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP_TX1- / LVDS_A1-	A74	B74	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP_TX0+ / LVDS_A2+	A75	B75	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP_TX0- / LVDS_A2-	A76	B76	LVDS_B2-	O	LVDS
eDP/LVDS	O	eDP_VDD_EN / LVDS_VDD_EN	A77	B77	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3+	A78	B78	LVDS_B3-	O	LVDS
LVDS	O	LVDS_A3-	A79	B79	eDP_BKLT_EN / LVDS_BKLT_EN	O	eDP/LVDS
	PWR	GND	A80	B80	GND	PWR	

eDP/LVDS	O	eDP_TX3+ / LVDS_A_CK+	A81	B81	LVDS_B_CK+	O	LVDS
eDP/LVDS	O	eDP_TX3- / LVDS_A_CK-	A82	B82	LVDS_B_CK-	O	LVDS
eDP/LVDS	I/O	eDP_AUX+ / LVDS_I2C_CK	A83	B83	eDP_BKLT_CTRL/LVDS_BKLT_CTRL	O	eDP/LVDS
eDP/LVDS	I/O	eDP_AUX- / LVDS_I2C_DAT	A84	B84	VCC_5V_SBY	PWR	
GPIO	I	GPI3	A85	B85	VCC_5V_SBY	PWR	
	N.A.	RSVD	A86	B86	VCC_5V_SBY	PWR	
eDP	I	eDP_HPD	A87	B87	VCC_5V_SBY	PWR	
PCIE	O	PCIE_CK_REF+	A88	B88	BIOS_DIS1#	I	SPI
PCIE	O	PCIE_CK_REF-	A89	B89	VGA_RED	O	VGA
	PWR	GND	A90	B90	GND	PWR	
SPI	O	SPI_POWER	A91	B91	VGA_GRN	O	VGA
SPI	I	SPI_MISO	A92	B92	VGA_BLU	O	VGA
GPIO	O	GPO0	A93	B93	VGA_HSYNC	O	VGA
SPI	O	SPI_CLK	A94	B94	VGA_VSYNC	O	VGA
SPI	O	SPI_MOSI	A95	B95	VGA_I2C_CK	I/O	VGA
MISC	I	TPM_PP	A96	B96	VGA_I2C_DAT	I/O	VGA
TYPE	N.A.	Type10#: N.C.	A97	B97	SPI_CS#	O	SPI
SERIAL	O	SER0_TX	A98	B98	RSVD	N.A.	
SERIAL	I	SER0_RX	A99	B99	RSVD	N.A.	
	PWR	GND	A100	B100	GND	PWR	
SERIAL	O	SER1_TX	A101	B101	FAN_PWMOUT	O	MISC
SERIAL	I	SER1_RX	A102	B102	FAN_TACHIN	I	MISC
PWR_MGMT	I	LID#	A103	B103	SLEEP#	I	PWR_MGMT
	PWR	VCC_12V	A104	B104	VCC_12V	PWR	
	PWR	VCC_12V	A105	B105	VCC_12V	PWR	
	PWR	VCC_12V	A106	B106	VCC_12V	PWR	
	PWR	VCC_12V	A107	B107	VCC_12V	PWR	
	PWR	VCC_12V	A108	B108	VCC_12V	PWR	
	PWR	VCC_12V	A109	B109	VCC_12V	PWR	
	PWR	GND	A110	B110	GND	PWR	

COM Express® Connector CD – CN6							
		ROW C			ROW D		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	C1	D1	GND	PWR	
	PWR	GND	C2	D2	GND	PWR	
USB	I	USB_SSRX0-	C3	D3	USB_SSTX0-	O	USB
USB	I	USB_SSRX0+	C4	D4	USB_SSTX0+	O	USB
	PWR	GND	C5	D5	GND	PWR	
USB	I	USB_SSRX1-	C6	D6	USB_SSTX1-	O	USB
USB	I	USB_SSRX1+	C7	D7	USB_SSTX1+	O	USB
	PWR	GND	C8	D8	GND	PWR	
USB	I	USB_SSRX2-	C9	D9	USB_SSTX2-	O	USB
USB	I	USB_SSRX2+	C10	D10	USB_SSTX2+	O	USB
	PWR	GND	C11	D11	GND	PWR	
USB	I	USB_SSRX3-	C12	D12	USB_SSTX3-	O	USB
USB	I	USB_SSRX3+	C13	D13	USB_SSTX3+	O	USB
	PWR	GND	C14	D14	GND	PWR	
	N.A.	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	I/O	DDI
	N.A.	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	I/O	DDI
	N.A.	RSVD	C17	D17	RSVD	N.A.	
	N.A.	RSVD	C18	D18	RSVD	N.A.	
	N.A.	N.C.	C19	D19	N.C.	N.A.	
	N.A.	N.C.	C20	D20	N.C.	N.A.	
	PWR	GND	C21	D21	GND	PWR	
	N.A.	N.C.	C22	D22	N.C.	N.A.	
	N.A.	N.C.	C23	D23	N.C.	N.A.	
DDI	I	DDI1_HPD	C24	D24	RSVD	N.A.	
	N.A.	N.C.	C25	D25	RSVD	N.A.	
	N.A.	N.C.	C26	D26	DDI1_PAIR0+	O	DDI

	N.A.	RSVD	C27	D27	DDI1_PAIR0-	O	DDI
	N.A.	RSVD	C28	D28	RSVD	N.A.	
	N.A.	N.C.	C29	D29	DDI1_PAIR1+	O	DDI
	N.A.	N.C.	C30	D30	DDI1_PAIR1-	O	DDI
	PWR	GND	C31	D31	GND	PWR	
DDI	I/O	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	O	DDI
DDI	I/O	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	O	DDI
DDI	I	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	I	DDI
	N.A.	RSVD	C35	D35	RSVD	N.A.	
DDI	I/O	DDI3_CTRLCLK_AUX+	C36	D36	DDI1_PAIR3+	O	DDI
DDI	I/O	DDI3_CTRLDATA_AUX-	C37	D37	DDI1_PAIR3-	O	DDI
DDI	I	DDI3_DDC_AUX_SEL	C38	D38	RSVD	N.A.	
DDI	O	DDI3_PAIR0+	C39	D39	DDI2_PAIR0+	O	DDI
DDI	O	DDI3_PAIR0-	C40	D40	DDI2_PAIR0-	O	DDI
	PWR	GND	C41	D41	GND	PWR	
DDI	O	DDI3_PAIR1+	C42	D42	DDI2_PAIR1+	O	DDI
DDI	O	DDI3_PAIR1-	C43	D43	DDI2_PAIR1-	O	DDI
DDI	I	DDI3_HPD	C44	D44	DDI2_HPD	I	DDI
	N.A.	RSVD	C45	D45	RSVD	N.A.	
DDI	O	DDI3_PAIR2+	C46	D46	DDI2_PAIR2+	O	DDI
DDI	O	DDI3_PAIR2-	C47	D47	DDI2_PAIR2-	O	DDI
	N.A.	RSVD	C48	D48	RSVD	N.A.	
DDI	O	DDI3_PAIR3+	C49	D49	DDI2_PAIR3+	O	DDI
DDI	O	DDI3_PAIR3-	C50	D50	DDI2_PAIR3-	O	DDI
	PWR	GND	C51	D51	GND	PWR	
PEG	I	PEG_RX0+	C52	D52	PEG_TX0+	O	PEG
PEG	I	PEG_RX0-	C53	D53	PEG_TX0-	O	PEG
TYPE	N.A.	TYPE0#: N.C.	C54	D54	N.C.	N.A.	
PEG	I	PEG_RX1+	C55	D55	PEG_TX1+	O	PEG
PEG	I	PEG_RX1-	C56	D56	PEG_TX1-	O	PEG

TYPE	N.A.	TYPE1#: N.C.	C57	D57	TYPE2#: GND	N.A.	TYPE
PEG	I	PEG_RX2+	C58	D58	PEG_TX2+	O	PEG
PEG	I	PEG_RX2-	C59	D59	PEG_TX2-	O	PEG
	PWR	GND	C60	D60	GND	PWR	
PEG	I	PEG_RX3+	C61	D61	PEG_TX3+	O	PEG
PEG	I	PEG_RX3-	C62	D62	PEG_TX3-	O	PEG
	N.A.	RSVD	C63	D63	RSVD	N.A.	
	N.A.	RSVD	C64	D64	RSVD	N.A.	
PEG	I	PEG_RX4+	C65	D65	PEG_TX4+	O	PEG
PEG	I	PEG_RX4-	C66	D66	PEG_TX4-	O	PEG
	N.A.	RSVD	C67	D67	GND	PWR	
PEG	I	PEG_RX5+	C68	D68	PEG_TX5+	O	PEG
PEG	I	PEG_RX5-	C69	D69	PEG_TX5-	O	PEG
	PWR	GND	C70	D70	GND	PWR	
PEG	I	PEG_RX6+	C71	D71	PEG_TX6+	O	PEG
PEG	I	PEG_RX6-	C72	D72	PEG_TX6-	O	PEG
	PWR	GND	C73	D73	GND	PWR	
PEG	I	PEG_RX7+	C74	D74	PEG_TX7+	O	PEG
PEG	I	PEG_RX7-	C75	D75	PEG_TX7-	O	PEG
	PWR	GND	C76	D76	GND	PWR	
	N.A.	RSVD	C77	D77	RSVD	N.A.	
	N.A.	N.C.	C78	D78	N.C.	N.A.	
	N.A.	N.C.	C79	D79	N.C.	N.A.	
	PWR	GND	C80	D80	GND	PWR	
	N.A.	N.C.	C81	D81	N.C.	N.A.	
	N.A.	N.C.	C82	D82	N.C.	N.A.	
	N.A.	RSVD	C83	D83	RSVD	N.A.	
	PWR	GND	C84	D84	GND	PWR	
	N.A.	N.C.	C85	D85	N.C.	N.A.	
	N.A.	N.C.	C86	D86	N.C.	N.A.	

PWR	GND	C87	D87	GND	PWR
N.A.	N.C.	C88	D88	N.C.	N.A.
N.A.	N.C.	C89	D89	N.C.	N.A.
PWR	GND	C90	D90	GND	PWR
N.A.	N.C.	C91	D91	N.C.	N.A.
N.A.	N.C.	C92	D92	N.C.	N.A.
PWR	GND	C93	D93	GND	PWR
N.A.	N.C.	C94	D94	N.C.	N.A.
N.A.	N.C.	C95	D95	N.C.	N.A.
PWR	GND	C96	D96	GND	PWR
N.A.	RSVD	C97	D97	RSVD	N.A.
N.A.	N.C.	C98	D98	N.C.	N.A.
N.A.	N.C.	C99	D99	N.C.	N.A.
PWR	GND	C100	D100	GND	PWR
N.A.	N.C.	C101	D101	N.C.	N.A.
N.A.	N.C.	C102	D102	N.C.	N.A.
PWR	GND	C103	D103	GND	PWR
PWR	VCC_12V	C104	D104	VCC_12V	PWR
PWR	VCC_12V	C105	D105	VCC_12V	PWR
PWR	VCC_12V	C106	D106	VCC_12V	PWR
PWR	VCC_12V	C107	D107	VCC_12V	PWR
PWR	VCC_12V	C108	D108	VCC_12V	PWR
PWR	VCC_12V	C109	D109	VCC_12V	PWR
PWR	GND	C110	D110	GND	PWR

3.2.3.1 Audio interface signals

The COMe-A98-CT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard. Up to 2 HD audio codecs on the carrier board can be supported.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_RUN.

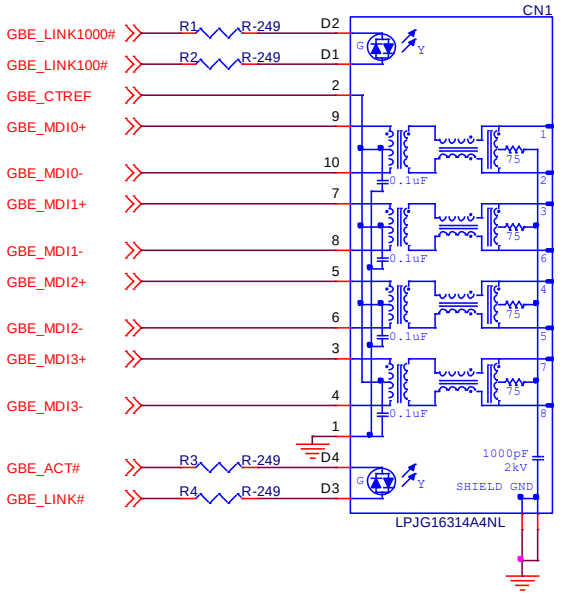
HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

HDA_SDIN[0..1]: HD Audio Serial Data In signal. Inputs to the module from the Codec(s) placed on the Carrier board, electrical level +3.3V_RUN.

The first four signals have to be connected to all the HD Audio codecs present on the carrier board. For each Codec, only one HDA_SDIN signal must be used. Please refer to the chosen Codecs' Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.3.2 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on COMe-A98-CT6 module, using an Intel® I210/I211 Gigabit Ethernet controller, which is interfaced to the SoC through the General Purpose PCI-express port #3.



Here following the signals involved in Gigabit Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_LAN.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_LAN.

+3.3V_LAN is derived from +3.3V_ALW power rail through a 120Ω ferrite bead.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic provided in the previous page as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector.

Intel® I210/I211 Gigabit Ethernet controllers, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.3.3 S-ATA signals

The AMD 3rd Generation R-Series SoCs offer two S-ATA Gen3 interfaces, which are all carried out on COM Express® connector AB.

All SATA ports support 1.5 Gbps, 3.0 Gbps and 6.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. +3.3V_RUN Active Low output signal with 10kΩ pull-up resistor.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors.

3.2.3.4 PCI Express interface signals

COMe-A98-CT6 can offer externally three PCI Express lane, which are managed directly by the AMD 3rd Generation R-Series SoCs.

These interfaces can be managed only as single PCI-e x1 lanes.

PCI express Gen3 (8 GT/s) is supported an all PCI-e ports.

Here following the signals involved in PCI express management.

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #0.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #0.

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #1.

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #1.

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #2.

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair. Connected to the AMD SoC's General Purpose PCI-e port #2.

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are seven different PCI express lanes and one PEG. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer should be used to replicate the reference clock to all the devices.

PCI Express ports #0 and #1 can be grouped to work as a single PCI-e x2 port. This can be done via BIOS settings (please check par. 3.2.3.4).

3.2.3.5 PEG interface signals

In addition to the three PCI express lanes, described in the previous paragraph, the COMe-A98-CT6 module offer a PCI-Express x8 graphics interface (PEG), which can be used for connection of external graphics cards. Such an interface is directly managed by the AMD 3rd Generation R-Series SoCs.

PCI express Gen3 is supported.

Here following the signals involved in PEG management.

PEG_TX[0..7]+/PEG_TX[0..7]-: PCI Express Graphics lane #0 ÷ #7, Transmitting Output Differential pairs.

PEG_RX[0..7]+/PEG_RX[0..7]-: PCI Express Graphics lane #0 ÷ #7, Receiving Output Differential pairs.

This PEG port can be configured to work as a single PCI-e x8 port or two PCI-e x4 ports (in that case, lanes #0÷#3 would be used for the first port, GFX#0, while lanes #4÷#7 would be used for the second port, GFX #1). This configuration can be done via BIOS settings (please check par. 3.2.3.4).

3.2.3.6 Express Card interface signals

According to Com Express® specifications, the COMe-A98-CT6 module offers the signals necessary for management of up to two Express Cards, managed by the module's embedded microcontroller.

The signals involved in Express Card management are the following.

EXCD0_CPPE#: PCI Express Capable Card slot #0 Request, +3.3V_RUN Active Low input signal with 10kΩ pull-up resistor.

EXCD0_PERST#: Express Card slot #0 reset, +3.3V_RUN Active Low output signal.

EXCD1_CPPE#: PCI Express Capable Card slot #1 Request, +3.3V_RUN Active Low input signal with 10kΩ pull-up resistor.

EXCD1_PERST#: Express Card slot #1 reset, +3.3V_RUN Active Low output signal.

3.2.3.7 USB interface signals

The AMD 3rd Generation R-Series SoCs embed one xHCI controller and one EHCI controller, which allow, globally, implementing four Superspeed ports (i.e. USB 3.0 compliant) and eight USB 1.x / 2.0 Host ports.

All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB0+/USB0-: Universal Serial Bus Port #0 bidirectional differential pair, managed by the xHCI controller.

USB1+/USB1-: Universal Serial Bus Port #1 bidirectional differential pair, managed by the xHCI controller.

USB2+/USB2-: Universal Serial Bus Port #2 bidirectional differential pair, managed by the xHCI controller.

USB3+/USB3-: Universal Serial Bus Port #3 bidirectional differential pair, managed by the xHCI controller.

USB4+/USB4-: Universal Serial Bus Port #4 bidirectional differential pair, managed by the EHCI controller.

USB5+/USB5-: Universal Serial Bus Port #5 bidirectional differential pair, managed by the EHCI controller.

USB6+/USB6-: Universal Serial Bus Port #6 bidirectional differential pair, managed by the EHCI controller.

USB7+/USB7-: Universal Serial Bus Port #7 bidirectional differential pair, managed by the EHCI controller.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by the xHCI controller.

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by the xHCI controller.

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair; it is managed by the xHCI controller.

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair; it is managed by the xHCI controller.

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair; it is managed by the xHCI controller.

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair; it is managed by the xHCI controller.

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair; it is managed by the xHCI controller.

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair; it is managed by the xHCI controller.

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-A98-CT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signa.l, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-A98-CT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-A98-CT6 module.

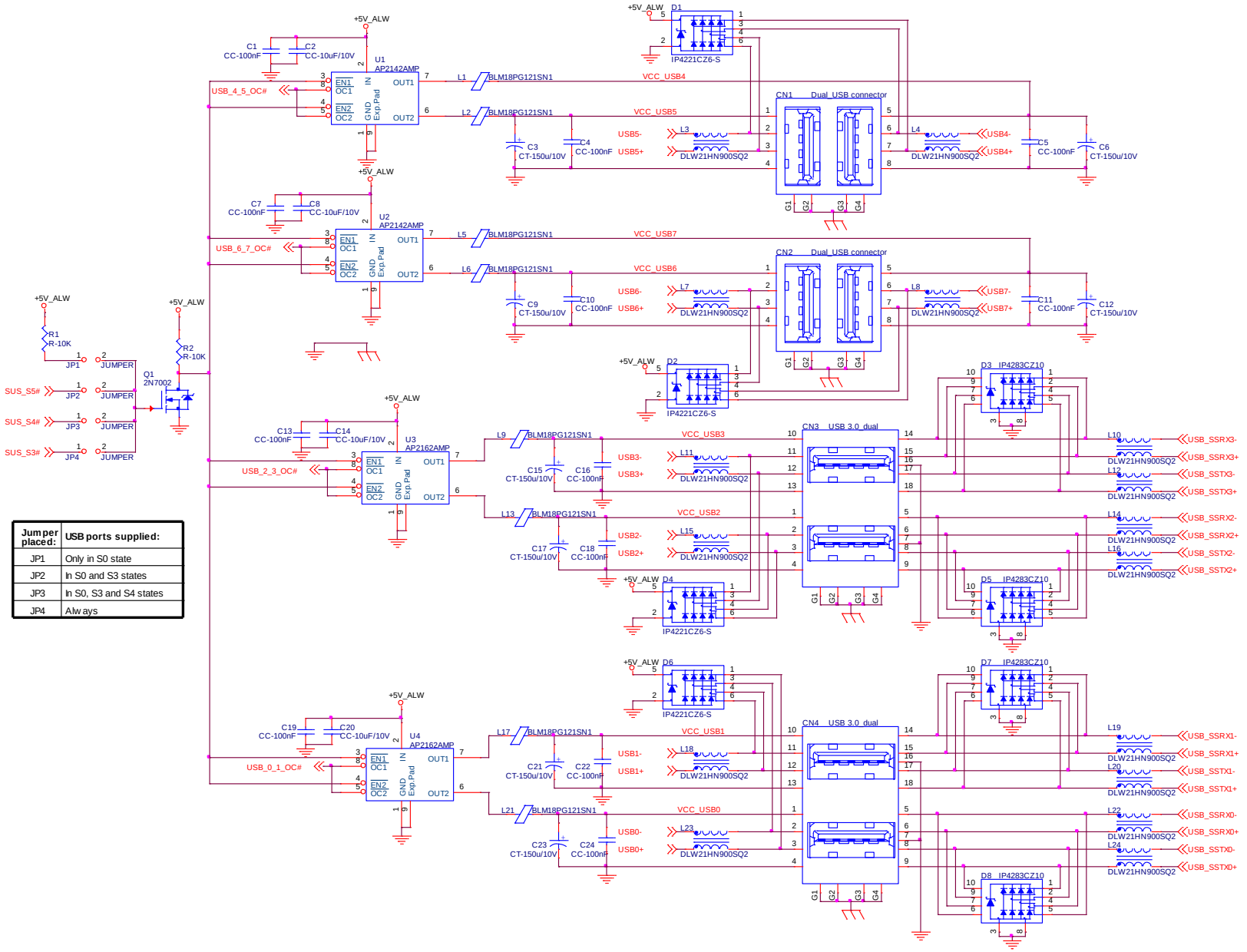
USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_ALW with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-A98-CT6 module.

100nF AC series decoupling capacitors are placed on each receiving line of USB Super speed differential pairs.

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and 3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	In S0, S3 and S4 states
JP4	Always

3.2.3.8 LVDS Flat Panel signals (R-Series SoCs only)

The AMD 3rd Generation R-Series SoCs offer three native Digital Display interfaces, which can support Display Port, DVI, or HDMI interfaces.

The LVDS interface, which is frequently used in many application fields, is not directly supported by these SoCs.

For this reason, as a factory option, COMe-A98-CT6 modules with R-Series SoCs can be equipped with an eDP to LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for AMD 3rd Generation R-Series SoCs, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins there can be the LVDS first channel **or** eDP interface (or none of them, in that case there will be DDI interface #3 on COM Express Connector CD).
>
> Furthermore, DDI interface #3 is not available with AMD 3rd Generation G-Series SoC-I ("Brown Falcon"), therefore not even LVDS nor eDP interfaces can be available with this SoC.
>
> When placing an order of COMe-A98-CT6 modules, please take care of specifying if it is necessary LVDS interface, eDP interface or DDI #3 interface.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: +3.3V_RUN electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: +3.3V_RUN electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +3.3V_RUN electrical level output.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_RUN with a 2k2Ω pull-up resistor.

3.2.3.9 Embedded Display Port (eDP) signals (R-Series SoCs only)

As described in the previous paragraph, the AMD 3rd Generation R-Series SoCs offer only Digital Display Interfaces.

As a factory option, one of these interfaces (DDI3) can be switched toward COM Express connector AB. When the board is not configured with the eDP-to-LVDS bridge, then the switched DDI interface supports eDP displays. Depending on the number of eDP lanes used (1, 2 or 4) it is possible to support the higher resolution displays.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0. AC coupled though 100nF ceramic capacitors on both lines.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1. AC coupled though 100nF ceramic capacitors on both lines.

eDP_TX2+/eDP_TX2-: eDP channel differential data pair #2. AC coupled though 100nF ceramic capacitors on both lines.

eDP_TX3+/eDP_TX3-: eDP channel differential data pair #3. AC coupled though 100nF ceramic capacitors on both lines.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel. AC coupled though 100nF ceramic capacitors on both lines.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_RUN electrical level input with 100KΩ pull-down resistor.

eDP_VDD_EN: +3.3V_RUN electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: +3.3V_RUN electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +3.3V_RUN electrical level output.

! Please remember that the eDP interface is not available with AMD 3rd Generation G-Series SoC-I ("Brown Falcon").

3.2.3.10 LPC interface signals

According to COM Express® specifications rel. 2.1, on the on COM Express connector AB there are 9 pins that are used for implementation of Low Pin Count (LPC) Bus interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_RUN electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_RUN electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_DRQ0#: LPC Serial DMA request, +3.3V_RUN electrical level input signals, active low. This signal is used to request DMA or bus master access.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_RUN electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_RUN electrical level. This signal is used only by peripherals requiring Interrupt support.

3.2.3.11 SPI interface signals

The AMD 3rd Generation R-Series SoCs offer also one dedicated controller for Serial Peripheral Interface (SPI), which can be used for connection of Serial Flash devices. Please be aware that this interface should be used exclusively to support platform firmware (BIOS).

Signals involved with SPI management are the following:

SPI_CS#: SPI Chip select, active low output signal, +3.3V_RUN voltage level.

SPI_MISO: SPI Master In Slave Out, Input to COM Express® module from SPI devices embedded on the Carrier Board. +3.3V_RUN voltage level.

SPI_MOSI: SPI Master Out Slave In, Output from COM Express® module to SPI devices embedded on the Carrier Board. +3.3V_RUN voltage level.

SPI_CLK: SPI Clock Output to carrier board's SPI embedded devices. +3.3V_RUN voltage level. Clock frequencies up to 66MHz are supported.

SPI_POWER: Power Supply Output for carrier board's SPI devices. +3.3V_RUN voltage level.

BIOS_DIS[0..1]#: BIOS Disable strap input, electrical level +3.3V_RUN with 10kΩ pull-up resistor. These two signals are inputs of the COM Express® Module, that on the carrier board can be left floating or pulled down in order to select which SPI Flash device has to be used for module's boot. Please refer to table 4.13 of COM Express® Module Base Specifications rel. 2.1 for the meaning of possible configurations of these two signals.

3.2.3.12 Analog VGA interface

The AMD 3rd Generation R-Series SoCs (and the G-Series SoC-I) don't offer an analog VGA interface, which however continues to be requested for legacy applications.

For this reason, as a factory option, it is possible to purchase COMe-A98-CT6 modules with a DP-to-VGA bridge (NXP PTN3356BS), which converts the Digital Display Interface #1 coming from the SoC. This makes available one analog display interface, which can be used for the connection of older VGA/CRT displays.

Signals dedicated to VGA interface are the following:

VGA_RED: Red Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_GRN: Green Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_BLU: Blue Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_HSYNC: Horizontal Synchronization output signal.

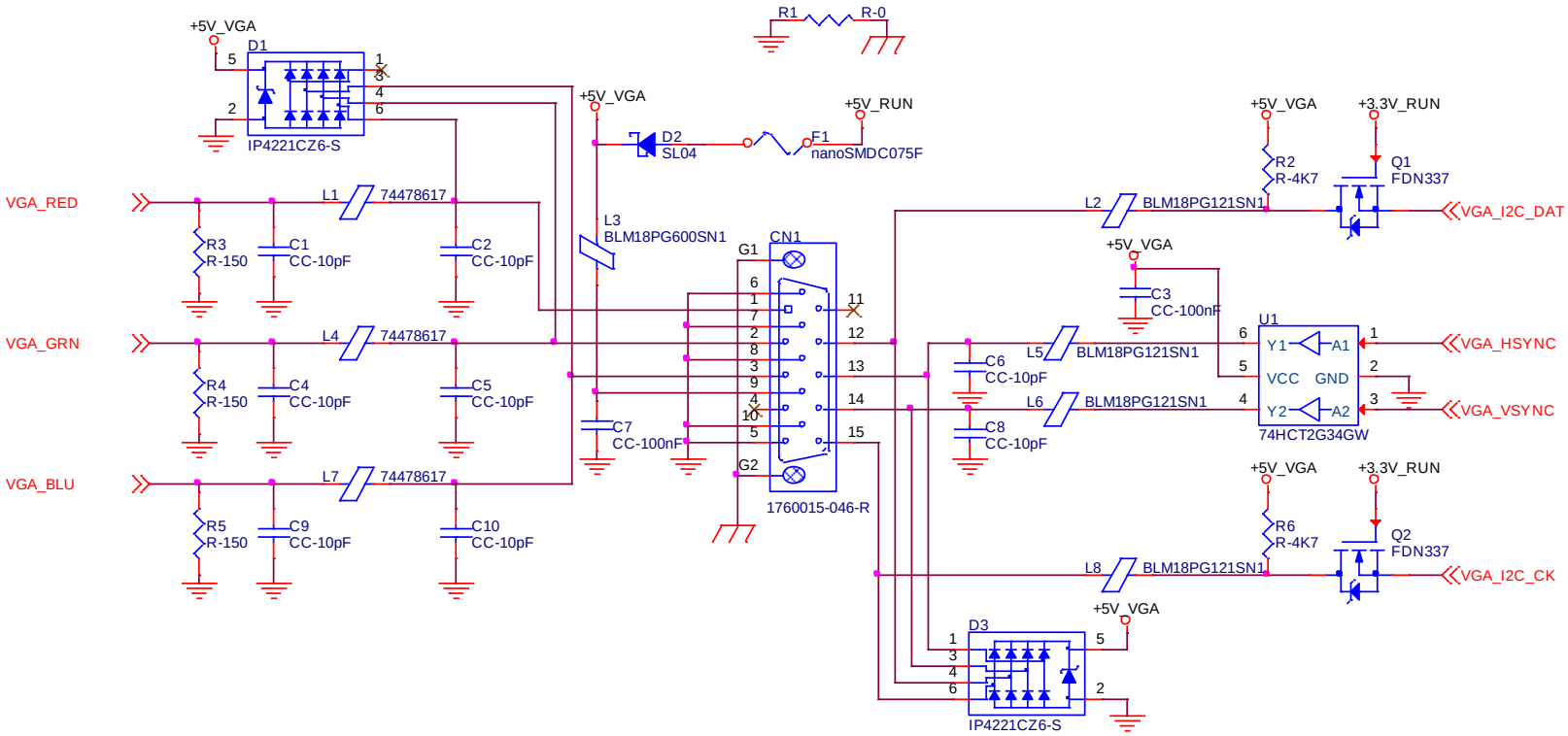
VGA_VSYNC: Vertical Synchronization output signal.

VGA_I2C_CK: DDC Clock line for VGA displays detection. Output signal, electrical level +3.3V_RUN with 2k2Ω pull-up resistor.

VGA_I2C_DAT: DDC Clock line for VGA displays detection. Bidirectional signal, electrical level +3.3V_RUN with 2k2Ω pull-up resistor.

> **!** Please remember that VGA interface is not native for AMD 3rd Generation R-Series SoCs / G-Series SoC-I, it is derived from an optional DP-to-VGA bridge. Depending on the factory option purchased, it is possible to have VGA interface con COM Express connector AB **or** DDI #2 on COM Express Connector CD.
>
> When placing an order of COMe-A98-CT6 modules, please take care of specifying if it is necessary VGA or DDI #1 interface.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection like in the following example schematics.


+5V_VGA
D1
IP4221CZ6-S
R1
R-0
D2
SL04
F1
nanoSMDC075F
+5V_RUN
VGA_RED
VGA_GRN
VGA_BLU
L1
L4
L7
74478617
R3
R-150
C1
CC-10pF
C2
CC-10pF
R4
R-150
C4
CC-10pF
C5
CC-10pF
R5
R-150
C9
CC-10pF
C10
CC-10pF
L3
BLM18PG600SN1
C7
CC-100nF
CN1
1760015-046-R
L2
L5
L6
L8
BLM18PG121SN1
R2
R-4K7
Q1
FDN337
VGA_I2C_DAT
+3.3V_RUN
C3
CC-100nF
C6
CC-10pF
C8
CC-10pF
U1
74HCT2G34GW
VGA_HSYNC
VGA_VSYNC
R6
R-4K7
Q2
FDN337
VGA_I2C_CK
D3
IP4221CZ6-S

3.2.3.13 Digital Display interfaces

The AMD Radeon™ 3rd Generation Graphics Core Next (GCN) GPU series, embedded inside the embedded 3rd Generation R-Series SoCs, offer three Digital Display Interfaces, which can support DP, eDP, DVI and/or HDMI interfaces. Using G-Series SoC-I, only two Digital Display interfaces are available (DDI#0 and DDI#1).

DDI #0 is always carried out to COM Express connector CD, while DDI ports #1 and #2 can be used to implement, on COM Express connector AB, the VGA interface, the LVDS interface or the eDP interface (see also paragraphs 3.2.3.8, 3.2.3.9 and 3.2.3.12).

The DDI ports can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

Digital Display Interfaces - Pin multiplexing					
		Multimode Display Port mode		TMDS (HDMI/DVI) mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
D26	DDI1_PAIR0+	DP1_LANE0+	DP1 Differential pair #0 non-inverting line	TMDS1_DATA2+	TMDS1 Differential pair #2 non-inverting line
D27	DDI1_PAIR0-	DP1_LANE0-	DP1 Differential pair #0 inverting line	TMDS1_DATA2-	TMDS1 Differential pair #2 inverting line
D29	DDI1_PAIR1+	DP1_LANE1+	DP1 Differential pair #1 non-inverting line	TMDS1_DATA1+	TMDS1 Differential pair #1 non-inverting line
D30	DDI1_PAIR1-	DP1_LANE1-	DP1 Differential pair #1 inverting line	TMDS1_DATA1-	TMDS1 Differential pair #1 inverting line
D32	DDI1_PAIR2+	DP1_LANE2+	DP1 Differential pair #2 non-inverting line	TMDS1_DATA0+	TMDS1 Differential pair #0 non-inverting line
D33	DDI1_PAIR2-	DP1_LANE2-	DP1 Differential pair #2 inverting line	TMDS1_DATA0-	TMDS1 Differential pair #0 inverting line
D36	DDI1_PAIR3+	DP1_LANE3+	DP1 Differential pair #3 non-inverting line	TMDS1_CLK+	TMDS1 Differential clock non-inverting line
D37	DDI1_PAIR3-	DP1_LANE3-	DP1 Differential pair #3 inverting line	TMDS1_CLK-	TMDS1 Differential clock inverting line
C24	DDI1_HPD	DP1_HPD	DP1 Hot Plug Detect signal	HDMI1_HPD	HDMI #1 Hot Plug Detect signal
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	DP1 Auxiliary channel non-inverting line	HDMI1_CTRLCLK	DDC Clock line for HDMI panel #1.
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	DP1 Auxiliary channel inverting line	HDMI1_CTRLDATA	DDC Data line for HDMI panel #1.
D34	DDI1_DDC_AUX_SEL	DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
D39	DDI2_PAIR0+	DP2_LANE0+	DP2 Differential pair #0 non-inverting line	TMDS2_DATA2+	TMDS2 Differential pair #2 non-inverting line

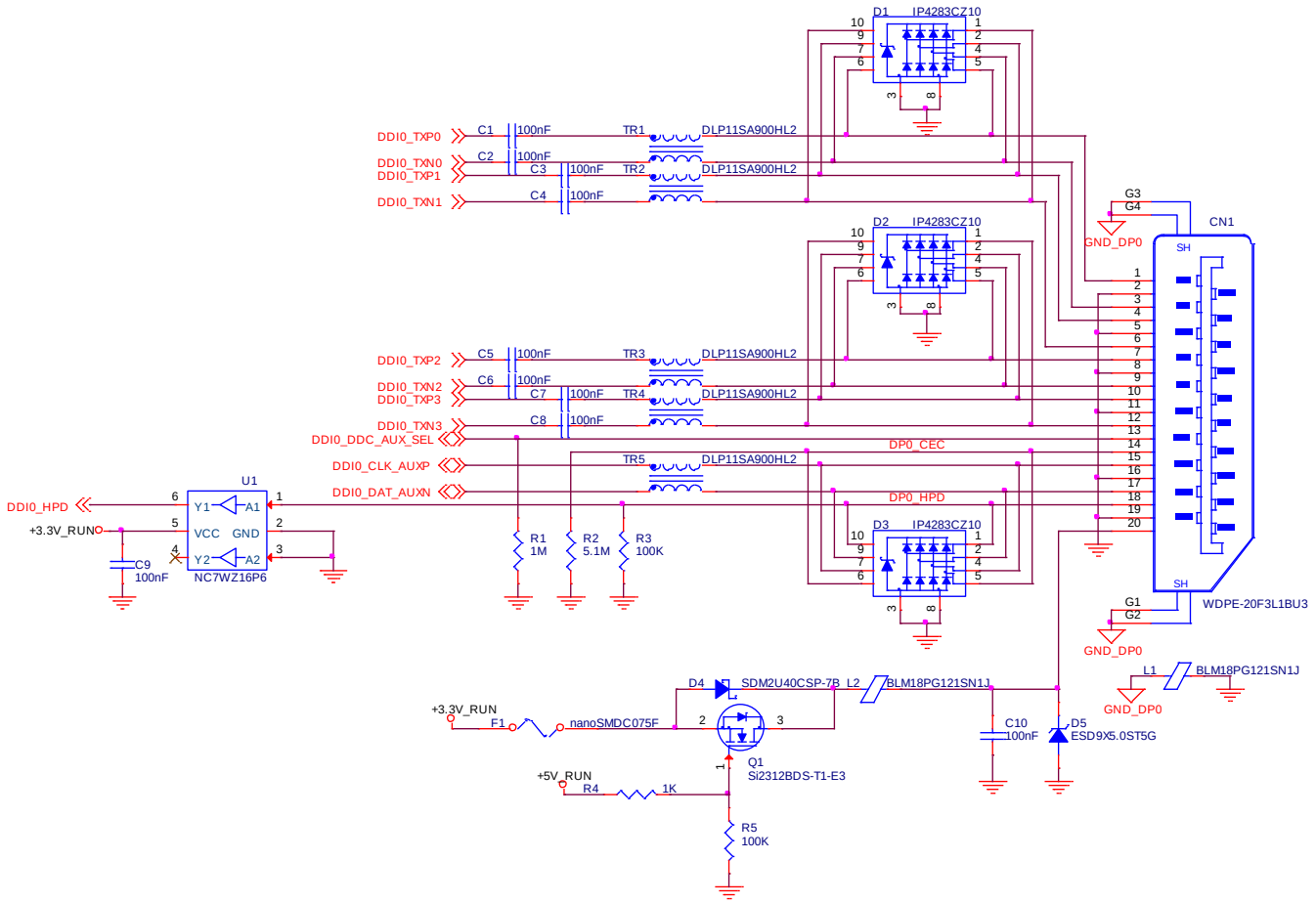
D40	DDI2_PAIR0-	DP2_LANE0-	DP2 Differential pair #0 inverting line	TMDS2_DATA2-	TMDS2 Differential pair #2 inverting line
D42	DDI2_PAIR1+	DP2_LANE1+	DP2 Differential pair #1 non-inverting line	TMDS2_DATA1+	TMDS2 Differential pair #1 non-inverting line
D43	DDI2_PAIR1-	DP2_LANE1-	DP2 Differential pair #1 inverting line	TMDS2_DATA1-	TMDS2 Differential pair #1 inverting line
D46	DDI2_PAIR2+	DP2_LANE2+	DP2 Differential pair #2 non-inverting line	TMDS2_DATA0+	TMDS2 Differential pair #0 non-inverting line
D47	DDI2_PAIR2-	DP2_LANE2-	DP2 Differential pair #2 inverting line	TMDS2_DATA0-	TMDS2 Differential pair #0 inverting line
D49	DDI2_PAIR3+	DP2_LANE3+	DP2 Differential pair #3 non-inverting line	TMDS2_CLK+	TMDS2 Differential clock non-inverting line
D50	DDI2_PAIR3-	DP2_LANE3-	DP2 Differential pair #3 inverting line	TMDS2_CLK-	TMDS2 Differential clock inverting line
D44	DDI2_HPD	DP2_HPD	DP2 Hot Plug Detect signal	HDMI2_HPD	HDMI #2 Hot Plug Detect signal
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	DP2 Auxiliary channel non-inverting line	HDMI2_CTRLCLK	DDC Clock line for HDMI panel #2..
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	DP2 Auxiliary channel inverting line	HDMI2_CTRLDATA	DDC Data line for HDMI panel #2.
C34	DDI2_DDC_AUX_SEL	DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			
C39	DDI3_PAIR0+	DP3_LANE0+	DP3 Differential pair #0 non-inverting line	TMDS3_DATA2+	TMDS3 Differential pair #2 non-inverting line
C40	DDI3_PAIR0-	DP3_LANE0-	DP3 Differential pair #0 inverting line	TMDS3_DATA2-	TMDS3 Differential pair #2 inverting line
C42	DDI3_PAIR1+	DP3_LANE1+	DP3 Differential pair #1 non-inverting line	TMDS3_DATA1+	TMDS3 Differential pair #1 non-inverting line
C43	DDI3_PAIR1-	DP3_LANE1-	DP3 Differential pair #1 inverting line	TMDS3_DATA1-	TMDS3 Differential pair #1 inverting line
C46	DDI3_PAIR2+	DP3_LANE2+	DP3 Differential pair #2 non-inverting line	TMDS3_DATA0+	TMDS3 Differential pair #0 non-inverting line
C47	DDI3_PAIR2-	DP3_LANE2-	DP3 Differential pair #2 inverting line	TMDS3_DATA0-	TMDS3 Differential pair #0 inverting line
C49	DDI3_PAIR3+	DP3_LANE3+	DP3 Differential pair #3 non-inverting line	TMDS3_CLK+	TMDS3 Differential clock non-inverting line
C50	DDI3_PAIR3-	DP3_LANE3-	DP3 Differential pair #3 inverting line	TMDS3_CLK-	TMDS3 Differential clock inverting line
C44	DDI3_HPD	DP3_HPD	DP3 Hot Plug Detect signal	HDMI3_HPD	HDMI #3 Hot Plug Detect signal
C36	DDI3_CTRLCLK_AUX+	DP3_AUX+	DP3 Auxiliary channel non-inverting line	HDMI3_CTRLCLK	DDC Clock line for HDMI panel #3.
C37	DDI3_CTRLDATA_AUX-	DP3_AUX-	DP3 Auxiliary channel inverting line	HDMI3_CTRLDATA	DDC Data line for HDMI panel #3.
C38	DDI3_DDC_AUX_SEL	DDI#3 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_RUN) for TMDS interface			

All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are active high inputs with 100KΩ pull-down resistors.

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

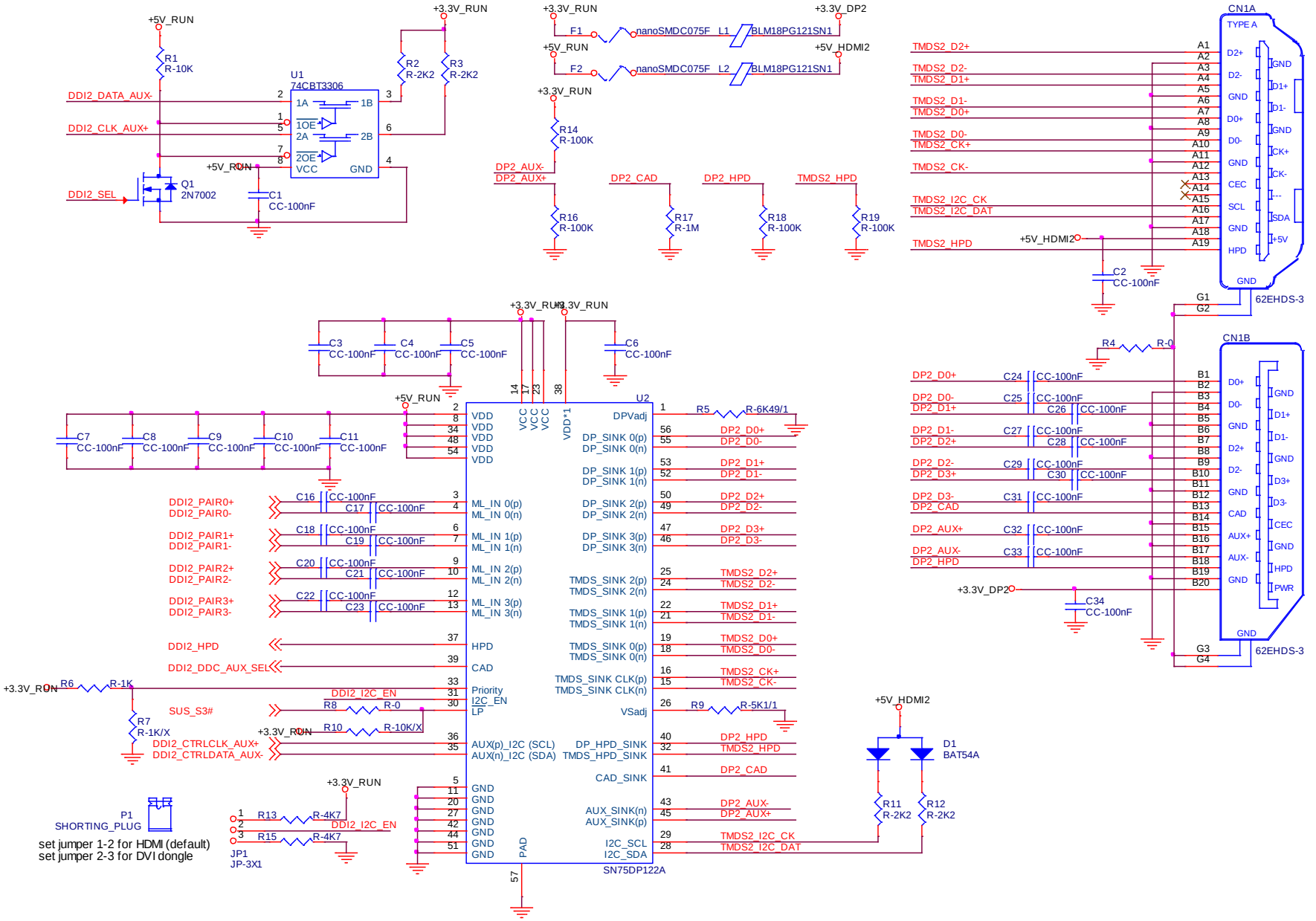
In the next page there is an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #0, but any DDI interface can be used.



The example schematics in the following page, instead, shows the implementation (using DDI interface #2, but any DDI can be used for this purpose) of a double connector DP++ and HDMI, managed using a DisplayPort 1:2 Switch with Integrated TMDS Translator, which provides to TMDS voltage level shifter for HDMI/DVI connection.

By implementing such a schematic, the module can configure itself automatically to work with external HDMI/DVI or multimode Display Port interfaces, depending on the cable connected. In case both an HDMI and a DP are connected, the HDMI interface will take priority automatically. This order can be changed by removing resistor R6 and mounting resistor R7.

The jumper JP1 is used to enable or disable switch's I2C internal registers, for use of TMDS interface, respectively, for HDMI or DVI displays.


+5V_RUN
+3.3V_RUN
+3.3V_DP2
+5V_HDMI2
U1
74CBT3306
U2
SN75DP122A
CN1A
TYPE A
CN1B
62EHDS-3
DDI2_DATA_AUX-
DDI2_CLK_AUX+
DDI2_SEL
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
DDI2_HPD
DDI2_DDC_AUX_SEL
SUS_S3#
DDI2_CTRLCLK_AUX+
DDI2_CTRLDATA_AUX-
DDI2_I2C_EN
DP2_AUX-
DP2_AUX+
DP2_CAD
DP2_HPD
TMDS2_HPD
TMDS2_D2+
TMDS2_D2-
TMDS2_D1+
TMDS2_D1-
TMDS2_D0+
TMDS2_D0-
TMDS2_CK+
TMDS2_CK-
TMDS2_I2C_CK
TMDS2_I2C_DAT
DP2_D0+
DP2_D0-
DP2_D1+
DP2_D1-
DP2_D2+
DP2_D2-
DP2_D3+
DP2_D3-
set jumper 1-2 for HDMI (default)
set jumper 2-3 for DVI dongle

3.2.3.14 Serial Port interface signals

According to COM Express® Rel. 2.1 specifications, since the COMe-A98-CT6 is a Type 6 module, it can offer two High Speed UART (HS UARTs) interfaces, which are managed by the AMD SoC.

Here following the signals related to UART interface:

SER0_TX: HS UART Interface #0, Serial data Transmit (output) line, 3.3V_S electrical level.

SER0_RX: HS UART Interface #0, Serial data Receive (input) line, 3.3V_S electrical level with a 47kΩ pull-up resistor.

SER1_TX: HS UART Interface #1, Serial data Transmit (output) line, 3.3V_S electrical level.

SER1_RX: HS UART Interface #1, Serial data Receive (input) line, 3.3V_S electrical level with a 47kΩ pull-up resistor.

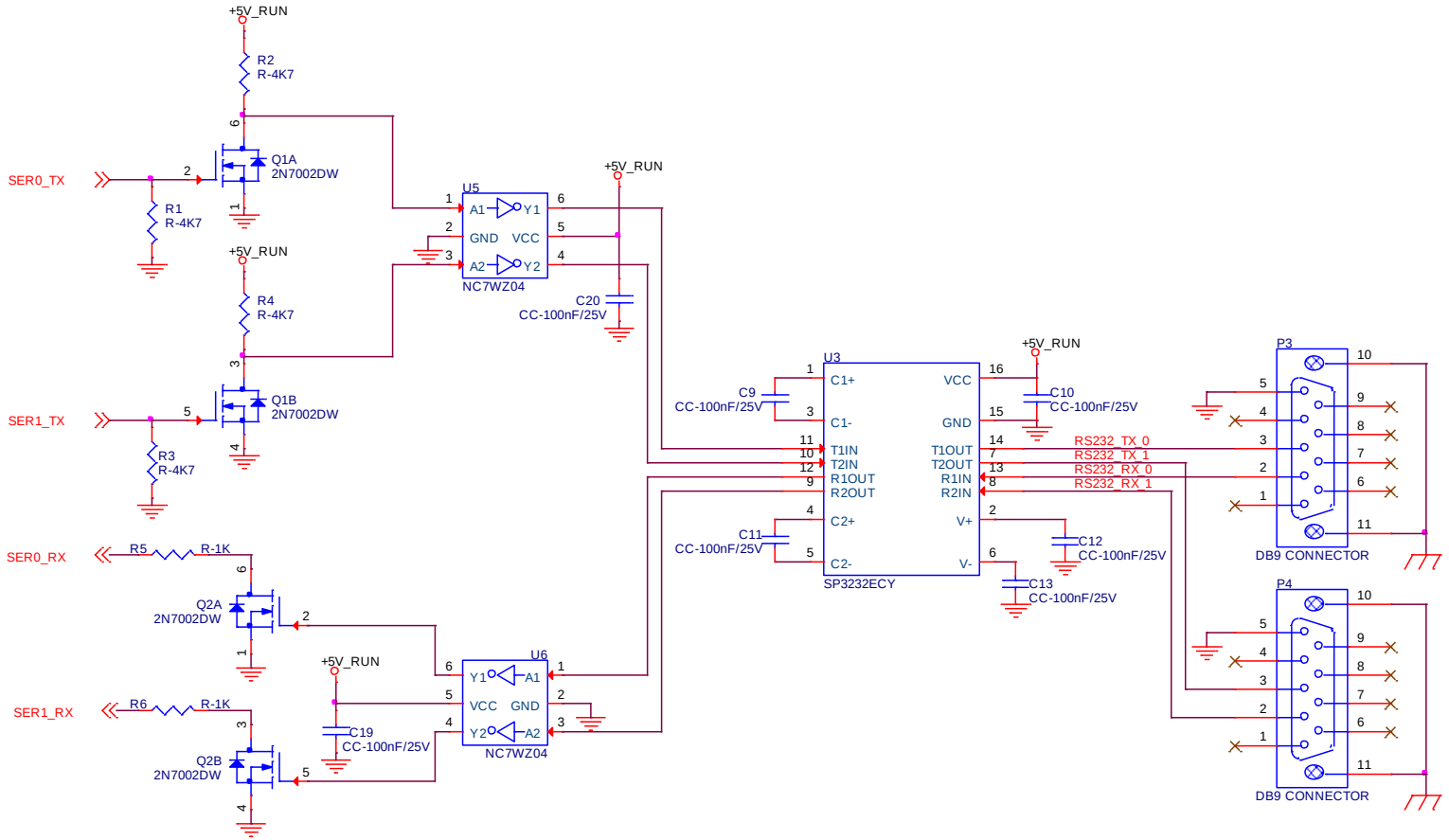
In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to +12V_{IN} power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then Schottky-diodes have been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the next page shows an example of implementation of RS-232 transceiver for the Carrier board.

Please be aware that the UARTs offered by the AMD SoCs are HS UARTs and not standard (legacy) COM ports.

Linux is able to manage them anyway, while Windows recognizes these interfaces as HS UART devices, not as legacy COM ports. This means that using Windows it is necessary to use specific drivers for the devices connected, it is not possible to use them using standard communication software like Tera Term, Putty…



3.2.3.15 I2C interface signals

This interface is managed by the embedded microcontroller.

Signals involved are the following

I2C_CK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_ALW with a 2K2Ω pull-up resistor.

3.2.3.16 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-A98-CT6 module.

SPKR: Speaker output, +3.3V_RUN voltage signal, managed by the embedded 3rd Generation R-Series SoCs.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_RUN voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWM_OUT*: PWM output for FAN speed management, +3.3V_RUN voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHIN*: External FAN Tachometer Input. +3.3V_RUN voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence pin. This signal is used to indicate Physical Presence to the optional TPM device onboard. It is an active high input signal.

THRM#: Thermal Alarm Input. Active Low signal, +3.3V_ALW voltage with 10kΩ pull-up resistor, managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_ALW voltage output signal. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the SoC began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

3.2.3.17 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the COMe-A98-CT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_RUN voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is needed.

PWR_OK: Power Good Input, +3.3V_RUN active high signal with 100kΩ pull-up resistor. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_RUN electrical voltage signal with 10kΩ pull-up resistor. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S4#: connected to SUS_S5# (see below).

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices that must become inactive only during S4 (Suspend to Disk) or S5 (Soft Off) power states.

WAKE0#: PCI Express Wake Input, active low +3.3V_ALW electrical voltage signal with 10kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_ALW electrical voltage signal with 2k2Ω pull-up resistor. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_ALW electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to LID# and SLEEP# inputs were dedicated to +12V_{IN} power rail. Protection circuitry has been added on LID# and SLEEP# so that they are +12V Tolerant. This has been made in order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then

3.2.3.18 SMBus signals

This interface is managed by the AMD 3rd Generation R-Series SoCs.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 4k7Ω pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_ALW with a 4k7Ω pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_ALW with a 10kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

3.2.3.19 GPIO/SDIO interface signals

According to COM Express® specifications rel. 2.1, there are 8 pins that can be used as General Purpose Inputs and Outputs **OR** as a SDIO interface.

The AMD 3rd Generation R-Series SoCs offer the SD Card management, while the four GPIs and the four GPOs are managed by the embedded microcontroller. The choice between SD and GPIO interface can be made via BIOS (please check paragraph 4.3.4).

All signals have an internal pull up of 8k2Ω, and are at +3.3V_RUN level. Please refer to the following table for a description of the signals in both configurations.

GPIO/SDIO Interfaces - Pin multiplexing					
		GPIO mode		SDIO mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
A54	GPI0	GPI0	General Purpose Input #0	SD_DATA0	SD Card Data Line 0.
A63	GPI1	GPI1	General Purpose Input #1	SD_DATA1	SD Card Data Line 2. Required only for 4-bit communication mode
A67	GPI2	GPI2	General Purpose Input #2	SD_DATA2	SD Card Data Line 2. Required only for 4-bit communication mode
A85	GPI3	GPI3	General Purpose Input #3	SD_DATA3	SD Card Data Line 1. Required only for 4-bit communication mode
A93	GPO0	GPO0	General Purpose Output #0	SD_CLK	SD Clock Output
B54	GPO1	GPO1	General Purpose Output #1	SD_CMD	SD Command/Response line. Bidirectional signal, used to send command from Host to the connected card, and the response from the card to the Host.
B57	GPO2	GPO2	General Purpose Output #2	SD_WP	Write Protect input. It is used to communicate the status of Write Protect switch of the external SD card.
B63	GPO3	GPO3	General Purpose Output #3	SD_CD#	Card Detect Input, active low Signal. This signal must be externally pulled low to signal when a SD Card Device is present.

Special consideration about SD_WP signal: since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal is tied to GND, otherwise the OS will always consider the card as protected from writing.

3.2.4 BOOT Strap Signals

Configuration straps are signals that, during system reset, are set as inputs (independently by their behaviour during normal operations) in order to allow the proper configuration of the SoC. For this reason, on COMe-A98-CT6 are placed the pull-up or pull-down resistors that are necessary to configure the board properly.

The customer must avoid to place, on the carrier board, pull-up or pull-down resistors on signals that are used as strap signal, since it could result in malfunctions of COMe-A98-CT6 module.

The following signals are used as configuration straps by COMe-A98-CT6 module at system reset.

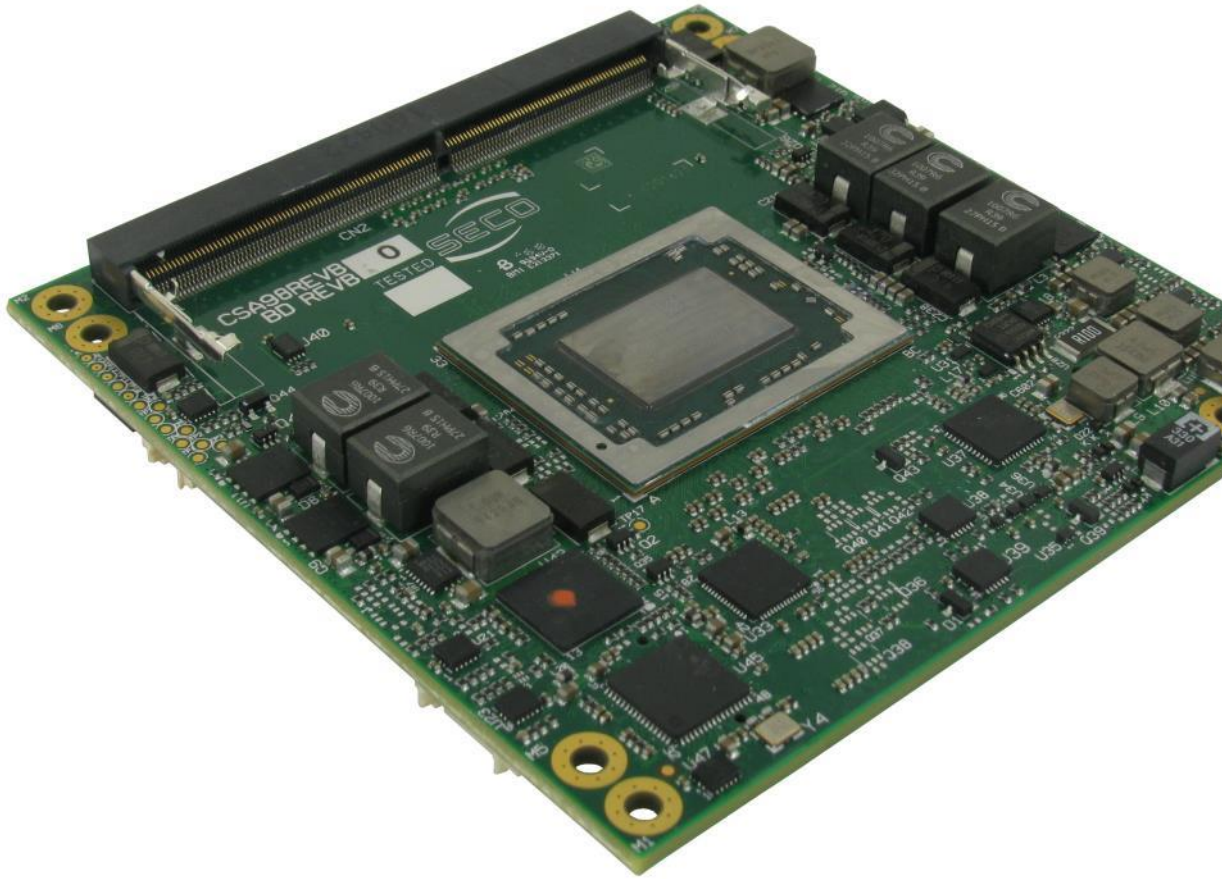
LPC_CLK: pin B10 of connector AB. Used to enable/disable the BOOT Fail Time. Signal at +3.3V_RUN voltage level with a 2kΩ pull-down resistor.

LPC_FRAME#: pin B3 of connector AB. Used to enable the boot from SPI Flash. Signal at +3.3V_RUN voltage level with a 10kΩ pull-up resistor.

SYS_RESET #: pin B49 of connector AB. Used to enable normal reset mode. Signal at +3.3V_ALW voltage level with a 10kΩ pull-up resistor.

Chapter 4.
BIOS SETUP

- InsydeH2O setup Utility
- Main setup menu
- Advanced menu
- Security menu
- Power menu
- Boot menu
- Exit menu



4.1 InsydeH2O setup Utility

Basic setup of the board can be done using Insyde Software Corp. “InsydeH2O Setup Utility”, that is stored inside an onboard SPI Serial Flash.

It is possible to access to InsydeH2O Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select “Setup Utility” item.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
<F5> / <F6>	<F5> and <F6> keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows to display the General Help screen.
<F9>	<F9> key allows loading Setup Defaults for the board. After pressing <F9> BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<F10>	<F10> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows to discard any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow to display the setup sub- screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Memory Configurations	See submenu	Setting Memory Controller features and memory clocks
PCI Express Configurations	See submenu	Configures settings for PCI Express
Boot Configuration	See submenu	Configures settings for Boot Phase
Peripheral Configuration	See submenu	Configures the peripherals
SATA Configuration	See submenu	Options to configure the SATA Host controller and the drives connected to the system
Video Configuration	See submenu	Configures the options for video section
USB Configuration	See submenu	Configures the USB support
ACPI Table/Features Control	See submenu	Configures the parameters for ACPI management
CPU Related settings	See submenu	Configures CPU related parameters
Super I/O Configuration	See submenu	Super I/O Setup Configuration Utility. Only available when a SuperI/O is found on the Carrier board
Console redirection	See submenu	Configures the parameters for redirection of video output on internal UARTs

4.3.1 Memory configurations submenu

Menu Item	Options	Description
Memory clock setting mode select	Auto Limited Specific	Sets memory clock management. In Auto mode, the memory clock will be set by reading SPD data. In Limited mode, if the clock value read through SPD is higher than the memory clock limit, than the memory clock will be set according to the limit, otherwise it will set itself according to the SPD data. In Specific mode, the memory clock will always run at the specific value.
Select memory clock value	800MHz / 1066MHz / 1333 MHz / 1600MHz / 1866MHz / 2133MHz	This menu item is available only when “Memory clock setting mode select” is not set to Auto. Sets a memory clock limit or a specific memory clock.
Memory Bank interleaving	Disabled / Enabled	Enable or disable the Memory Bank interleaving
Memory Channel interleaving	Disabled / Enabled	Enable or disable the Memory Channel interleaving
Phy PLL PD bypass mode	Disabled / Enabled	When Enabled, supports high rate memory modules. When Disabled, supports low power solid down memories
Memory Power Down	Disabled / Enabled	Enable or disable the memory power down feature
Memory ECC Enable	Disabled / Enabled	Enable or Disable the ECC correction using the recommended AMD settings. ECC features will not work unless this feature is enabled

4.3.2 PCI Express configuration submenu

Menu Item	Options	Description
Spread Spectrum	Disabled / Enabled	Enable or disable the Spread spectrum on PCI-e clock
PSPP Policy	Disabled / Performance / Balanced High / Balanced Low/ Power Saving / Auto	PCIe Speed Power policy: the processor can dynamically support the changing to the link frequency due to changes in system configuration and power policy.
IOMMU Support	Disabled / Enabled	Enable or disable the support for IOMMU (IO Memory Management Unit. Also known as AMD Virtualization™ Technology).
GFX PCI-E Lane Grouping	x8 / x4 x4	Allows the configuration of PCI-e Graphics (PEG) in a single port PCI-e x8 or two ports PCI-e x4
GFX #0	See following options	Configuration options for PEG x8 port or first PEG x4 port
GFX #1	See following options	This item will be available only when “GFX PCI-E Lane Grouping” is set to “x4 x4”. Configuration options for second PEG x4 port

GPP PCI-E Lane Grouping	x1 x1 x1 x1 x2 x1 x1	Allows the configuration of PCI-e ports in four single PCI-e x1 ports or a port PCI-e x2 + 2 x PCI-e ports x1
GPP #0 GPP #1 GPP #2 Internal LAN	See following options	Configuration options for PCI-e ports #0÷#3. GPP #1 will be available only when "GPP PCI-E Lane Grouping" is set to " x1 x1 x1 x1" (i.e. 4 PCI-e ports x1). The fourth PCI-e port (GPP#3) is used for the management of the Gigabit Ethernet controller

4.3.2.1 GFX #x / GPP #x / Internal LAN Features submenu

Menu Item	Options	Description
Enabled	Auto / Disabled / Enabled	Use this item to enable this PCI-e port. AUTO means this port will follow its default implementations. Please be aware that GPP Port#3 on COMe-A98-CT6 module is connected to the Gigabit Ethernet Controller (Internal LAN). Disabling GPP Port #3, therefore, will result in disabling Ethernet interface.
Hotplug Support	Disabled / Basic / Enhanced	This menu item is available only when corresponding GFX or GPP port is set to Enabled. Sets the support for the Hotplug. Not available for "Internal LAN" menu item.
Speed Mode	Auto / Gen1 / Gen2 / Gen3	This menu item is available only when corresponding GFX or GPP port is set to Enabled. Set PCI-e ports link speed/capability
Link ASPM	Disabled / L0s	This menu item is available only when corresponding GFX or GPP port is set to Enabled. Manages PCI Express L0s power states, for OSs able to handle Active State Power Management (ASPM)

4.3.3 Boot configuration submenu

Menu Item	Options	Description
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off
Wait for slow peripherals reset	0 ÷ 10	This item allows to select a variable amount of time, in the range 0 ÷10 seconds, that the system must wait before enumerating the peripherals, in order to handle slower/delayed devices.

4.3.4 Peripheral configuration submenu

Menu Item	Options	Description
SERIRQ Continuous Mode	Disabled / Enabled / Auto	Allow Enabling the Continuous mode of working for SERIRQ. When Enabled, the SERIRQ working is set to Quiet Mode
Trust Platform Module	Disabled Enable Device TPM Enable firmware TPM	Enable or Disable TPM Physical presence. It is necessary to reboot after enabling, before selecting TPM operations.
HD Audio Device	Enabled Disabled	Controls the detection of the HD Audio Controller Enable the HD Audio Codec if present on the Carrier board . Enabled: the Audio controller will be unconditionally Enabled
SDIO / GPIO Select	GPIO / SDIO	Select the GPIO or SD Card function on multiplexed pins (please check par. 3.2.3.19).
GPO0 / GPO1 / GPO2 / GPO3	Low / High / Last	This item is available only when “SDIO / GPIO Select” is set to GPIO. Allows setting the initial value of each general Purpose output, i.e. if they must be High at boot, Low at boot or have the same value that they had assumed before the last boot
UART Controller 0	Enabled / Disabled	Enable or disable the internal UART Controller #0
UART Controller 1	Enabled / Disabled	Enable or disable the internal UART Controller #1

4.3.5 SATA configuration submenu

Menu Item	Options	Description
SATA Controller	Disabled / Enabled	Enabled: Enable the SATA controller. Disabled: Disable the SATA controller.
SATA Maximum Speed	SATA II SATA III	Sets SATA Maximum Speed. It is possible to choose between SATA III (default) and SATA II
SATA Configure As	IDE AHCI	Set SATA Configuration type. Can be set only when “SATA Controller” is Enabled. With AHCI, is not possible to install/boot UEFI O.S., only Legacy OS can be installed (a simpler driver is required). Setting to IDE, the controller is managed as a PCI device, so addresses reallocation and INT line sharing is possible.
Serial ATA Port 0 Serial ATA Port 1		Shows information related to eventual devices connected to SATA ports 0 or 1.

4.3.6 Video configuration submenu

Menu Item	Options	Description
Primary Video Adaptor	Int. Graphics (IGD) Ext. Graphics (PEG)	Allows to select if Internal Graphics controller (IGD) or external PCI-e Graphic Controller x8 (PEG) should be used as a Primary display
HDMI Audio	Disabled / Enabled	Enable or Disable Audio on HDMI
Force IGPU Disabled	Yes / No	Force to disabled the iGPU
UMA size (MB)	Auto / 32 / 64 / 128 / 256 / 512 / 1024 / 2048	This menu item is available only when the module has not the iGPU forced to disabled. Select the UMA (Unified memory Architecture) size. In "Auto" mode, only the UMA necessary for the video requirements will be reserved. Other items will reserve a specific size of memory to UMA
DDI0 DDI1 DDI2	Enabled / Disabled	Allow to enable or disable the single DDI ports
LVDS Color Mode	VESA 24bpp JEIDA 24bpp 18 bpp	This menu item is available only when the module has the eDP-to-LVDS bridge installed. Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
LFP Interface	Single Channel Dual Channel	This menu item is available only when the module has the eDP-to-LVDS bridge installed. Allows configuration of LVDS interface in Single or Dual channel mode
LVDS Advanced Options	See Submenu	Advanced options for LVDS panel configuration
LVDS EDID	External / Custom / 600x480 / 800x480 / 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	This menu item is available only when the module has the eDP-to-LVDS bridge installed. Select a software resolution (EDID setting) to use for the internal flat panel
LVDS Custom Parameters	See Submenu	Select Detailed Timing Descriptor Parameters

4.3.6.1 LVDS Advanced options submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
LVDS Spreading Depth	No Spreading / 0.5% / 1.0% / 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum

LVDS Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing
T3 Timing	0 ÷ 255	Minimum T3 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 10 (500ms)
T4 Timing	0 ÷ 255	Minimum T4 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 2 (100ms)
T12 Timing	0 ÷ 255	Minimum T12 timing of panel power sequence to enforce (expressed in units of 50ms). Default is 20 (1s)
T2 Delay	Enabled / Disabled	When Enabled, T2 is delayed by 20ms ± 50%
T5 Delay	Enabled / Disabled	When Enabled, T5 is delayed by 20ms ± 50%
P/N Pairs Swapping	Enabled / Disabled	Enable or disable LVDS Differential pairs swapping (Positive ⇔ Negative)
Pairs Order Swapping	Enabled / Disabled	Enable or disable channel differential pairs order swapping (A ⇔ D, B ⇔ CLK, C ⇔ C)
LVDS BUS Swapping	Enabled / Disabled	Enable or disable Bus swapping (Odd ⇔ Even)

4.3.6.2 LFP Custom submenu

Using this submenu, it is possible to set all the following parameters to meet the LVDS display requirements.

Menu Item	Options	Description
Pixel Clock / 10000	Any value in range [2500..22400]	Working Frequency in 10kHz units, e.g 6350 → 63.5MHz. Allowed range from 2500 (25MHz) to 22400 (224MHz)
Horizontal Active	Any value in range [1..4095]	Horizontal Addressable Video in pixels, a.k.a. Horizontal resolution (e.g. 1024 on a 1024x768 LFP)
Horizontal Blank	Any value in range [1..4095]	Horizontal Blanking in pixels, equals to Horizontal Total (Horizontal Active + Horizontal Front Porch + Horizontal Black Porch)
Vertical Active	Any value in range [1..4095]	Vertical Addressable Video in pixels, a.k.a. Vertical resolution (e.g. 768 on a 1024x768 LFP)
Vertical Blank	Any value in range [1..4095]	Vertical Blanking in pixels, equals to Vertical Total (Vertical Active + Vertical Front Porch + Vertical Black Porch)
Horizontal Offset	Any value in range [1..1023]	Horizontal Front Porch in pixels
Horizontal Pulse	Any value in range [1..1023]	Horizontal Sync Pulse Width in pixels
Vertical Offset	Any value in range [1..63]	Vertical Front Porch in pixels
Vertical Pulse	Any value in range [1..63]	Vertical Sync Pulse Width in pixels
Horizontal Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)
Vertical Polarity	Negative / Positive	Sync Signal Polarity: Default is Negative (Active Low)

4.3.7 USB configuration submenu

Menu Item	Options	Description
EHCI (Ports 4-7)	Enabled / Disabled	Enables or disables the EHCI controller, which takes control of USB 2.0 ports #4 ÷ #7
xHCI (Ports 0-3)	Enabled / Disabled	Enables or disables the xHCI controller, which takes control of all Superspeed ports and USB 2.0 ports #0 ÷ #3
USB BIOS Support	Enabled / Disabled /UEFI only	Sets the support for USB keyboard / mouse / storage under UEFI and DOS environment. When set to UEFI only, then it will support exclusively UEFI environment.

4.3.8 ACPI Table/Features Control submenu

Menu Item	Options	Description
FACP – RTC S4 Wakeup	Enabled / Disabled	Enable or disable FACP (Fixed ACPI Description Table) support for S4 wakeup from RTC
HPET - HPET Support	Enabled / Disabled	High Precision Event Timer is supported in Windows Vista or above. HPET controller should not been seen in Windows XP, independently by the SCU setting. When this feature is enabled, the HPET table will be added into ACPI Tables.
_OSC Support	Enabled / Disabled	Enable or Disable ACPI Operating System Capabilities (_OSC) Method to communicate to the O. S. which features available in the system can be controlled by the operating system
Adaptive S4	Enabled / Disabled	Enable or Disable the Adaptive S4

4.3.9 CPU related setting submenu

Menu Item	Options	Description
SVM support	Enabled / Disabled	Enable or Disable Secure Virtual Machine Mode (SVM) support, for users who require to use Virtual Machines
SMM Code Lock	Enabled / Disabled	Enable or disable locking of the SMM (System Management Mode) code segment / registers for preventing changes to the internal code/registers

4.3.10 SuperI/O configuration submenu

Menu Item	Options	Description
Name of the SuperI/O found		This menu item will show the name of all the Super I/Os that are found on the carrier board. By selecting the adequate SuperI/O, it will be possible to set the serial ports and possibly other parameters as shown in the following menu items. If no Super I/O is available on the Carrier Board, this menu will not be available.
Keyboard Controller	Enabled / Disabled	Enable / disable the Keyboard Controller (if the SuperI/O supports it, otherwise this item will not be available).
Serial Port 1 / Serial Port 2 / Serial Port 3 / Serial Port 4	Enabled / Disabled	Enable or Disable single serial port #1, #2, #3 or #4 (the number of serial ports depends on the Super I/O).
Address	0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each Serial Port, if enabled.
IRQ	3 / 4 / 5 / 6/ 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.
Floppy Disk Controller	Enabled / Disabled	Enable / disable the Floppy Disk Controller, if the SuperI/O supports it
Parallel Port Mode	Parallel Port / External FDC	Configure the Parallel Port mode of working, if the SuperI/O supports it
LPT Port	Enabled / Disabled	When the previous item is set to “Parallel Port”, this item will allow to enable or disable the LPT port.
LPT Mode	SPP / EPP 1.9 and SPP / ECP / ECP-EPP 1.9 / Printer Mode / EPP 1.7 and SPP / ECP-EPP 1.7	When the LPT port is enabled, this item will allow to configure the LPT protocol
Hardware Monitor	Enabled / Disabled	Enable or disable the Super I/O Hardware monitor (if it is supported by the Super I/O)
Watchdog	Disabled / 1 Minute / 2 Minutes / 3 Minutes	Enable or Configure the Super I/O Watchdog (if the Super I/O Used supports it, otherwise this item will not be available)

4.3.11 Console Redirection submenu

Menu Item	Options	Description
Console Serial Redirect	Enabled / Disabled	Enable or disable Console redirection. When enabled, all the submenus of the following paragraph will appear
Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Set Console Redirection terminal type
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Set Console Redirection baud rate
Data Bits	7 bits / 8 bits	Set Console Redirection data bits
Parity	None / Even / Odd	Set Console Redirection parity bits
Stop Bits	1 bit / 2 bits	Set Console Redirection stop bits
Flow Control	None RTS/CTS XON/XOFF	Set Console Redirection flow control type
Information Wait Time	0 Seconds / 2 Seconds / 5 Seconds / 10 Seconds / 30 Seconds	Set Console Redirection port information display time
C.R. After Post	Yes / No	Console Redirection continues to work even after Bios POST.
Text Mode Resolution	AUTO Force 80x25 Force 80x24 (DEL FIRST ROW) Force 80x24 (DEL LAST ROW)	Select the Text Mode resolution for the Console Resolution. With Auto, the text will follow the VGA resolution. Force 80x25 will ignore the VGA resolution and force the video text output to 80 char x 25 rows Force 80x24 (DEL FIRST ROW) will ignore the VGA resolution and force the video text output to 80 characters x 24 rows, deleting the first row. Force 80x24 (DEL LAST ROW) will ignore the VGA resolution and force the video text output to 80 characters x 24 rows, deleting the last row.
AutoRefresh	Enabled / Disabled	When this feature is enabled, the screen will auto refresh once after detecting the connection of a remote terminal
FailSafeBaudRate	Enabled / Disabled	This feature will auto detect remote terminal baud rate and connect C.R serial device with detected baud rate
ACPI SPCR Table	Enabled / Disabled	Serial Port Console Redirection Table. When this feature is enabled, the SPCR table will be add-into ACPI tables.

4.4 Security menu

Menu Item	Options	Description
BIOS Firmware Volume	Enabled / Disabled	Measuring of PEI phase loaded PE images. Affects PCR[0]. Changes with BIOS updating.
Separator	Enabled / Disabled	Measuring separation from pre-boot and post-boot environment. Affects all BIOS PCRs (PCR[0-7]). Does never change.
SMBIOS Table	Enabled / Disabled	Measuring SMBIOS Tables. Affects PCR[1]. Changes with Hardware configuration (e.g. RAM) and BIOS updating-
Legacy BIOS	Enabled / Disabled	Measuring Legacy BIOS. Affects PCR[2]. Rarely changes with BIOS updating.
PE images	Enabled / Disabled	Measuring of DXE phase loaded PE images. Affects PCR[2] (drivers) and PCR[4] (applications). Changes with BIOS updating and/or different Operating Systems loaders.
Boot Sequence	Enabled / Disabled	Measuring of Boot order, Boot Devices and Boot Sequence. Affects PCR[5]. May change across different boot sessions, even with the same setup settings.
Secure boot	Enabled / Disabled	Measuring of Secure Boot Variables and Data. Affects PCR[7]. Changes Enabling and Disabling the Secure Boot. May change with BIOS updating.
Post Code	Enabled / Disabled	Measuring of Post Code ACPI Table Loading. Affects PCR[0]. Rarely, changes with BIOS updating
Set Supervisor Password		Install or Change the password for supervisor. Length of password must be greater than one character.
Power on Password	Enabled / Disabled	Available only when Supervisor Password has been set. Enabled: System will ask to input a password during P.O.S.T. phase. Disabled: system will ask to input a password only for entering Setup utility

4.5 Power menu

Menu Item	Options	Description
Set cTDP Value	Auto / 12 / 15 / 25 / 35	Sets the Configurable TDP Value in Watt Units
Watchdog Configuration	See submenu	Configures various parameters for Watchdog
Thermal Configuration	See submenu	Thermal Zone Configuration: Active and Passive Cooling Settings.
Reset Causes Handling		By selecting this item, an information screen with the handling of latest resets causes will appear.
Hardware Monitor		By selecting this item, and information screen with System parameters will appear
ACPI S3	Enabled / Disabled	Enable or Disable ACPI S3 Sleep State
Wake on PME	Enabled / Disabled	Determines whether the system must wake up or not when the system power is off and occurs a PCI Power Management Enable wake-up event.
Auto Wake on S5	Disabled By Every Day By Day of Month	Auto wake up from S5 state, it can be set to happen “By Every Day” or “By Day of Month”
Wake on S5 time	[hh:mm:ss]	This menu item is available only when “ Auto Wake on S5” is set to “By Every Day” of “By Day of Month”. Set time of the day when the board must wake up automatically
Day of month	1 ÷ 31	This menu item is available only when “Auto Wake on S5” is set to “By Day of Month” This is the help for the day field. Valid range is from 1 to 31. Error checking will be done against month/day/year combinations that are not supported. Use + / - to Increase / reduce
LID# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configure LID_BTN# Signal as always open or closed (i.e., Force Open / Force Closed), no matter the pin level, or configures the signal polarity: “Normal Polarity” means the signal goes High when open, “Inverted Polarity” means the signal goes Low when open
LID# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	This item can be changed only when “LID # Configuration” is not set to Force Open or Force Closed. Configure LID # Wake capability. According to the pin configuration, when the LID is open it can cause a system wake from a sleep state
SLEEP# Wake	Enabled / Disabled	Disable or enable the capability of SLEEP# signal to wake the system from S3/S4 states.
SMB_ALERT# Wake Configuration	No Wake Only from S3 Wake from S3/S4/S5	Configures the Wake Capabilities of SMB_ALERT#signal

Battery less Operation	Disabled / Enabled	This item has to be enabled in case that the RTC battery is not present on the Carrier board
Power Fail Resume Type	Always ON Always OFF Last State	Determine the System Behavior after a power failure event. In case the option is “Always ON”, the board will start every time the power supply is present. When the option is “Always OFF”, the board will not start automatically when the power supply returns. Finally, if this option is set to “Last State”, the board will remember the state it had when the power supply went down: so, if the board was on, it will start again when the power returns, and will remain off if the board was in this state when the power went down.

4.5.1 Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Disabled / Enabled	Enables or disables the Watchdog Timer Mechanism. When disabled, all remaining menu options will be not accessible.
Event Action	Raise WDT signal Power Button Pulse None	Select the action that will performed when the Watchdog event time-out expires
Reset Action	System Reset Power Button Override Raise WDT Signal	Select the action that will performed when the Watchdog Reset time-out expires
Watchdog Delay	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes of delay, after system power up, before the watchdog Event timeout starts counting. During the delay timeout, a refresh operation will immediately trigger to normal operations.
Event Time-Out	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the Event action triggers. A refresh will restart this timeout
Reset Time-Out	1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the reset action triggers. A refresh will restart to the beginning of the event Timeout.

4.5.2 Thermal configuration submenu

Menu Item	Options	Description
Critical Temperature (°C)	80 / 85 / 90 / 95 / 100	Above this threshold, an ACPI aware OS will perform a critical shut down
Passive Cooling Temperature (°C)	60 / 65 / 70 / 75 / 80 / 85 / 90 / Disabled	Above this threshold, an ACPI aware OS will start to lower the SoC speed.
TC1	0..16	Thermal Constant 1: Part of the ACPI Passive Cooling Formula
TC2	0..16	Thermal Constant 2: Part of the ACPI Passive Cooling Formula
TSP (seconds)	2..32	Period of temperature sampling when Passive Cooling
Internal FAN PF Duty Cycle (%)	0..100	Duty Cycle when resuming from Power Failure (G3→S0)
Internal FAN Control	Enabled / Disabled	Disable or Enable Thermal Feedback FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Internal FAN Control" is Enabled Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when "Internal FAN Control" is Enabled. Select the lowest temperature under which the onboard fan must be OFF.
Temperature Hysteresis	0 .. 10	Only available when "Internal FAN Control" is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when "Internal FAN Control" is Enabled. Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the fan will run at full speed.
Speed Change Duration	0 .. 50	Only available when "Internal FAN Control" is Enabled. Duration in seconds of linear FAN Speed Change.
FAN Duty Cycle	0 .. 100	Only available when "Internal FAN Control" is Disabled. Default FAN Duty Cycle (%).
FAN_PWMOUT Device Type	3-Wire FAN 4-Wire FAN Generic PWM	Specifies if a 3-Wire (Default) or a 4-Wire FAN is connected to FAN_PWMOUT / FAN_TACHOIN signals. Generic PWM has to be used when the signal is not used to drive a FAN.
FAN_PWMOUT frequency	1 .. 60.000	Sets the frequency of the FAN_PWMOUT signal. If fed to a FAN, typical values are 100 for a 3-Wire device and 20.000 for a 4-Wire one.

External FAN PF Duty Cycle (%)	0 .. 100	Only available when “External FAN Type” is not set to Generic PWM. Duty Cycle when resuming from Power Failure (G3→S0)
External FAN Control	0 .. 100	Only available when “External FAN Type” is not set to Generic PWM. Disable or Enable Thermal Feedback FAN Control
AC0 Temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when “External FAN Control” is Enabled Select the highest temperature above which the external fan must work always at Full Speed
AC1 Temperature (°C)	5 / 10 / 15 / 20 /25 / 30 / 35 / 40 / 45 / 50 / 55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100	Only available when “External FAN Control” is Enabled. Select the lowest temperature under which the external fan must be OFF.
Temperature Hysteresis	0 .. 10	Only available when “External FAN Control” is Enabled. Value added (when temperature is growing) to the ACx thresholds or subtracted from them (when temperature is decreasing) to avoid oscillations.
FAN Duty Cycle (%) Above AC1	0 .. 100	Only available when “External FAN Control” is Enabled. Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed.
Speed Change Duration	0 .. 50	Only available when “External FAN Control” is Enabled. Duration in seconds of linear FAN Speed Change.
FAN Duty Cycle (%)	0 .. 100	Only available when “FAN_PWMOUT Device Type” is not set to Generic PWM and External FAN Control is Disabled. Default FAN Duty Cycle (%)
FAN_PWMOUT PF Duty Cycle (%)	0 .. 100	Only available when “FAN_PWMOUT Device Type” is set to Generic PWM. Default FAN_PWMOUT Duty Cycle (%) when resuming from Power Failure (G3→S0).
FAN_PWMOUT Duty Cycle (%)	0 .. 100	Only available when “FAN_PWMOUT Device Type” is set to Generic PWM. Default FAN_PWMOUT Duty Cycle (%) during boot

4.6 Boot menu

Menu Item	Options	Description
Boot with battery low	Normal Inhibit OS Force S5	When this menu item is set to “Normal” (default), then the BATLOW# signal will be ignored. When this menu item is set to “Inhibit OS”, then the system will not perform the boot to OS in case that the signal BATLOW# is asserted (Low). When this menu item is set to “Force S5”, then the system will not leave S5 state in case that the signal BATLOW# is asserted (Low).
Boot type	Dual boot Type Legacy Boot Type UEFI Boot Type	Allows to select if the OS must be booted using Legacy Boot Mode, UEFI Boot mode or indifferently using both modalities (depending on the OS)
Quick Boot	Enabled / Disabled	Skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Enabled / Disabled	Disables or enables booting in Text Mode.
Display ESC Key Strings	Enabled / Disabled	Display or Hide the “ESC key” strings during the BIOS boot. Disabling this configuration, no information on how to enter Setup Configuration Utility will be displayed.
Display Boot Logo	Enabled / Disabled	Enable or display the visualization of a logo during Boot phase
Logo Persistence Time (s)	0 ÷ 10	This submenu is available only when “Display Boot Logo” is set to Enabled. Forced wait time in seconds during the boot logo visualization. 0 means boot as fast as possible. Even with 0 wait time, UEFI OSes supporting BGRT table will display the logo while booting.
Network Stack	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “UEFI Boot type” or “Dual Boot type”. When enabled, this option will make available the following Network Stack services: Windows 8 BitLocker Unlock UEFI IPv4/IPv6 PXE Legacy PXE OpROM
PXE Boot Capability	Disabled UEFI: IPv4 UEFI: IPv6 UEFI: IPv4/IPv6 Legacy	This submenu is available only when “Network Stack” is Enabled Specifies the PXE (Preboot Execution Environment) Boot possibilities. When Disabled, Network Stack is supported For UEFI, it is possible to support IPv4, IPv6 or both of them In Legacy mode, only Legacy PXE OpROM is supported
PXE Boot to LAN	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “Legacy Boot type”. Disables or enables the possibility for the PXE to perform the boot from LAN.

Power Up in Standby Support	Enabled / Disabled	Disable or enable Power Up in Standby Support. The PUIS feature set allows devices to be powered-up in the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot options	First / Last / Auto	Specifies the position in Boot Order for Shell, Network and Removable Disks
ACPI selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0	Using this menu item is possible to select to which specifications release the ACPI tables must be compliant.
USB Boot	Enabled / Disabled	Disables or enables booting from USB boot devices.
EFI Device First	Enabled / Disabled	Determine if boot must happen first through EFI devices or through legacy devices. When enabled, it will happen first from EFI devices. When disabled, it will happen first from Legacy devices.
UEFI OS Fast Boot	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type. If enabled, the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type and “UEFI OS Fast Boot” is Enabled. Enable or disable the support for USB HotKeys while booting. This will decrease the time needed to boot the system
Timeout	0 ÷ 10	The number of seconds that the firmware will wait before booting the original default boot selection.
Automatic Failover	Enabled / Disabled	When this item is enabled, if boot from the default device fails, then the system will attempt directly to boot from the next device on the Boot devices list When this item is disabled, in case of failure from booting from the first boot device, then a Warning Message will pop up and subsequently enter into Firmware UI.
EFI	See Submenu	This submenu is available only when “Boot Type” is not set to “Legacy Boot type”. Entering the submenu, will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.
Legacy	See Submenu	This submenu is available only when “Boot Type” is not set to “UEFI Boot type”. Entering the submenu, will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.

4.6.1 Legacy submenu

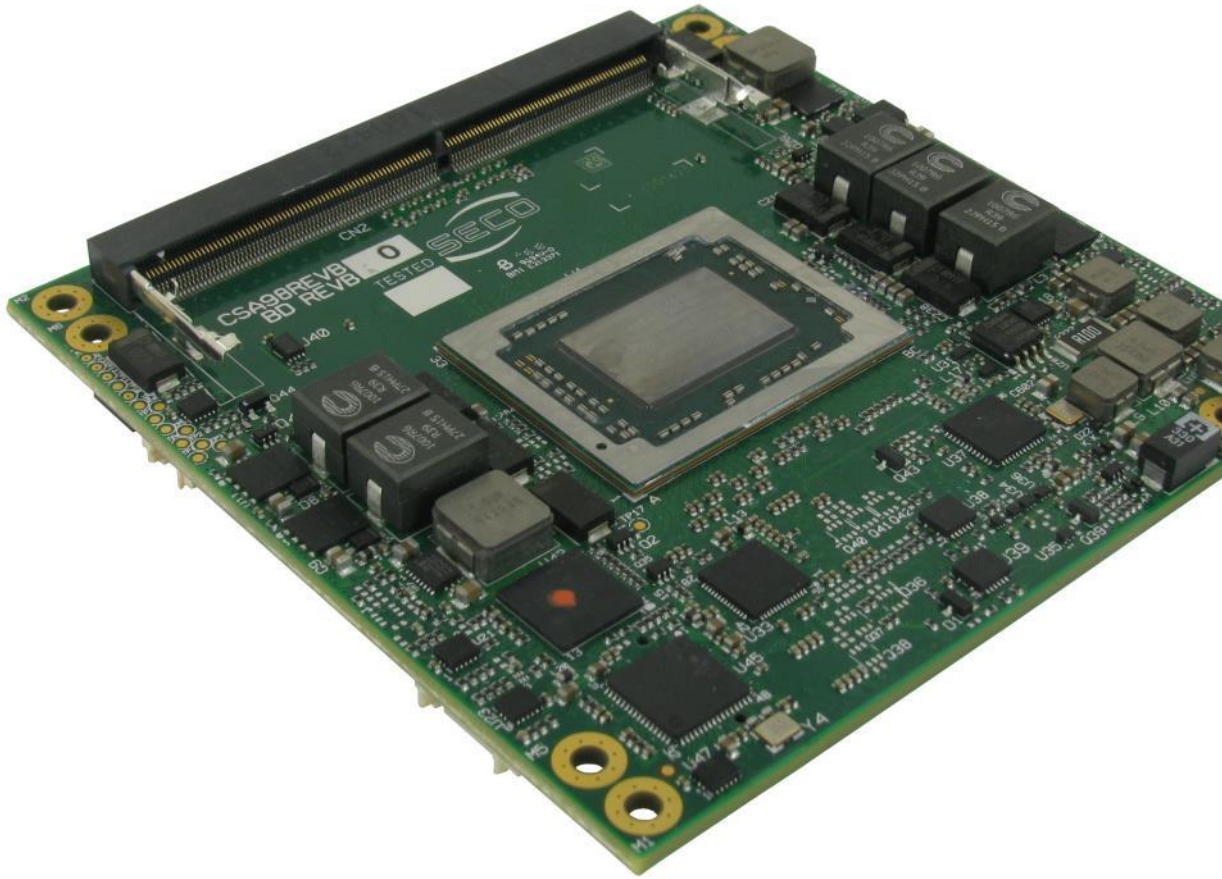
Menu Item	Options	Description
Boot Menu	Normal / Advance	When set to Normal, this submenu will allow configuring all possible options for Legacy boot. When set to Advance, it will be possible to configure Boot Order only for bootable devices found in the system
Boot Type Order	Floppy Drive / Hard Disk Drive CD/DVD-ROM Drive / USB / Others	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will allows selecting the boot from different devices. Use the + and - Keys to change the boot order priority
Hard Disk Drive	*List of HD Drives found connected*	This voice will be selectable only when “Boot menu” is set to “Normal” and if there are HD drives connected. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority
USB	*List of USB Drives found connected*	This voice will be selectable only with “Boot menu” set to “Normal” and if there are USB disks connected. The list shown under this item will show different USB disks found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority

4.7 Exit menu

Menu Item	Options	Description
Exit Saving Changes		Exit system setup after saving the changes. F10 key can be used for this operation.
Save Change Without Exit		Save all changes made, but doesn't exit from setup utility.
Exit Discarding Changes		Exit system setup without saving any changes. ESC key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup items. F9 key can be used for this operation.
Load Custom Defaults		Load Custom Default values for all the setup items.
Save Custom Defaults		Save Custom Default values for all the setup items.

Chapter 5.
Appendices

- Thermal Design



5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-A98-CT6 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-A98-CT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-A98-CT6 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
MA98-DISS-1-PK	COMe-A98-CT6 Heat Spreader (passive), packaged
MA98-DISS-3-H-PK	COMe-A98-CT6 Heat Sink (active), Horizontal Fins orientation, packaged
MA98-DISS-3-V-PK	COMe-A98-CT6 Heat Sink (active), Vertical Fins orientation, packaged

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