Com express

User Manual

COMe-A41
CT6

COM-Express™ Type 6 Module with the
Intel® Bay Trail family SOCs

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	28th January 2016	First Release	SB

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist you.

INDEX

Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site http://www.seco.com/en/prerma (RMA Online). The RMA Authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.r.l. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.r.l. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The COMe-A41-CT6 module uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The COMe-A41-CT6 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a COMe-A41-CT6 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The COMe-A41-CT6 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
AHCI	Advanced Host Controller Interface, a standard which defines the operation modes of SATA interface
API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CRT	Cathode Ray Tube. Initially used to indicate a type of monitor, this acronym has been used over time to indicate the analog video interface used to drive them.
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock
DDR3	DDR, 3rd generation
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface specifically developed for the internal connections between boards and displays
EHCI	Enhanced Host Controller interface, a high-speed controller for USB ports, able to support USB2.0 standard
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD. The eMMC are the embedded version of the MMC. They are devices that include both the memory controller and the flash memories on a single BGA chip.
N.A.	Not Applicable

N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OS	Operating System
PCI-e	Peripheral Component Interface Express
PSU	Power Supply Unit
PWM	Pulse Width Modulation
PWR	Power
PXE	Preboot Execution Environment, a way to perform the boot from the network ignoring local data storage devices and/or the installed OS
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like smart batteries and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signaling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UEFI	Unified Extensible Firmware Interface, a specification defining the interface between the OS and the board's firmware. It is meant to replace the original BIOS interface
USB	Universal Serial Bus
V_REF	Voltage reference Pin
VGA	Video Graphics Array, an analog computer display standard, commonly referred to also as CRT
xHCI	eXtensible Host Controller Interface, Host controller for USB 3.0 ports, which can also manage USB 2.0 and USB1.1 ports

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
AHCI	http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html
Com Express	http://www.picmg.org/v2internal/specifications2.cfm?thetype=One&thebusid=3
Com Express Carrier Design Guide	http://picmg.org//wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	http://www.vesa.org
DP, eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml http://www.ti.com/lit/ml/snla187/snla187.pdf
MMC/eMMC	http://www.jedec.org/committees/jc-649
OpenGL	http://www.opengl.org
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
TMDS	http://www.siliconimage.com/technologies/tmds
UEFI	http://www.uefi.org

USB 2.0	http://www.usb.org/developers/docs/usb_20_070113.zip
USB 3.0	http://www.usb.org/developers/docs/usb_30_spec_070113.zip
xHCI	http://www.intel.com/content/www/us/en/io/universal-serial-bus/extensible-host-controler-interface-usb-xhci.html
Intel® Bay trail family	http://ark.intel.com/products/codename/55844/Bay-Trail#@Embedded

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

The COMe-A41-CT6 is a COM Express® Type 6, basic Form Factor, based on the Intel® family of System-on-Chips (SOCs) formerly coded as Bay Trail, a series of Single/ Dual / Quad SOCs with 64-bit instruction set.

These SOCs embed all the features usually obtained by combination of CPU + platform Controller hubs, all in one single IC, which allows, therefore, the system minimisation and performance optimisation. A complete list of SOCs available is detailed in the next chapter.

All the supported SOCs offer a 64-bit Instruction set, and provide direct access to the memory, which is available on two SODIMM DDR3L memory modules. Frequencies up to 1333MHz are supported, with a maximum capacity up to 8GB. Please notice that total amount of memory available is OS dependant, and depends also on the SOC.

All SOCs integrate an Intel® HD Graphics 400 Series Controller, which offer high graphical performances, with support for Microsoft® DirectX11, OpenGL 3.0, OpenCL 1.2, OpenGLES 2.0 and HW acceleration for video decoding of H.264, MPEG2, MVG, VC-1, VP8 and MJPEG video standards (for H.264, MPEG2 and MVG also HW encoding is offered).

This embedded GPU is able to drive two independent displays and makes available two Digital Display Interfaces: one of them is carried out directly on connector CD, and can be used to drive external Display Port, HDMI or DVI displays; the second interface is carried to an internal switch, which is driven via BIOS. By moving this switch, it is possible to carry out he second Digital Display Interface directly to connector CD, like the previous one, or to the connector AB to manage external embedded Display Port displays. It is also possible to use it this Digital Display Interface to drive an eDP-to-LVDS bridge, which will make available the LVDS interface. Please be aware that selection between eDP or LVDS is a factory option, while it is always possible to switch the Digital Display interface between the connector CD and AB (where will be available as eDP or LVDS). An additional CRT interface represents another video output offered by the CPU.

The module is completed with HD Audio Interface, up to 4 x PCI Express ports (one of them can be optionally used, as a factory option, to manage a Gigabit Ethernet controller), 2 x external Serial ATA channels, one optional eMMC disk soldered on board, 7 USB 2.0 ports, 4 USB 3.0 ports, Real Time Clock, LPC and SM Bus. Please refer to following chapter for a complete list of all peripherals integrated and characteristics.

The product is COM Express® Rel.2.1 standard compliant, an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available. Specifically, COMe-A41-CT6 is a COM Express® module, Compact Form factor, Type 6 (95mm x 95mm).

COM Express® module integrates all the core components and has to be mounted onto an application-specific carrier board; carrier board designers can utilise as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration. Most important, COM Express® modules are scalable, which means that once an application has been created there is the ability to diversify the product range through the use of different performance class or form factor size modules. Simply unplug one module and replace it with another, no redesign is necessary. The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

SOC

Intel® Atom™ E3845, Quad Core @1.91GHz, 2MB Cache, 10W TDP
Intel® Atom™ E3827, Dual Core @1.75GHz, 1MB Cache, 8W TDP
Intel® Atom™ E3826, Dual Core @1.46GHz, 1MB Cache, 7W TDP
Intel® Atom™ E3825, Dual Core @1.33GHz, 1MB Cache, 6W TDP
Intel® Atom™ E3815, Single Core @1.46GHz, 512KB Cache, 5W TDP
Intel® Celeron® J1900, Quad Core @2.0GHz, 2MB Cache, 10W TDP
Intel® Celeron® N2930, Quad Core @1.83GHz, 2MB Cache, 7.5W TDP
Intel® Celeron® N2807, Dual Core @1.58GHz, 1MB Cache, 4.3W TDP

Memory

DDRL non-ECC SO-DIMM slots, 4GB modules supported per each slot
E3845, E3827, J1900, N2930: up to 8GB Dual-Channel DDR3L 1333MHz
E3826: up to 8GB Dual-Channel DDR3L 1066MHz
N2807: up to 4GB Single-Channel DDR3L 1333MHz
E3825, E3815: up to 4GB Single-Channel DDR3L 1066MHz

Graphics

Integrated Intel® HD Graphics 4000 series controller
Dual independent display support
HW decoding of H.264, MPEG2, MVC, VC1, VP8, MJPEG formats
HW encoding of H.264, MPEG2 and MVC formats

Video Interfaces

1 x Digital Display Interface (DDI) able to drive HDMI / DVI / DP++ interface
Additional switched DDI, can be switched to manage embedded Display Port **or**
18/24 bit single/dual channel LVDS interface
CRT interface

Video Resolutions

CRT Interface:	up to 2560 x 1600 @ 60Hz
HDMI:	Up to 1920x1080p@60Hz
Display Port, eDP:	Up to 2560x1600@60Hz
Optional LVDS interface:	Up to 1920x1200@60Hz

Mass Storage

Optional eMMC disk soldered on board
2 x external S-ATA channels
SD Card interface (multiplexed with GPIO signals)

USB

7 x USB 2.0 Host Ports
4 x USB 3.0 Host ports

Networking

Optional Gigabit Ethernet interface (uses one PCI-e lane)

Audio

HD Audio interface

PCI Express

Up to 4 x PCI-e x1 Gen2 lanes

Serial Ports

2 x Serial port (TX/RX only, TTL interface)

Other Interfaces

2 x Express Card interfaces
I2C bus
LPC Bus
SM Bus
4 x GPI, 4 x GPO
Thermal / FAN management
Watch Dog timer
Power Management Signals

Power supply voltage: +12V_{DC} ± 10% and + 5V_{SB} (optional)

Operating temperature: 0°C ÷ +60°C (commercial version) **
-40°C ÷ +85°C (industrial version) **

Dimensions: 95 x 95 mm (3.74" x 3.74")

! *** Temperatures indicated are the minimum and maximum temperature that the heatspreader / heatsink can reach in any of its parts. This means that it is customer's responsibility to use any passive cooling solution along with an application-dependent cooling system, capable to ensure that the heatspreader / heatsink temperature remains in the range above indicated. Please also check paragraph 5.1*

2.3 Electrical Specifications

According to COM Express® specifications, the COMe-A41-CT6 board needs to be supplied only with an external +12V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through COM Express Connectors CN5 and CN6.

All remaining voltages needed for board's working are generated internally from +12V_{DC} power rail.

2.3.1 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_S: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_S, +5V_S.

_A: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_A, +3.3V_A.

_U: unswitched ACPI S3 voltages, i.e. power rails that are active both in ACPI's S0 (Working) and S3 (Standby) state. Examples: +1.5V_U.

2.3.2 Power Consumption

TBM

2.4 Mechanical Specifications

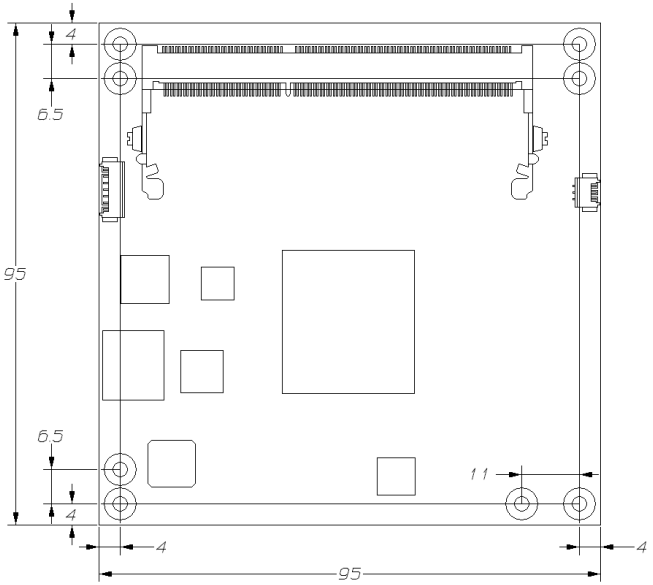
The COMe-A41-CT6 is a COM Express board, Compact Form Factor type; therefore its dimensions are 95 mm x 95 mm (3.74” x 3.74”).

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

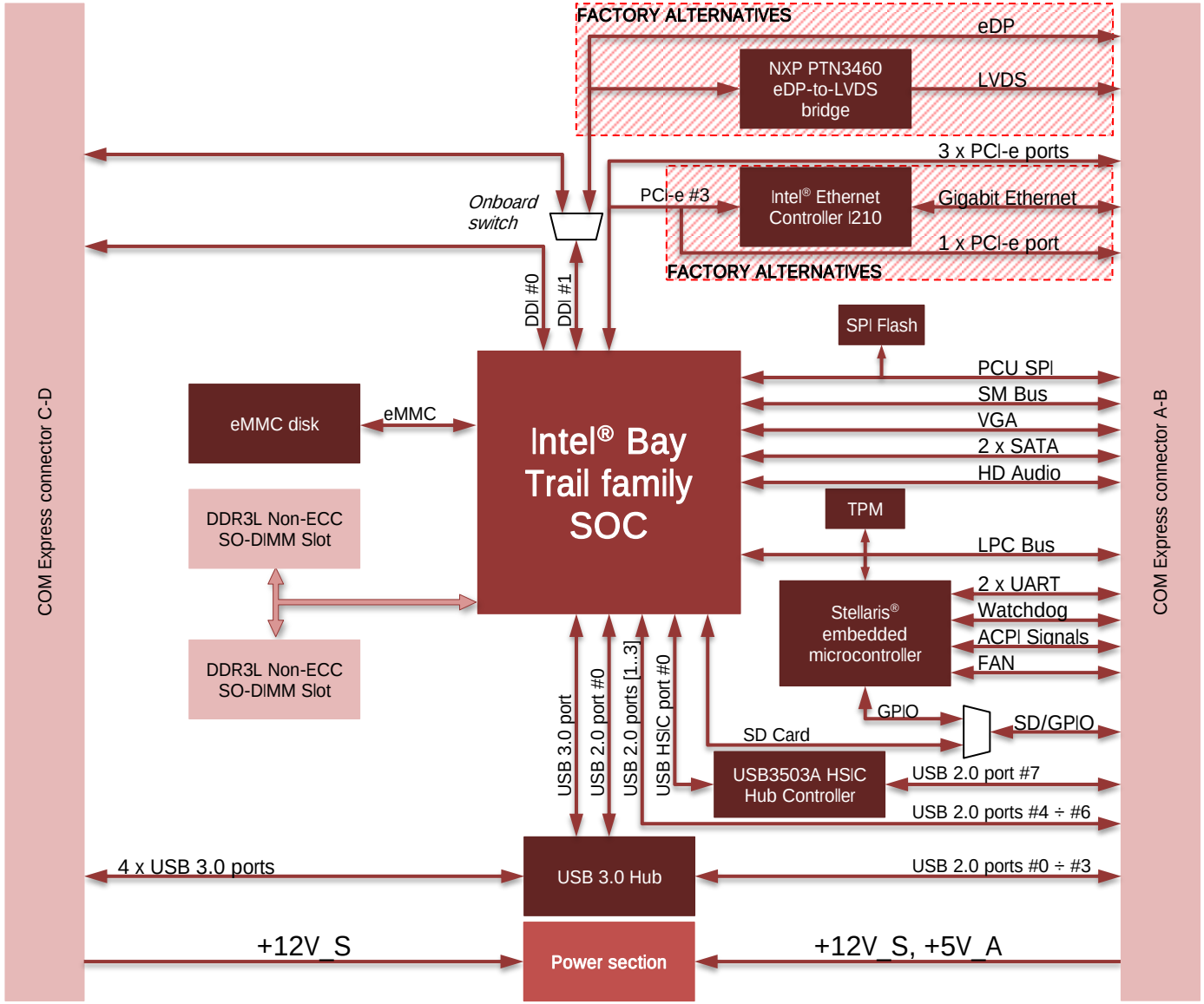
According to COM Express specifications, the carrier board plug can be of two different heights, 5mm and 8mm.

Whichever connector’s height is chosen, in designing a custom carrier board please remember that, according to COM Express® specifications, components placed on bottom side of COMe-A41-CT6 will have a maximum height of 3.8mm.

This value must be kept in high consideration when choosing the carrier board plugs’ height, if it is necessary to place components on the carrier board in the zone under the COM Express® module.



2.5 Block Diagram



Chapter 3.
CONNECTORS

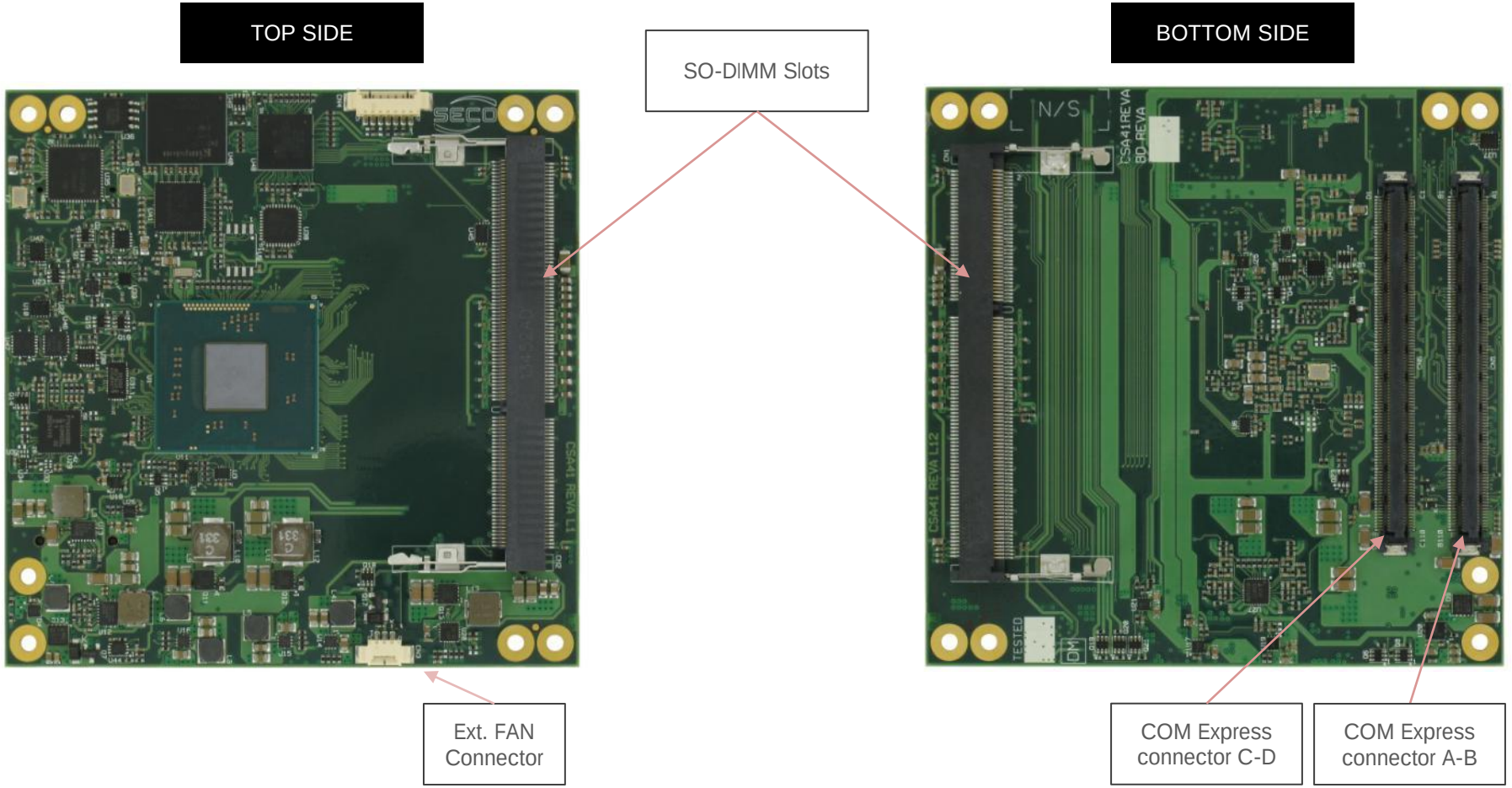
- Introduction
- Connectors description

3.1 Introduction

According to COM Express® specifications, all interfaces to the board are available through two 220 pin connectors, for a total of 440 pin. Simplifying the terminology in this documentation, the primary connector is called A-B and the secondary C-D, since each one consists of two rows.

In addition, a Fan connector has been placed on one side of the board, in order to allow an easier connection of active heatsinks to the module.

! Please be aware that, depending on the configuration purchased, the appearance of the board could be different from the following pictures.

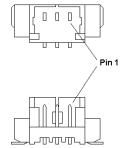


3.2 Connectors description

3.2.1 FAN Connector

FAN Connector - CN3	
Pin	**Signal**
1	GND
2	FAN_POWER
3	FAN_TACHO_IN

Depending on the usage model of COMe-A41-CT6 module, for critical applications/environments on the module itself it is available a 3-pin dedicated connector for an external +12V_{DC} FAN.



FAN Connector is a 3-pin single line SMT connector, type MOLEX 53261-0319 or equivalent, with pinout shown in the table on the left.

Mating connector: MOLEX 51021-0300 receptacle with MOLEX 50079-8000 female crimp terminals.

Please be aware that the use of an external fan depends strongly on customer's application/installation.

Please refer to chapter 5.1 for considerations about thermal dissipation.

FAN_POWER: +12V_S derived power rail for FAN, managed by the embedded microcontroller via PWM signal.

FAN_TACHO_IN: tachometric input from the fan to the embedded microcontroller, +3.3V_S electrical level signal.

3.2.2 SO-DIMM DDR3 Slots

CPUs used on the COMe-A41-CT6 board provide support to DDR3L memories, which can be integrated by using the dedicated DDR3L SO-DIMM sockets.

Please be aware that E3845, E3827, J1900, N2930 and N2807 SOCs support 1333MHz DDRL modules, while E3826, E3825 and E3815 SOCs support only 1066MHz modules.

For use of this memories, on board there are two SO-DIMM DDR3 sockets.

The socket placed on top side (CN2) is type Tyco 2013290-1 or equivalent, a right angle, low profile, reverse type socket, used for high speed system memory applications. This socket is available only with SOCs able to support dual channel memories (i.e., E3845, E3827, E3826, J1900, N2930).

The socket placed on bottom side (CN1) is type Tyco 2013022-1 or equivalent, and is a socket with performances similar to the other, only it is standard type, not reverse. The two sockets together allow the insertion of up to 2 SO-DIMM modules, for support to dual channel memories.

3.2.3 COM Express® Module connectors

For the connection of COM Express® CPU modules, on board there is one double connector, type TYCO 3-1827231-6 (440 pin, ultra thin, 0.5mm pitch, h=4mm), as requested by COM Express® specifications.

The pinout of the module is compliant to COM Express® Type 6 specifications. Not all the signals contemplated in COM Express® standard are implemented on the double connector, due to the functionalities really implemented on COMe-A41-CT6 board. Therefore, please refer to the following table for a list of effective signals reported on the connector. For accurate signals description, please consult the following paragraphs.

COM Express® Connector AB - CN5							
		ROW A			ROW B		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	A1	B1	GND	PWR	
GBE	I/O	GBE0_MDI3-	A2	B2	GBE0_ACT#	O	GBE
GBE	I/O	GBE0_MDI3+	A3	B3	LPC_FRAME#	O	LPC
GBE	O	GBE0_LINK100#	A4	B4	LPC_AD0	I/O	LPC
GBE	O	GBE0_LINK1000#	A5	B5	LPC_AD1	I/O	LPC
GBE	I/O	GBE0_MDI2-	A6	B6	LPC_AD2	I/O	LPC
GBE	I/O	GBE0_MDI2+	A7	B7	LPC_AD3	I/O	LPC
GBE	O	GBE0_LINK#	A8	B8	N.C.	N.A.	
GBE	I/O	GBE0_MDI1-	A9	B9	N.C.	N.A.	
GBE	I/O	GBE0_MDI1+	A10	B10	LPC_CLK	O	LPC
	PWR	GND	A11	B11	GND	PWR	
GBE	I/O	GBE0_MDI0-	A12	B12	PWRBTN#	I	PWR_MGMT
GBE	I/O	GBE0_MDI0+	A13	B13	SMB_CK	I/O	SMBUS
	N.A.	N.C.	A14	B14	SMB_DAT	I/O	SMBUS
PWR_MGMT	O	SUS_S3#	A15	B15	SMB_ALERT#	I	SMBUS
SATA	O	SATA0_TX+	A16	B16	SATA1_TX+	O	SATA
SATA	O	SATA0_TX-	A17	B17	SATA1_TX-	O	SATA
PWR_MGMT	O	SUS_S4#	A18	B18	SUS_STAT#	O	PWR_MGMT
SATA	I	SATA0_RX+	A19	B19	SATA1_RX+	I	SATA
SATA	I	SATA0_RX-	A20	B20	SATA1_RX-	I	SATA

	PWR	GND	A21	B21	GND	PWR	
	N.A.	N.C.	A22	B22	N.C.	N.A.	
	N.A.	N.C.	A23	B23	N.C.	N.A.	
PWR_MGMT	O	SUS_S5#	A24	B24	PWR_OK	I	PWR_MGMT
	N.A.	N.C.	A25	B25	N.C.	N.A.	
	N.A.	N.C.	A26	B26	N.C.	N.A.	
PWR_MGMT	I	BATLOW#	A27	B27	WDT	O	MISC
SATA	O	SATA_ACT#	A28	B28	N.C.	N.A.	
AUDIO	O	HDA_SYNC	A29	B29	HDA_SDIN1	I/O	AUDIO
AUDIO	O	HDA_RST#	A30	B30	HDA_SDIN0	I/O	AUDIO
	PWR	GND	A31	B31	GND	PWR	
AUDIO	I/O	HDA_BITCLK	A32	B32	SPKR	O	MISC
AUDIO	O	HDA_SDOUT	A33	B33	I2C_CK	I/O	I2C
	N.A.	N.C.	A34	B34	I2C_DAT	I/O	I2C
MISC	O	THRMTRIP#	A35	B35	THRM#	I	MISC
USB	I/O	USB6-	A36	B36	USB7-	I/O	USB
USB	I/O	USB6+	A37	B37	USB7+	I/O	USB
USB	I	USB_6_7_OC#	A38	B38	USB_4_5_OC#	I	USB
USB	I/O	USB4-	A39	B39	USB5-	I/O	USB
USB	I/O	USB4+	A40	B40	USB5+	I/O	USB
	PWR	GND	A41	B41	GND	PWR	
USB	I/O	USB2-	A42	B42	USB3-	I/O	USB
USB	I/O	USB2+	A43	B43	USB3+	I/O	USB
USB	I	USB_2_3_OC#	A44	B44	USB_0_1_OC#	I	USB
USB	I/O	USB_0-	A45	B45	USB1-	I/O	USB
USB	I/O	USB_0+	A46	B46	USB1+	I/O	USB
	PWR	VCC_RTC	A47	B47	EXCD1_PERST#	O	EXCD
EXCD	O	EXCD0_PERST#	A48	B48	EXCD1_CPPE#	I	EXCD
EXCD	I	EXCD0_CPPE#	A49	B49	SYS_RESET#	I	PWR_MGMT
LPC	I/O	LPC_SERIRQ	A50	B50	CB_RESET#	O	PWR_MGMT

	PWR	GND	A51	B51	GND	PWR	
	N.A.	N.C.	A52	B52	N.C.	N.A.	
	N.A.	N.C.	A53	B53	N.C.	N.A.	
GPIO / SD	I/O	GPI0	A54	B54	GPO1	O	GPIO / SD
	N.A.	N.C.	A55	B55	N.C.	N.A.	
	N.A.	N.C.	A56	B56	N.C.	N.A.	
	PWR	GND	A57	B57	GPO2	I/O	GPIO / SD
PCIE	O	PCIE_TX3+	A58	B58	PCIE_RX3+	I	PCIE
PCIE	O	PCIE_TX3-	A59	B59	PCIE_RX3-	I	PCIE
	PWR	GND	A60	B60	GND	PWR	
PCIE	O	PCIE_TX2+	A61	B61	PCIE_RX2+	I	PCIE
PCIE	O	PCIE_TX2-	A62	B62	PCIE_RX2-	I	PCIE
GPIO / SD	I/O	GPI1	A63	B63	GPO3	I/O	GPIO / SD
PCIE	O	PCIE_TX1+	A64	B64	PCIE_RX1+	I	PCIE
PCIE	O	PCIE_TX1-	A65	B65	PCIE_RX1-	I	PCIE
	PWR	GND	A66	B66	WAKE0#	I	PWR_MGMT
GPIO / SD	I/O	GPI2	A67	B67	WAKE1#	I	PWR_MGMT
PCIE	O	PCIE_TX0+	A68	B68	PCIE_RX0+	I	PCIE
PCIE	O	PCIE_TX0-	A69	B69	PCIE_RX0-	I	PCIE
	PWR	GND	A70	B70	GND	PWR	
LVDS	O	LVDS_A0+	A71	B71	LVDS_B0+	O	LVDS
LVDS	O	LVDS_A0-	A72	B72	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP_TX1+/LVDS_A1+	A73	B73	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP_TX1-/LVDS_A1-	A74	B74	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP_TX0+/LVDS_A2+	A75	B75	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP_TX0-/LVDS_A2-	A76	B76	LVDS_B2-	O	LVDS
eDP/LVDS	O	eDP/LVDS_VDD_EN	A77	B77	LVDS_B3+	O	LVDS
LVDS	O	LVDS_A3+	A78	B78	LVDS_B3-	O	LVDS
LVDS	O	LVDS_A3-	A79	B79	eDP/LVDS_BKLT_EN	O	eDP/LVDS
	PWR	GND	A80	B80	GND	PWR	

LVDS	O	LVDS_A_CK+	A81	B81	LVDS_B_CK+	O	LVDS
LVDS	O	LVDS_A_CK-	A82	B82	LVDS_B_CK-	O	LVDS
eDP/LVDS	I/O	eDP_AUX+/LVDS_I2C_CK	A83	B83	eDP/LVDS_BKLT_CTRL	O	LVDS
eDP/LVDS	I/O	eDP_AUX-/LVDS_I2C_DAT	A84	B84	+5V_A	PWR	
GPIO / SD	I/O	GPI3	A85	B85	+5V_A	PWR	
	N.A.	N.C.	A86	B86	+5V_A	PWR	
eDP	I	eDP_HPD	A87	B87	+5V_A	PWR	
PCIE	O	PCIE_CLK_REF+	A88	B88	N.C.	N.A.	
PCIE	O	PCIE_CLK_REF-	A89	B89	VGA_RED	O	VGA
	PWR	GND	A90	B90	GND	PWR	
SPI	O	SPI_POWER	A91	B91	VGA_GRN	O	VGA
	N.A.	N.C.	A92	B92	VGA_BLU	O	VGA
GPIO / SD	O	GPO0	A93	B93	VGA_HSYNC	O	VGA
	N.A.	N.C.	A94	B94	VGA_VSYNC	O	VGA
	N.A.	N.C.	A95	B95	VGA_I2C_CK	I/O	VGA
MISC	I	TPM_PP	A96	B96	VGA_I2C_DAT	I/O	VGA
TYPE	N.A.	TYPE10#: N.C.	A97	B97	N.C.	N.A.	
UART	O	SER0_TX	A98	B98	N.C.	N.A.	
UART	I	SER0_RX	A99	B99	N.C.	N.A.	
	PWR	GND	A100	B100	GND	PWR	
UART	O	SER1_TX	A101	B101	FAN_PWNOUT	O	MISC
UART	I	SER1_RX	A102	B102	FAN_TACHIN	I	MISC
PWR_MGMT	I	LID#	A103	B103	SLEEP#	I	PWR_MGMT
	PWR	+12V_S	A104	B104	+12V_S	PWR	
	PWR	+12V_S	A105	B105	+12V_S	PWR	
	PWR	+12V_S	A106	B106	+12V_S	PWR	
	PWR	+12V_S	A107	B107	+12V_S	PWR	
	PWR	+12V_S	A108	B108	+12V_S	PWR	
	PWR	+12V_S	A109	B109	+12V_S	PWR	
	PWR	GND	A110	B110	GND	PWR	

COM Express® Connector CD - CN6							
		ROW C			ROW D		
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	C1	D1	GND	PWR	
	PWR	GND	C2	D2	GND	PWR	
USB	I	USB_SSRX0-	C3	D3	USB_SSTX0-	O	USB
USB	I	USB_SSRX0+	C4	D4	USB_SSTX0+	O	USB
	PWR	GND	C5	D5	GND	PWR	
USB	I	USB_SSRX1-	C6	D6	USB_SSTX1-	O	USB
USB	I	USB_SSRX1+	C7	D7	USB_SSTX1+	O	USB
	PWR	GND	C8	D8	GND	PWR	
USB	I	USB_SSRX2-	C9	D9	USB_SSTX2-	O	USB
USB	I	USB_SSRX2+	C10	D10	USB_SSTX2+	O	USB
	PWR	GND	C11	D11	GND	PWR	
USB	I	USB_SSRX3-	C12	D12	USB_SSTX3-	O	USB
USB	I	USB_SSRX3+	C13	D13	USB_SSTX3+	O	USB
	PWR	GND	C14	D14	GND	PWR	
	N.A.	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	I/O	DDI
	N.A.	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	I/O	DDI
	N.A.	N.C.	C17	D17	N.C.	N.A.	
	N.A.	N.C.	C18	D18	N.C.	N.A.	
	N.A.	N.C.	C19	D19	N.C.	N.A.	
	N.A.	N.C.	C20	D20	N.C.	N.A.	
	PWR	GND	C21	D21	GND	PWR	
	N.A.	N.C.	C22	D22	N.C.	N.A.	
	N.A.	N.C.	C23	D23	N.C.	N.A.	
DDI	I	DDI1_HPD	C24	D24	N.C.	N.A.	
	N.A.	N.C.	C25	D25	N.C.	N.A.	
	N.A.	N.C.	C26	D26	DDI1_PAIR0+	O	DDI

	N.A.	N.C.	C27	D27	DDI1_PAIR0-	O	DDI
	N.A.	N.C.	C28	D28	N.C.	N.A.	
	N.A.	N.C.	C29	D29	DDI1_PAIR1+	O	DDI
	N.A.	N.C.	C30	D30	DDI1_PAIR1-	O	DDI
	PWR	GND	C31	D31	GND	PWR	
DDI	I/O	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	O	DDI
DDI	I/O	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	O	DDI
DDI	I	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	I	DDI
	N.A.	N.C.	C35	D35	N.C.	N.A.	
	N.A.	N.C.	C36	D36	DDI1_PAIR3+	O	DDI
	N.A.	N.C.	C37	D37	DDI1_PAIR3-	O	DDI
	N.A.	N.C.	C38	D38	N.C.	N.A.	
	N.A.	N.C.	C39	D39	DDI2_PAIR0+	O	DDI
	N.A.	N.C.	C40	D40	DDI2_PAIR0-	O	DDI
	PWR	GND	C41	D41	GND	PWR	
	N.A.	N.C.	C42	D42	DDI2_PAIR1+	O	DDI
	N.A.	N.C.	C43	D43	DDI2_PAIR1-	O	DDI
	N.A.	N.C.	C44	D44	DDI2_HPD	I	DDI
	N.A.	N.C.	C45	D45	N.C.	N.A.	
	N.A.	N.C.	C46	D46	DDI2_PAIR2+	O	DDI
	N.A.	N.C.	C47	D47	DDI2_PAIR2-	O	DDI
	N.A.	N.C.	C48	D48	N.C.	N.A.	
	N.A.	N.C.	C49	D49	DDI2_PAIR3+	O	DDI
	N.A.	N.C.	C50	D50	DDI2_PAIR3-	O	DDI
	PWR	GND	C51	D51	GND	PWR	
	N.A.	N.C.	C52	D52	N.C.	N.A.	
	N.A.	N.C.	C53	D53	N.C.	N.A.	
TYPE	N.A.	TYPE0#: N.C.	C54	D54	N.C.	N.A.	
	N.A.	N.C.	C55	D55	N.C.	N.A.	
	N.A.	N.C.	C56	D56	N.C.	N.A.	

TYPE	N.A.	TYPE1#: N.C.	C57	D57	TYPE2#: GND	N.A.	TYPE
	N.A.	N.C.	C58	D58	N.C.	N.A.	
	N.A.	N.C.	C59	D59	N.C.	N.A.	
	PWR	GND	C60	D60	GND	PWR	
	N.A.	N.C.	C61	D61	N.C.	N.A.	
	N.A.	N.C.	C62	D62	N.C.	N.A.	
	N.A.	N.C.	C63	D63	N.C.	N.A.	
	N.A.	N.C.	C64	D64	N.C.	N.A.	
	N.A.	N.C.	C65	D65	N.C.	N.A.	
	N.A.	N.C.	C66	D66	N.C.	N.A.	
	N.A.	N.C.	C67	D67	GND	PWR	
	N.A.	N.C.	C68	D68	N.C.	N.A.	
	N.A.	N.C.	C69	D69	N.C.	N.A.	
	PWR	GND	C70	D70	GND	PWR	
	N.A.	N.C.	C71	D71	N.C.	N.A.	
	N.A.	N.C.	C72	D72	N.C.	N.A.	
	PWR	GND	C73	D73	GND	PWR	
	N.A.	N.C.	C74	D74	N.C.	N.A.	
	N.A.	N.C.	C75	D75	N.C.	N.A.	
	PWR	GND	C76	D76	GND	PWR	
	N.A.	N.C.	C77	D77	N.C.	N.A.	
	N.A.	N.C.	C78	D78	N.C.	N.A.	
	N.A.	N.C.	C79	D79	N.C.	N.A.	
	PWR	GND	C80	D80	GND	PWR	
	N.A.	N.C.	C81	D81	N.C.	N.A.	
	N.A.	N.C.	C82	D82	N.C.	N.A.	
	N.A.	N.C.	C83	D83	N.C.	N.A.	
	PWR	GND	C84	D84	GND	PWR	
	N.A.	N.C.	C85	D85	N.C.	N.A.	
	N.A.	N.C.	C86	D86	N.C.	N.A.	

PWR	GND	C87	D87	GND	PWR
N.A.	N.C.	C88	D88	N.C.	N.A.
N.A.	N.C.	C89	D89	N.C.	N.A.
PWR	GND	C90	D90	GND	PWR
N.A.	N.C.	C91	D91	N.C.	N.A.
N.A.	N.C.	C92	D92	N.C.	N.A.
PWR	GND	C93	D93	GND	PWR
N.A.	N.C.	C94	D94	N.C.	N.A.
N.A.	N.C.	C95	D95	N.C.	N.A.
PWR	GND	C96	D96	GND	PWR
N.A.	N.C.	C97	D97	N.C.	N.A.
N.A.	N.C.	C98	D98	N.C.	N.A.
N.A.	N.C.	C99	D99	N.C.	N.A.
PWR	GND	C100	D100	GND	PWR
N.A.	N.C.	C101	D101	N.C.	N.A.
N.A.	N.C.	C102	D102	N.C.	N.A.
PWR	GND	C103	D103	GND	PWR
PWR	+12V_S	C104	D104	+12V_S	PWR
PWR	+12V_S	C105	D105	+12V_S	PWR
PWR	+12V_S	C106	D106	+12V_S	PWR
PWR	+12V_S	C107	D107	+12V_S	PWR
PWR	+12V_S	C108	D108	+12V_S	PWR
PWR	+12V_S	C109	D109	+12V_S	PWR
PWR	GND	C110	D110	GND	PWR

3.2.3.1 Audio interface signals

The COMe-A41-CT6 module supports HD audio format, thanks to native support offered by the processor to this audio codec standard. Up to 2 HD audio codecs on the carrier board can be supported.

Here following the signals related to HD Audio interface:

HDA_SYNC: HD Audio Serial Bus Synchronization. 48kHz fixed rate output from the module to the Carrier board, electrical level +3.3V_S.

HDA_RST#: HD Audio Codec Reset. Active low signal, output from the module to the Carrier board, electrical level +3.3V_S.

HDA_BITCLK: HD Audio Serial Bit Clock signal. 24MHz serial data clock generated by the Intel HD audio controller, output from the module to the Carrier board, electrical level +3.3V_S.

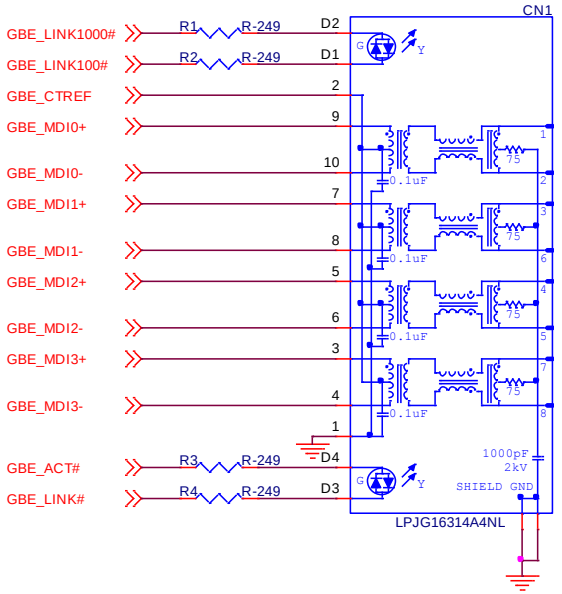
HDA_SDOUT: HD Audio Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_S.

HDA_SDIN[0..1]: HD Audio Serial Data In signal. Inputs to the module from the Codec(s) placed on the Carrier board, electrical level +3.3V_S.

The first four signals have to be connected to all the HD Audio codecs present on the carrier board. For each Codec, only one HDA_SDIN signal must be used. Please refer to the chosen Codecs' Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.3.2 Gigabit Ethernet signals

The Gigabit Ethernet interface is optional, and is realised, on COMe-A41-CT6 module, using an Intel® I210 Gigabit Ethernet controller, which is interfaced to the SOC through PCI-express lane #3.



Here following the signals involved in Gigabit Ethernet management

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE0_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_A.

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_A.

These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic on the left as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. Intel® I210 Gigabit Ethernet controller, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on COM Express® connector AB.

All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.r.l. for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.3.3 S-ATA signals

The Intel® Bay Trail family of SOCs offer two S-ATA interfaces. All of them are carried out on COM Express® connector AB.

SATA ports are Gen2 compliant, therefore support 1.5 Gbps and 3.0 Gbps data rates.

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA_ACT#: Serial ATA Activity Led. Active low output signal at +3.3V_S voltage.

10nF AC series decoupling capacitors are placed on each line of SATA differential pairs.

On the carrier board, these signals can be carried out directly to the SATA connectors.

3.2.3.4 PCI Express interface signals

COMe-A41-CT6 can offer externally up to four PCI Express lane, which are directly managed by the Intel® Bay Trail SOC.

PCI express Gen 2.0 (5Gbps) is supported.

> **!** Please be aware that PCI Express lane #3 is available as a factory option, alternative to the Gigabit Ethernet interface (i.e., the module purchased will have PCI Express Lane #3 available OR Gigabit Ethernet Interface, both of them is not possible).

Here following the signals involved in PCI express management.

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair.

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE1_TX+/PCIE1_TX-: PCI Express lane #1, Transmitting Output Differential pair

PCIE1_RX+/PCIE1_RX-: PCI Express lane #1, Receiving Input Differential pair

PCIE2_TX+/PCIE2_TX-: PCI Express lane #2, Transmitting Output Differential pair

PCIE2_RX+/PCIE2_RX-: PCI Express lane #2, Receiving Input Differential pair

PCIE3_TX+/PCIE3_TX-: PCI Express lane #3, Transmitting Output Differential pair

PCIE3_RX+/PCIE3_RX-: PCI Express lane #3, Receiving Input Differential pair

PCIE_CLK_REF+/ PCIE_CLK_REF-: PCI Express 100MHz Reference Clock, Differential Pair. Please consider that only one reference clock is supplied, while there are many different PCI express lanes and one PEG. When more than one PCI Express lane is used on the carrier board, then a zero-delay buffer must be used to replicate the reference clock to all the devices.

3.2.3.5 Express Card interface signals

According to Com Express® specifications, the COMe-A41-CT6 module offers the signals necessary for management of up to two Express Cards, managed by the module's embedded microcontroller.

The signals involved in Express Card management are the following.

EXCD0_CPPE#: PCI Express Capable Card slot #0 Request, +3.3V_S Active Low input signal with 10kΩ pull-up resistor.

EXCD0_PERST#: Express Card slot#0 reset, +3.3V_S Active Low output signal.

EXCD1_CPPE#: PCI Express Capable Card slot #1 Request, +3.3V_S Active Low input signal with 10kΩ pull-up resistor.

EXCD1_PERST#: Express Card slot #1 reset, +3.3V_S Active Low output signal.

3.2.3.6 USB interface signals

Intel® Bay trail family of SOCs embed both one xHCI and one EHCI controllers, which are able to manage one Superspeed ports (i.e. USB 3.0 compliant), up to four USB 1.x / 2.0 Host ports and up to two HSIC USB ports. On COMe-A41-CT6 module there is one USB 3.0 Hub that, interfaced to USB 2.0 port #0 and to the native USB 3.0 (SuperSpeed) port, makes available four USB 2.0 and four USB 3.0 ports.

Moreover, an HSIC USB Hub converts one of the HSIC ports to USB 2.0, so that there will be a total of 8 USB 2.0 ports.

Via BIOS settings it is possible to enable or disable the xHCI controller, therefore enabling USB 3.0 and HSIC functionalities or leaving only USB 1.1 and USB 2.0 support. All USB 2.0 ports are able to work in High Speed (HS), Full Speed (FS) and Low Speed (LS).

Here following the signals related to USB interfaces.

USB_0+/USB_0-: Universal Serial Bus Port #0 bidirectional differential pair.

USB_1+/USB_1-: Universal Serial Bus Port #1 bidirectional differential pair.

USB_2+/USB_2-: Universal Serial Bus Port #2 bidirectional differential pair.

USB_3+/USB_3-: Universal Serial Bus Port #3 bidirectional differential pair.

USB_4+/USB_4-: Universal Serial Bus Port #4 bidirectional differential pair.

USB_5+/USB_5-: Universal Serial Bus Port #5 bidirectional differential pair.

USB_6+/USB_6-: Universal Serial Bus Port #6 bidirectional differential pair.

USB_7+/USB_7-: Universal Serial Bus Port #7 bidirectional differential pair.

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair; it is managed by the xHCI controller only.

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair; it is managed by the xHCI controller only.

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair; it is managed by the xHCI controller only.

USB_0_1_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port#0 and #1 of COMe-A41-CT6 module

USB_2_3_OC#: USB Over Current Detect Input. Active Low Input signa.l, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Ports #2 and #3 of COMe-A41-CT6 module.

USB_4_5_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #4 and/or #5 of COMe-A41-CT6 module.

USB_6_7_OC#: USB Over Current Detect Input. Active Low Input signal, electrical level +3.3V_A with 10kΩ pull-up resistor. This pin has to be used for overcurrent detection of USB Port #6 and/or #7 of COMe-A41-CT6 module.

100nF AC series decoupling capacitors are placed on each receiving line of USB Super speed differential pairs.

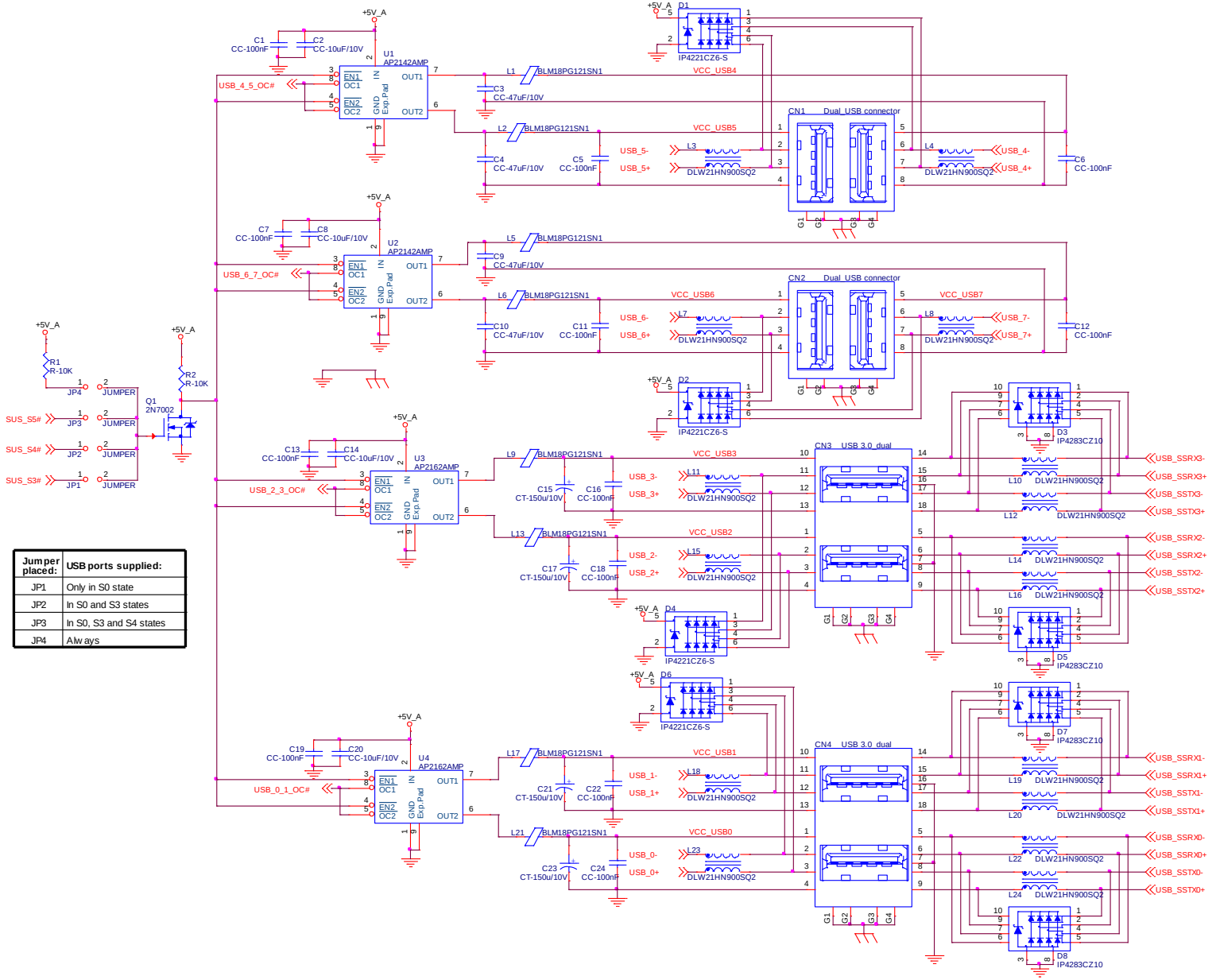
In the following table is shown the correspondence between USB ports available on COM Express connectors and internal USB ports managed by the Bay Trail SOCs. (see also paragraph 4.3.3).

Com Express USB Port number	Derived from
USB 2.0 #0	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 2.0 #1	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 2.0 #2	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 2.0 #3	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 2.0 #4	SOC's native USB 2.0 port #1
USB 2.0 #5	SOC's native USB 2.0 port #2
USB 2.0 #6	SOC's native USB 2.0 port #3
USB 2.0 #7	USB HSIC USB Controller on SOC's HSIC port #0
USB 3.0 #0	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 3.0 #1	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 3.0 #2	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0
USB 3.0 #3	USB 3.0 HUB on SOC's Superspeed port and USB 2.0 port #0

Please notice that for correct management of Overcurrent signals, power distribution switches are needed on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

The schematics in the following page show an example of implementation on the Carrier Board. In there, USB ports #4, #5, #6 and #7 are carried out to standard USB 2.0 Type A receptacles, while USB 2.0 port #0, #1, #2 and 3 along with the corresponding Superspeed USB ports, are carried to standard USB 3.0 Type A receptacles. Always remember that, for correct implementation of USB 3.0 connections, any Superspeed port must be paired with corresponding number of USB 2.0 port (i.e. USB 2.0 port#0 must be paired with USB 3.0 port #0 and so on).



Jumper placed:	USB ports supplied:
JP1	Only in S0 state
JP2	In S0 and S3 states
JP3	In S0, S3 and S4 states
JP4	Always

3.2.3.7 LVDS Flat Panel signals

The Intel® Bay Trail family of SOCs offer only two Digital Display Interfaces for the video, and doesn't offer the support for LVDS interface, which is conversely much used in many application fields, as well as embedded Display Port.

For this reason, on COMe-A41-CT6 there is a Display Port switch, driven via BIOS, that allows redirecting the Digital Display Interface to the embedded Display Port/LVDS interface pins on connector AB instead of on the pins on connector CD reserved for Digital Display Interface.

As a factory option, it is possible to choose if the board must be equipped with an eDP-to-LVDS bridge (NXP PTN3460), which allow the implementation of a Dual Channel LVDS, with a maximum supported resolution of 1920x1200 @ 60Hz (dual channel mode).

> **!** Please remember that LVDS interface is not native for Bay Trail family of SOCs, it is derived from an optional eDP-to-LVDS bridge. Depending on the factory option purchased, on the same pins it is available LVDS first channel **or** eDP interface.
>
> When placing an order of COMe-A41-CT6 modules, please take care of specifying if it is necessary LVDS interface or eDP.

Here following the signals related to LVDS management:

LVDS_A0+/LVDS_A0-: LVDS Channel #A differential data pair #0.

LVDS_A1+/LVDS_A1-: LVDS Channel #A differential data pair #1.

LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2.

LVDS_A3+/LVDS_A3-: LVDS Channel #A differential data pair #3.

LVDS_A_CLK+/LVDS_A_CLK-: LVDS Channel #A differential clock.

LVDS_B0+/LVDS_B0-: LVDS Channel #B differential data pair #0.

LVDS_B1+/LVDS_B1-: LVDS Channel #B differential data pair #1.

LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2.

LVDS_B3+/LVDS_B3-: LVDS Channel #B differential data pair #3.

LVDS_B_CLK+/LVDS_B_CLK-: LVDS Channel #B differential Clock

LVDS_VDD_EN: +3.3V_S electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected LVDS display.

LVDS_BKLT_EN: +3.3V_S electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected LVDS display.

LVDS_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

LVDS_I2C_DAT: DisplayID DDC Data line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

LVDS_I2C_CK: DisplayID DDC Clock line for LVDS flat Panel detection. Bidirectional signal, electrical level +3.3V_S with a 2k2Ω pull-up resistor.

3.2.3.8 Embedded Display Port (eDP) signals

As described in the previous paragraph, the Intel® Bay Trail family of SOCs offers only Digital Display Interfaces.

One of these two interfaces can be switched toward COM Express connector AB. When the board is not configured with the eDP-to-LVDS bridge, then the switched DDI interface supports eDP displays, which can have resolutions up to 1920 x 1200 @ 60Hz.

Here following the signals related to eDP management:

eDP_TX0+/eDP_TX0-: eDP channel differential data pair #0. AC coupled though 100nF ceramic capacitors on both lines.

eDP_TX1+/eDP_TX1-: eDP channel differential data pair #1. AC coupled though 100nF ceramic capacitors on both lines.

eDP_AUX+/eDP_AUX-: eDP channel differential auxiliary channel. AC coupled though 100nF ceramic capacitors on both lines.

eDP_HPD: eDP channel Hot Plug Detect. Active High Signal, +3.3V_S electrical level input.

eDP_VDD_EN: +3.3V_S electrical level output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

eDP_BKLT_EN: +3.3V_S electrical level output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

eDP_BKLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

3.2.3.9 LPC interface signals

According to COM Express® specifications rel. 2.0, on the on COM Express connector AB there are 8 pins that are used for implementation of Low Pin Count (LPC) Bus interface.

The following signals are available:

LPC_AD[0÷3]: LPC address, command and data bus, bidirectional signal, +3.3V_S electrical level.

LPC_CLK: LPC Clock Output line, +3.3V_S electrical level. Since only a clock line is available, if more LPC devices are available on the carrier board, then it is necessary to provide for a zero-delay clock buffer to connect all clock lines to the single clock output of COM Express module.

LPC_FRAME#: LPC Frame indicator, active low output line, +3.3V_S electrical level. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

LPC_SERIRQ: LPC Serialised IRQ request, bidirectional line, +3.3V_S electrical level. This signal is used only by peripherals requiring Interrupt support.

3.2.3.10 Analog VGA interface

The Intel® Bay trail family of SOCs offer one Analog display interface, which can be used for the connection of older VGA/CRT displays.

Signals dedicated to VGA interface are are the following:

VGA_RED: SOC's internal DAC's Red Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_GRN: SOC's internal DAC's Green Signal video output. A 150Ω pull-down resistor is placed on the line.

VGA_BLU: SOC's internal DAC's Blue Signal video output. A 150Ω pull-down resistor is placed on the line.

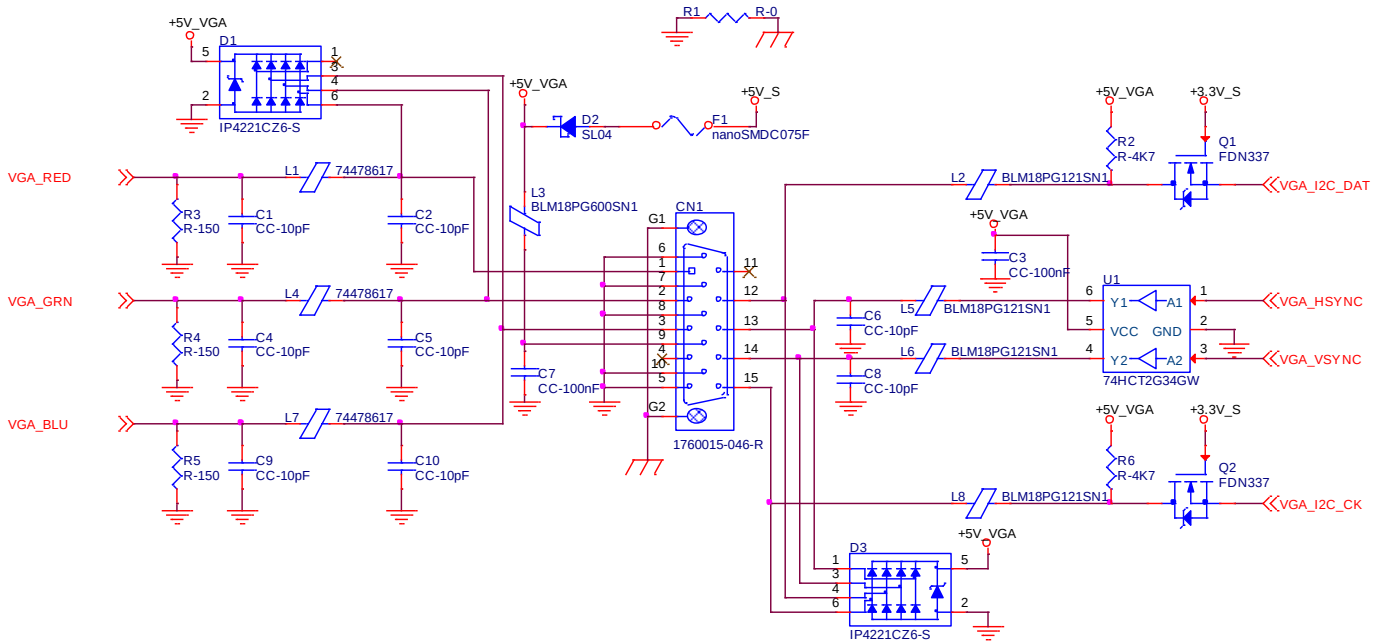
VGA_HSYNC: SOC's internal DAC's Horizontal Synchronization output signal.

VGA_VSYNC: SOC's internal DAC's DAC's Vertical Synchronization output signal.

VGA_I2C_CK: internal DAC's DDC Clock line for VGA displays detection. Output signal, electrical level +3.3V_S with 2K2Ω pull-up resistor.

VGA_I2C_DAT: internal DAC's DDC Clock line for VGA displays detection. Bidirectional signal, electrical level +3.3V_S with 2K2Ω pull-up resistor.

Please be aware that for the connection to external VGA displays, on the carrier board it is necessary to provide for filters and ESD protection like in the following example schematics.



3.2.3.11 Digital Display interfaces

The Intel® HD Graphics 4000 Series controllers, embedded inside the Intel® Bay Trail family of SOCs, offer two Digital Display interfaces, which can be used for the implementation, on the carrier board, of HDMI/DVI or Multimode Display Port interfaces.

Switching between HDMI/DVI (or, more correctly, TMDS) and Display Port is dynamic, i.e. the interfaces coming out from COM Express® module can be used to implement a multimode Display Port interface (and in this way only AC coupling capacitors are needed on the carrier board) or a HDMI/DVI interface (an in this case TMDS level shifters are needed).

This is reached by multiplexing DP/HDMI interfaces on the same pins.

Depending by the interface chosen, therefore, on COM Express connector CD there will be available the following signals:

Digital Display Interfaces - Pin multiplexing					
		Multimode Display Port mode		TMDS (HDMI/DVI) mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
D26	DDI1_PAIR0+	DP1_LANE0+	DP1 Differential pair #0 non-inverting line	TMDS1_DATA2+	TMDS1 Differential pair #2 non-inverting line
D27	DDI1_PAIR0-	DP1_LANE0-	DP1 Differential pair #0 inverting line	TMDS1_DATA2-	TMDS1 Differential pair #2 inverting line
D29	DDI1_PAIR1+	DP1_LANE1+	DP1 Differential pair #1 non-inverting line	TMDS1_DATA1+	TMDS1 Differential pair #1 non-inverting line
D30	DDI1_PAIR1-	DP1_LANE1-	DP1 Differential pair #1 inverting line	TMDS1_DATA1-	TMDS1 Differential pair #1 inverting line
D32	DDI1_PAIR2+	DP1_LANE2+	DP1 Differential pair #2 non-inverting line	TMDS1_DATA0+	TMDS1 Differential pair #0 non-inverting line
D33	DDI1_PAIR2-	DP1_LANE2-	DP1 Differential pair #2 inverting line	TMDS1_DATA0-	TMDS1 Differential pair #0 inverting line
D36	DDI1_PAIR3+	DP1_LANE3+	DP1 Differential pair #3 non-inverting line	TMDS1_CLK+	TMDS1 Differential clock non-inverting line
D37	DDI1_PAIR3-	DP1_LANE3-	DP1 Differential pair #3 inverting line	TMDS1_CLK-	TMDS1 Differential clock inverting line
C24	DDI1_HPD	DP1_HPD	DP1 Hot Plug Detect signal	HDMI1_HPD	HDMI #1 Hot Plug Detect signal
D15	DDI1_CTRLCLK_AUX+	DP1_AUX+	DP1 Auxiliary channel non-inverting line	HDMI1_CTRLCLK	DDC Clock line for HDMI panel #1.
D16	DDI1_CTRLDATA_AUX-	DP1_AUX-	DP1 Auxiliary channel inverting line	HDMI1_CTRLDATA	DDC Data line for HDMI panel #1.
D34	DDI1_DDC_AUX_SEL	DDI#1 DP or TMDS interface selector: pull this signal low or leave it floating for DP++ interface, pull high (+3.3V_S) for TMDS interface			
D39	DDI2_PAIR0+	DP2_LANE0+	DP2 Differential pair #0 non-inverting line	TMDS2_DATA2+	TMDS2 Differential pair #2 non-inverting line
D40	DDI2_PAIR0-	DP2_LANE0-	DP2 Differential pair #0 inverting line	TMDS2_DATA2-	TMDS2 Differential pair #2 inverting line
D42	DDI2_PAIR1+	DP2_LANE1+	DP2 Differential pair #1 non-inverting line	TMDS2_DATA1+	TMDS2 Differential pair #1 non-inverting line
D43	DDI2_PAIR1-	DP2_LANE1-	DP2 Differential pair #1 inverting line	TMDS2_DATA1-	TMDS2 Differential pair #1 inverting line
D46	DDI2_PAIR2+	DP2_LANE2+	DP2 Differential pair #2 non-inverting line	TMDS2_DATA0+	TMDS2 Differential pair #0 non-inverting line

D47	DDI2_PAIR2-	DP2_LANE2-	DP2 Differential pair #2 inverting line	TMDS2_DATA0-	TMDS2 Differential pair #0 inverting line
D49	DDI2_PAIR3+	DP2_LANE3+	DP2 Differential pair #3 non-inverting line	TMDS2_CLK+	TMDS2 Differential clock non-inverting line
D50	DDI2_PAIR3-	DP2_LANE3-	DP2 Differential pair #3 inverting line	TMDS2_CLK-	TMDS2 Differential clock inverting line
D44	DDI2_HPD	DP2_HPD	DP2 Hot Plug Detect signal	HDMI2_HPD	HDMI #2 Hot Plug Detect signal
C32	DDI2_CTRLCLK_AUX+	DP2_AUX+	DP2 Auxiliary channel non-inverting line	HDMI2_CTRLCLK	DDC Clock line for HDMI panel #2..
C33	DDI2_CTRLDATA_AUX-	DP2_AUX-	DP2 Auxiliary channel inverting line	HDMI2_CTRLDATA	DDC Data line for HDMI panel #2.
C34	DDI2_DDC_AUX_SEL	DDI#2 DP or TMDS interface selector: pull this signal low or leave floating for DP++ interface, pull high (+3.3V_S) for TMDS interface			

All Hot Plug Detect Input signals (valid both for DP++ and TMDS interface) are +3.3V_S electrical level signal, active high with 1MΩ pull-down resistors.

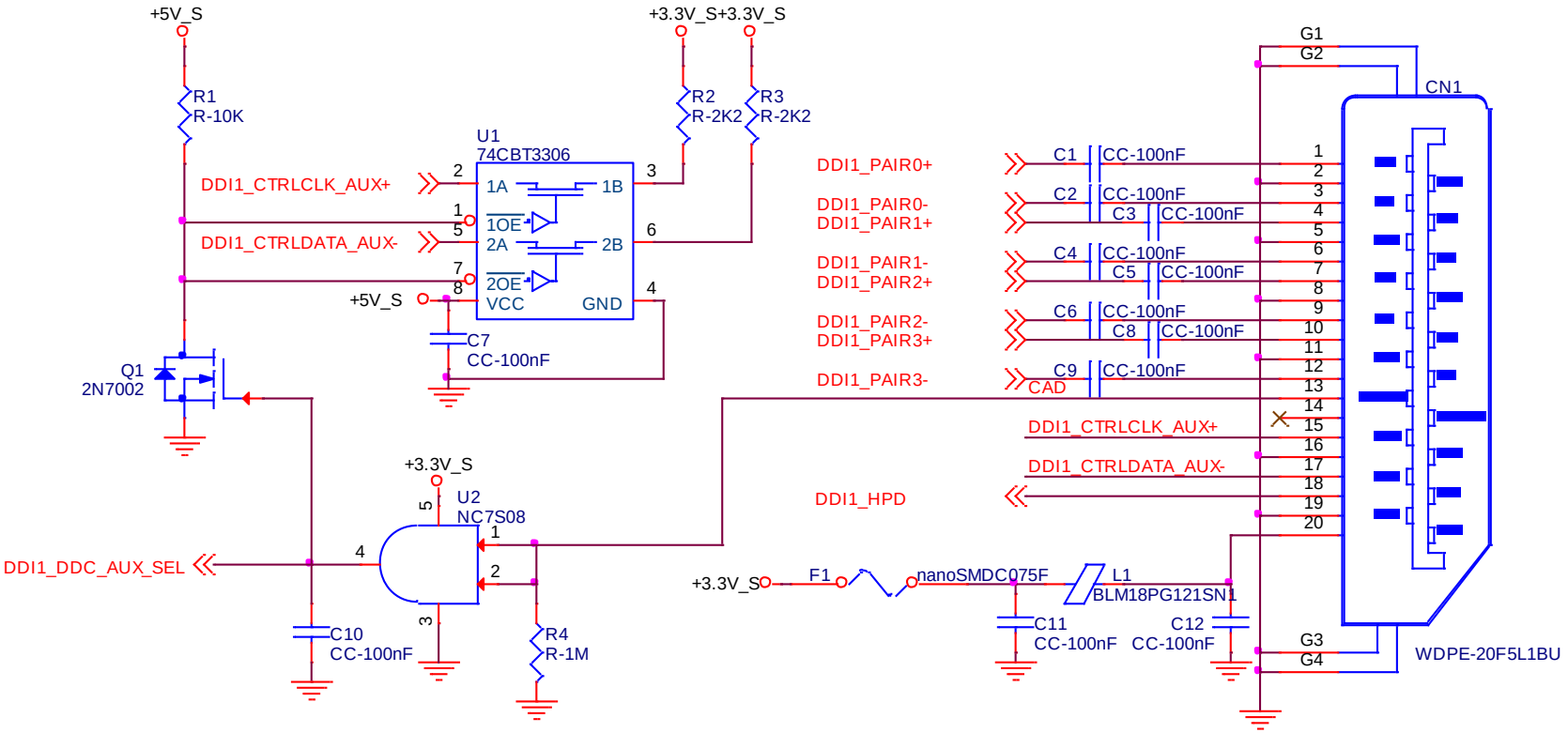
All HDMI Control signals (CTRLCLK and CTRLDATA) are bidirectional signal, electrical level +3.3V_S with a 100kΩ pull-up resistor

Please be aware that for correct implementation of HDMI/DVI interfaces, it is necessary to implement, on the Carrier board, voltage level shifter for TMDS differential pairs, for Control data/Clock signals and for Hot Plug Detect signal.

Voltage clamping diodes are also highly recommended on all signal lines for ESD suppression.

> **!** Please be aware that Digital Display Interface #1, available on pins named as DDI2_xxx,can be internally switched to drive eDP or LVDS displays, as explained in paragraphs 3.2.3.7 and 3.2.3.8. This means that on the carrier board it is possible to use the DDI2 interface or the eDP / LVDS interface, it is not possible to use both of them simultaneously.

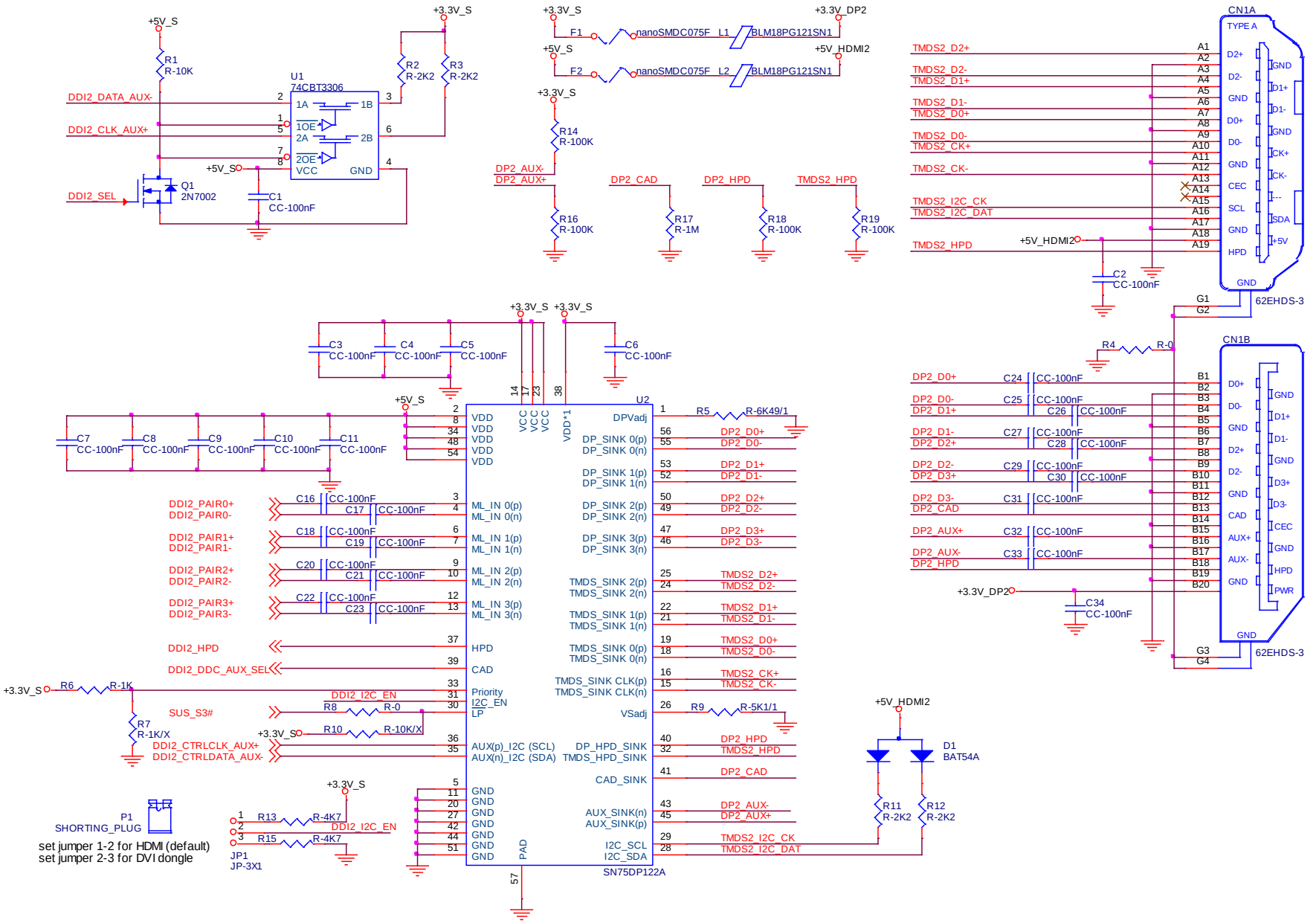
Here following an example of implementation of multimode Display Port on the carrier board. In this example, are used signals related to Digital Display interface #1, but any DDI interface can be used.



The example schematics in the following page, instead, shows the implementation (using DDI interface #2, but any DDI can be used for this purpose) of a double connector DP++ and HDMI, managed using a DisplayPort 1:2 Switch with Integrated TMDS Translator, which provides to TMDS voltage level shifter for HDMI/DVI connection.

By implementing such a schematic, the module can configure itself automatically to work with external HDMI/DVI or multimode Display Port interfaces, depending on the cable connected. In case both an HDMI and a DP are connected, the HDMI interface will take priority automatically. This order can be changed by removing resistor R6 and mounting resistor R7.

The jumper JP1 is used to enable or disable switch's I2C internal registers, for use of TMDS interface, respectively, for HDMI or DVI displays.


+5V_S
+3.3V_S
+3.3V_DP2
+5V_HDMI2
R1
R-10K
R2
R-2K2
R3
R-2K2
U1
74CBT3306
DDI2_DATA_AUX-
DDI2_CLK_AUX+
DDI2_SEL
Q1
2N7002
C1
CC-100nF
F1
F2
nanoSMDC075F
BLM18PG121SN1
L1
L2
R14
R-100K
R16
R-100K
R17
R-1M
R18
R-100K
R19
R-100K
DP2_AUX-
DP2_AUX+
DP2_CAD
DP2_HPD
TMDS2_HPD
CN1A
TYPE A
TMDS2_D2+
TMDS2_D2-
TMDS2_D1+
TMDS2_D1-
TMDS2_D0+
TMDS2_D0-
TMDS2_CK+
TMDS2_CK-
TMDS2_I2C_CK
TMDS2_I2C_DAT
C2
CC-100nF
G1
G2
62EHDS-3
C3
C4
C5
C6
CC-100nF
U2
SN75DP122A
DPVadj
DP_SINK 0(p)
DP_SINK 0(n)
DP_SINK 1(p)
DP_SINK 1(n)
DP_SINK 2(p)
DP_SINK 2(n)
DP_SINK 3(p)
DP_SINK 3(n)
TMDS_SINK 2(p)
TMDS_SINK 2(n)
TMDS_SINK 1(p)
TMDS_SINK 1(n)
TMDS_SINK 0(p)
TMDS_SINK 0(n)
TMDS_SINK CLK(p)
TMDS_SINK CLK(n)
VSadj
DP_HPD_SINK
TMDS_HPD_SINK
CAD_SINK
AUX_SINK(n)
AUX_SINK(p)
I2C_SCL
I2C_SDA
R5
R-6K49/1
R9
R-5K1/1
DDI2_PAIR0+
DDI2_PAIR0-
DDI2_PAIR1+
DDI2_PAIR1-
DDI2_PAIR2+
DDI2_PAIR2-
DDI2_PAIR3+
DDI2_PAIR3-
ML_IN 0(p)
ML_IN 0(n)
ML_IN 1(p)
ML_IN 1(n)
ML_IN 2(p)
ML_IN 2(n)
ML_IN 3(p)
ML_IN 3(n)
DDI2_HPD
DDI2_DDC_AUX_SEL
SUS_S3#
DDI2_I2C_EN
DDI2_CTRLCLK_AUX+
DDI2_CTRLDATA_AUX-
HPD
CAD
Priority
I2C_EN
LP
AUX(p)_I2C (SCL)
AUX(n)_I2C (SDA)
R6
R-1K
R7
R-1K/X
R8
R-0
R10
R-10K/X
P1
SHORTING_PLUG
set jumper 1-2 for HDMI (default)
set jumper 2-3 for DVI dongle
JP1
JP-3X1
R13
R-4K7
R15
R-4K7
D1
BAT54A
R11
R-2K2
R12
R-2K2
R4
R-0
CN1B
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
CC-100nF
DP2_D0+
DP2_D0-
DP2_D1+
DP2_D1-
DP2_D2+
DP2_D2-
DP2_D3+
DP2_D3-
DP2_CAD
DP2_AUX+
DP2_AUX-
DP2_HPD
G3
G4
62EHDS-3

3.2.3.12 UART interface signals

According to COM Express® Rel. 2.0 specifications, since the COMe-A41-CT6 is a Type 6 module, it can offer two UART interfaces, which are managed by the embedded microcontroller.

Here following the signals related to UART interface:

SER0_TX: UART Interface #0, Serial data Transmit (output) line, 3.3V_S electrical level.

SER0_RX: UART Interface #0, Serial data Receive (input) line, 3.3V_S electrical level.

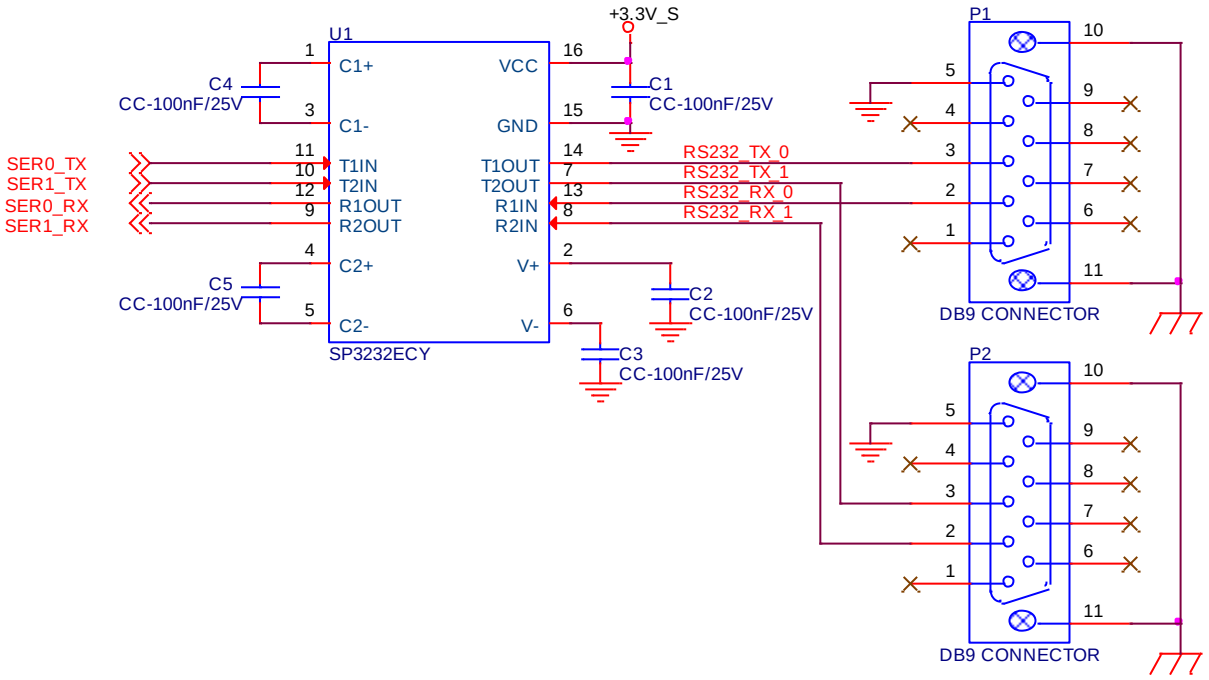
SER1_TX: UART Interface #1, Serial data Transmit (output) line, 3.3V_S electrical level.

SER1_RX: UART Interface #1, Serial data Receive (input) line, 3.3V_S electrical level.

In COM Express® specifications prior to Rel. 2.0, the pins dedicated to these two UART interfaces were dedicated to +12V_{IN} power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on UART interfaces' TX and RX lines so that they are +12V Tolerant.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it is not explicitly necessary to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The schematic on the right shows an example of implementation of RS-232 transceiver for the Carrier board.



3.2.3.13 I2C interface signals

This interface is managed by the embedded microcontroller.

Signals involved are the following:

I2C_CK: general purpose I2C Bus clock line.

I2C_DAT: general purpose I2C Bus data line.

3.2.3.14 Miscellaneous signals

Here following, a list of COM Express® compliant signals that complete the features of COMe-A41-CT6 module.

SPKR: Speaker output, +1.8V_S voltage signal, open drain, managed by SOC's embedded counter 2.

WDT: Watchdog event indicator Output. It is an active high signal, +3.3V_S voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. This signal is managed by the module's embedded microcontroller.

FAN_PWM_OUT*: PWM output for FAN speed management, +3.3V_S voltage signal. It is managed by the module's embedded microcontroller.

FAN_TACHOIN*: External FAN Tachometer Input. +3.3V_S voltage signal, directly managed by the module's embedded microcontroller.

TPM_PP: Trusted Platform Module (TPM) Physical Presence pin. This signal is used to indicate Physical Presence to the optional TPM device onboard. It is an active high input signal. Please be aware that if the module purchased doesn't have the TPM module, this pin will result not connected.

THRM#: Thermal Alarm Input. Active Low +3.3V_S voltage signal with 10kΩ pull-up resistor, directly managed by the module's embedded microcontroller. This input gives the possibility, to carrier board's hardware, to indicate to the main module an overheating situation, so that the CPU can begin thermal throttling.

THRMTRIP#: Active Low +3.3V_S voltage output signal. This signal is used to communicate to the carrier board's devices that, due to excessive overheating, the CPU began the shutdown in order to prevent physical damages.

* Note: In COM Express® specifications prior to Rel. 2.0, the pins dedicated to FAN management were dedicated to $+12V_{IN}$ power rail. In order to prevent damages to the module, in case it is inserted in carrier board not designed for Type 6, then protection circuitry has been added on FAN_PWM_OUT and FAN_TACHOIN lines so that they are +12V Tolerant.

3.2.3.15 Power Management signals

According to COM Express® specifications, on the connector AB there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWRBTN#: Power Button Input, active low, +3.3V_A buffered voltage signal with 10kΩ pull-up resistor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

SYS_RESET#: Reset Button Input, active low, +3.3V_A voltage signal with 10kΩ pull-up resistor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the COMe-A41-CT6 module.

CB_RESET#: System Reset Output, active low, +3.3V_A voltage buffered signal. It can be used directly to drive externally a single RESET Signal. In case it is necessary to supply Reset signal to multiple devices, a buffer on the carrier board is needed.

PWR_OK: Power Good Input, +3.3V_S active high signal. It must be driven by the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

SUS_STAT#: Suspend status output, active low +3.3V_A electrical voltage signal. This output can be used to report to the devices on the carrier board that the module is going to enter in one of possible ACPI low-power states.

SUS_S3#: S3 status output, active low +3.3V_A electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S4#: S4 status output, active low +3.3V_A electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S4 (Suspend to Disk) power state.

SUS_S5#: S5 status output, active low +3.3V_A electrical voltage signal. This signal is not managed by Intel™ Bay Trail family of SOCs, therefore this signal is electrically tied to SUS_S4# signal.

WAKE0#: PCI Express Wake Input, active low +3.3V_A electrical voltage signal with 27kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event related to PCI Express has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

WAKE1#: General Purpose Wake Input, active low +3.3V_A electrical voltage signal with 2k2Ω pull-up resistor. It can be driven low, on the carrier board, to report that a general Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

BATLOW#: Battery Low Input, active low, +3.3V_A voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. It can be left unconnected if not used.

LID# *: LID button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a LID Switch on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

SLEEP# *: Sleep button Input, active low +3.3V_A electrical level signal, with 10kΩ pull-up resistor. This signal can be driven, using a pushbutton on the carrier board, to trigger the transition of the module from Working to Sleep status, or vice versa. It can be left unconnected if not used on the carrier board.

3.2.3.16 SMBus signals

This interface is directly managed by the SOC.

Signals involved are the following:

SMB_CK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_A with a 4k7Ω pull-up resistor.

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_A with a 4k7Ω pull-up resistor.

SMB_ALERT#: SM Bus Alert line for System Management. Input signal, electrical level +3.3V_A with a 10kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

3.2.3.17 GPIO/SD interface signals

According to COM Express® specifications rel. 2.0, there are 8 pins that can be used as General Purpose Inputs and Outputs **OR** as a SDIO interface.

The Intel® Bay trail family of SOCs embeds one SD Card 3.0 controller, therefore can provide for the SD (not SDIO) interface on these pins. The embedded microcontroller, instead, is used to realise four General Purpose Inputs and four General Purpose Outputs. Via BIOS, it is possible to switch between SD interface and GPI/Os for the external connection (please check par. 4.3.5).

Please refer to the following table for a description of the signals in both configurations.

GPIO / SD Interfaces - Pin multiplexing					
		GPIO mode		SDIO mode	
Pin nr.	Pin name	Signal	Description	Signal	Description
A54	GPI0	GPI0	General Purpose Input #0	SD_DATA0	SD Card Data Line 0.
A63	GPI1	GPI1	General Purpose Input #1	SD_DATA1	SD Card Data Line 2. Required only for 4-bit communication mode
A67	GPI2	GPI2	General Purpose Input #2	SD_DATA2	SD Card Data Line 2. Required only for 4-bit communication mode
A85	GPI3	GPI3	General Purpose Input #3	SD_DATA3	SD Card Data Line 1. Required only for 4-bit communication mode
A93	GPO0	GPO0	General Purpose Output #0	SD_CLK	SD Clock Output
B54	GPO1	GPO1	General Purpose Output #1	SD_CMD	SD Command/Response line. Bidirectional signal, used to send command from Host to the connected card, and the response from the card to the Host.
B57	GPO2	GPO2	General Purpose Output #2	SD_WP	Write Protect input. It is used to communicate the status of Write Protect switch of the external SD card.
B63	GPO3	GPO3	General Purpose Output #3	SD_CD#	Card Detect Input, active low Signal. This signal must be externally pulled low to signal when a SD Card Device is present.

Special consideration about SD_WP signal: since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal is tied to GND, otherwise the OS will always consider the card as protected from writing.

Chapter 4.
BIOS SETUP

- InsydeH2O setup Utility
- Main setup menu
- Advanced menu
- Security menu
- Power menu
- Boot menu
- Exit menu

4.1 InsydeH2O setup Utility

Basic setup of the board can be done using Insyde Software Corp. "InsydeH2O Setup Utility", that is stored inside an onboard SPI Serial Flash.

It is possible to access to InsydeH2O Setup Utility by pressing the <ESC> key after System power up, during POST phase. On the splash screen that will appear, select "SCU" icon.

On each menu page, on left frame are shown all the options that can be configured.

Grayed-out options are only for information and cannot be configured.

Only options written in blue can be configured. Selected options are highlighted in white.

Right frame shows the key legend.

KEY LEGEND:

← / →	Navigate between various setup screens (Main, Advanced, Security, Power, Boot...)
↑ / ↓	Select a setup item or a submenu
<F5> / <F6>	<F5> and <F6> keys allows to change the field value of highlighted menu item
<F1>	The <F1> key allows to display the General Help screen.
<F9>	<F9> key allows loading Setup Defaults for the board. After pressing <F9> BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<F10>	<F10> key allows save any changes made and exit Setup. After pressing <F10> key, BIOS Setup utility will request for a confirmation, before saving and exiting. By pressing <ESC> key, this function will be aborted
<ESC>	<Esc> key allows to discard any changes made and exit the Setup. After pressing <ESC> key, BIOS Setup utility will request for a confirmation, before discarding the changes. By pressing <Cancel> key, this function will be aborted
<ENTER>	<Enter> key allows to display or change the setup option listed for a particular setup item. The <Enter> key can also allow to display the setup sub- screens.

4.2 Main setup menu

When entering the Setup Utility, the first screen shown is the Main setup screen. It is always possible to return to the Main setup screen by selecting the Main tab.

In this screen, are shown details regarding BIOS version, Processor type, Bus Speed and memory configuration.

Only two options can be configured:

4.2.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values directly through the keyboard, or using + / - keys to increase / reduce displayed values. Press the <Enter> key to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

The system date is in the format mm/dd/yyyy.

4.3 Advanced menu

Menu Item	Options	Description
Boot Configuration	See submenu	Configures settings for Boot Phase
PCI Express Configuration	See submenu	PCI Express Configuration Settings
USB Configuration	See submenu	Configures USB Section
Audio Configuration	See submenu	Configures Audio Section
LPSS & SCC Configuration	See submenu	Configures LPSS (Low-Power Sub-System, i.e. DMA, PWM, UART and I2C interfaces) and SCC (Storage Control Cluster) devices
Miscellaneous Configuration	See submenu	Enable / Disable Misc. features
Security configuration (TXE)	See submenu	
Video Configuration	See submenu	Configures the options for video section
Chipset Configuration	See submenu	Configure Chipset's parameters
SATA Configuration	See submenu	Select the SATA controller and hard disk drive type installed in the system
Console Redirection	See submenu	Configures the parameters for Console redirection
ACPI Table / Features Control	See submenu	Configures the parameters for ACPI management
Super I/O Configuration	See submenu	Super I/O Setup Configuration Utility
INT/IRQ Configuration	See submenu	Configures PCI INT and IRQ assignments

4.3.1 Boot configuration submenu

Menu Item	Options	Description
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off

4.3.2 PCI Express configuration submenu

Menu Item	Options	Description
PCI Express Root Port 0 PCI Express Root Port 1 PCI Express Root Port 2 PCI Express Root Port 3 (internal LAN)	See submenu	

4.3.2.1 PCI Express Root Port #x configuration submenus

Menu Item	Options	Description
PCI Express Root Port #x	Disabled / Enabled	Enable or Disable single PCI Express Root Port #x. PCI Express Root Port#3 is internally connected to Intel® Gigabit Ethernet Controller I210 Disabling this port will result in disabling Ethernet interface.
PCI Express Port #x Speed	Auto / Gen1 / Gen2	This menu item is available only when corresponding Root Port is set to Enabled. Set PCI-e ports link speed/capability. Not available for PCI Express Root Port #3
PCI Express Port #x ASPM	Disabled / L0s / L1 / L0s & L1 / Auto	This menu item is available only when corresponding Root Port is set to Enabled. Manages PCI Express L0s and L1 power states, for OSs able to handle Active State Power Management (ASPM). Not available for PCI Express Root Port #3

4.3.3 USB configuration submenu

Menu Item	Options	Description
USB BIOS Support	Disabled / Enabled / UEFI Only	Sets the support for USB keyboard / mouse / storage under UEFI and DOS environment. When set to UEFI only, then it will support exclusively UEFI environment.
xHCI Mode	Disabled Enabled Auto Smart Auto Best Auto	Mode of operation of xHCI controller Disabled: USB 3.0 functionalities are always disabled, USB 3.0 devices will work in High Speed Mode Enabled: USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the xHCI driver is installed). Auto: USB 3.0 devices will work only when OS has started, provided that hcSwitch and xHCI drivers are installed. In BIOS and during boot USB 3.0 devices will work in High Speed mode Smart Auto: when starting from a Mechanical Off (G3) state, USB 3.0 functionalities are available both in BIOS and in OS (also for booting, provided that the hcSwitch and xHCI driver is installed). When the system boots from a different ACPI state, USB 3.0 devices will be managed by xHCI or EHCI controller depending on the last used configuration. Best Auto: always route to xHCI
Win7 Uninstall xHCI driver workaround	Disabled / Enabled	Enable / Disable Windows 7 Uninstall xHCI driver workaround. When enabled, Windows 7 USB (EHCI mode) will still work after uninstalling xHCI driver, but the WHCK test will fail
xHCI Controller	Disabled / Enabled	Enable/Disable xHCI Controller for USB 3.0 functionalities support
USB2 Link Power Management	Disabled / Enabled	Can be changed only when “xHCI Controller” is Enabled Enable/Disable the USB2 Link Power Management, i.e. the management of different Link Power (Lx) States of connected USB devices depending on the workload of the device itself.
xHCI Streams	Disabled / Enabled	Can be changed only when “xHCI Controller” is Enabled Enable/Disable the xHCI Stream Support.
EHCI Controller	Disabled / Enabled	Controls the USB EHCI (USB 2.0) functionalities. One EHCI controller must always be enabled.
USB EHCI debug	Disabled / Enabled	Can be changed only when “EHCI Controller” is Enabled Enable / Disable PCH EHCI debug capability
USB Per-Port Control	Disabled / Enabled	Allows to enable / disable singularly each of USB ports #0 ÷ #3
USB Ports #0 to #3 USB Port #4 USB Port #5 USB Port #6	Disabled / Enabled	Available only when “USB Per-Port Control” is Enabled. Allows to enable / disable individually each external USB port. Due to the routing of the USB Root Ports on COMe-A41-CT6 module, disabling the USB Port#0 will disable all the four USB 3.0 ports and the external USB 2.0 ports #0÷#3, disabling the internal USB Port #1 will disable the external USB Port #4, disabling the internal USB Port #2 will disable the external USB Port #5 and disabling the internal USB Port #3 will disable the external USB Port #6

USB Ignore Settings	See Submenu	Allows excluding BIOS support for single USB Devices/Ports/Hosts.
USB Ignore Request Timeout (sec.)	0÷30	When enabled (i.e., timeout greater than zero), for each USB bootable device it is required the user confirmation. Without any action, when the timeout expires the USB device is ignored. If the timeout is set to zero, it means that this feature is disabled, and the boot sequence works in the standard way. When enabled, the Confirm Dialog Box is displayed only for disks with a valid MBR.
Display USB Device's Name	Disabled / Enabled	Available only when "USB Ignore request Timeout (Sec.)" is Set. Allows enabling / disabling the disabling of USB Device's name in the timeout string.

4.3.3.1 USB Ignore Settings submenu

Using this submenu, it is possible to define up to four (4) rules for the USB ports to be ignored from BIOS support, if desired. Each rule will offer the following options:

Menu Item	Options	Description
Host Controller	None / All / Int. xHCI (Usb3.0) / Int. EHCI (Usb2.0)	Select the Host Controller to ignore
Port	None / All / Port 0 / Port 1 / Port 2 / Port 3 / Port 4 / Port 5 / Port 6 / Port 7	Select the USB Port to ignore
USB Class	None All Hid Mass Storage	Select the USB Class of Devices to ignore. HID: Touch Controllers, Mouses Keyboards Mass Storage: USB disks, CD/DVD, Floppy Disks
Vendor ID	0x0001 ÷ 0 x FFFE	Specify the Vendor ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None
Device ID	0x0001 ÷ 0 x FFFE	Specify the Device ID to ignore. 0xFFFF = Ignore All 0xFFFE = Ignore None

! If the BIOS support is excluded for all ports and/or all HID devices, it will be impossible to enter in the Setup Configuration utility using USB keyboards.

Please be careful before changing these settings.

4.3.4 Audio configuration submenu

Menu Item	Options	Description
Audio Controller	Disabled / Enabled	Controls the detection of the Azalia Audio Controller Disabled: the Audio controller will be unconditionally Disabled Enabled: the Audio controller will be unconditionally Enabled
VC1 Enable	Disabled / Enabled	Available only when “Audio Controller” is Enabled Enable or Disable Virtual Channel 1 of Audio Controller
Azalia HDMI Codec	Disabled / Enabled	Enable or Disable internal HDMI Codec for Azalia

4.3.5 LPSS & SCC configuration submenu

Menu Item	Options	Description
LPSS & SCC Devices Mode	ACPI Mode PCI Mode	Allows setting the Working mode of LPSS (Low-Power Sub-System) and SCC (Storage Control Cluster) devices. Use PCI mode for Windows® 7, use ACPI mode for Android and Windows® 8
LPSS & SCC Auto Switch	Enable / Disable	Available only when “LPSS & SCC Devices Mode” is set to ACPI Mode. Auto switches LPSS and SCC devices from ACPI mode to PCI mode when the OS doesn’t support ACPI mode.
Hide unsupported LPSS devices	Enable / Disable	Available only when “LPSS & SCC Devices Mode” is set to ACPI Mode. Hide unsupported LPSS devices when in ACPI mode.
SCC eMMC Boot Controller	Disabled / Enabled	Enable/ Disable the eMMC controller
eMMC Secure Erase	Enable / Disable	Can be changed only when “SCC eMMC Boot Controller” is enabled. Disable/Enable eMMC Secure Erase. When enabled, all the data on eMMC will be erased.
DDR50 Capability Support	Enable / Disable	Can be changed only when “SCC eMMC Boot Controller” is enabled. Enable or Disable SCC eMMC 4.5 DDR50 support
HS200 Capability Support	Enable / Disable	Can be changed only when “SCC eMMC Boot Controller” is enabled. Enable or Disable SCC eMMC 4.5 DDR50 support
Re Tune Timer Value	0 / 1 / 2 / 3 / 4 / 5 / 6 / 7 / 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15	Can be changed only when “SCC eMMC Boot Controller” is enabled.and “DDR50 Capability Support is disabled. Sets the re-tune timer value
GPIO/SD Card Selection	GPIO / SD Card	Select the GPIO or SD Card function on multiplexed pins (please check par. 3.2.3.17).

4.3.6 Miscellaneous Configuration submenu

Menu Item	Options	Description
HPET - HPET Support	Enabled / Disabled	High Precision Event Timer is supported in Windows Vista or above. HPET controller should not been seen in Windows XP, no matter if enabled/disabled in SCU. If this feature is enabled, the HPET table will be added into ACPI Tables.
Clock Spread Spectrum	Enabled / Disabled	Allows enabling Clock Chip's Spread Spectrum feature
BIOS Lock	Enabled / Disabled	Enable or disable BIOS SPI region write protect
PCI Express Dynamic Clock Gating	Enabled / Disabled	Enable or Disable PCI Express Dynamic Clock Gating
Force Legacy Free	Enable / Disable	When enabled, this item will force the Legacy Free mode (it will disable the KBC).
Serial IRQ	Enabled / Disabled	Enables or disables the Serial IRQ.
Serial IRQ Mode	Quiet Mode Continuous Mode	Select Serial IRQ Mode. In continuous mode, the host will continually check for device interrupts. In Quiet Mode, Host will wait for a SERIRQ slave to generate a request by driving the SERIRQ line low.

4.3.7 Security configuration (TXE) submenu

Menu Item	Options	Description
TXE	Disabled / Enabled	Enable or Disable the Intel® Trusted Execution Engine (TXE, available only on Celeron CPUs)
TXE HMRFP0	Disabled / Enabled	Enable this option to remove temporarily the flash protection, in order to program the Intel® TXE region
TXE Firmware update	Disabled / Enabled	Enable this option to require a re-flashing of TXE Firmware Image
TXE EOP Message	Disabled / Enabled	Send EOP (End of POST) Message before entering OS
TXE Unconfiguration Perform	Yes / No	Only selectable on CPUs with the TXE feature. Allows to revert TXE settings to the factory defaults

4.3.8 Video configuration submenu

Menu Item	Options	Description
CRT	Enabled / Disabled	Enable or Disable the CRT Video Output of the module
DDI0 Configured As	Display Port HDMI/DVI DisplayPort with HDMI/DVI Compatible No Device	Select the Hardware DDI0 configuration for the proper usage on the Carrier Board.
DDI1 Configured As	eDP→LVDS Display Port HDMI/DVI DisplayPort with HDMI/DVI Compatible No Device	Select the Hardware DDI1 configuration for the proper usage on the Carrier Board. eDP→ LVDS setting has to be used in case the DDI1 interface has to be used for the connection of eDP or LVDS displays (depending on the factory configuration of the module) though the COM Express connector AB, the other settings for displays connected, on the carrier board, through the connector CD.
Primary Display	CRT / DDI0 / DDI1 / None	Select the Primary Display for the use in WEC7 operating System
Secondary Display	CRT / DDI0 / DDI1 / None	Select the Secondary Display for the use in WEC7 operating System
Display Mode	Single / Extended / Extended Vertical / Clone	Select the Display Mode for the use in WEC7 operating System
LFP	Custom / 640x480 / 800x480 800x600 / 1024x600 / 1024x768 / 1280x720 / 1280x800 / 1280x1024 / 1366x768 / 1400x900 / 1600x900 / 1680x1050 / 1920x1080	Select a software resolution (EDID settings) to be used for the internal flat panel.
LFP Color Mode	VESA 24bpp JEIDA 24bpp 18 bpp	Select the color depth of LVDS interface. For 24-bit color depth, it is possible to choose also the color mapping on LVDS channels, i.e. if it must be VESA-compatible or JEIDA compatible.
LFP Interface	Single Channel Dual Channel	Allows configuration of LVDS interface in Single or Dual channel mode
LFP Spreading Depth	No Spreading / 0.5% / 1.0% 1.5% / 2.0% / 2.5%	Sets percentage of bandwidth of LVDS clock frequency for spreading spectrum
LFP Output Swing	150 mV / 200 mV / 250 mV / 300 mV / 350 mV / 400 mV / 450 mV	Sets the LVDS differential output swing

LFP Default brightness (%)	0 ÷ 100	LFP Default brightness percentage. Valid values are in the range 0-100, where 0 means backlight OFF. This setup configuration, during the BIOS boot, is valid only with a single LFP connected (no multi-monitor).
LFP Max ACPI Brightness (%)	0 ÷ 100	Maximum ACPI Brightness percentage allowed with an ACPI aware OS
Integrated Graphics Device	Disabled / Enabled	Enabled: enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disabled: always disable IGD
Primary Display	Auto / IGD / PCIe	Select which of IGD or external PCI-e Graphic Controller should be the Primary display
RC6(Render Standby)	Disabled / Enabled	Permits to enable the render standby features, which allows the onboard graphics entering in standby mode to decrease power consumption
PAVC	Disabled / LITE Mode / SERPENT Mode	Allows enabling the hardware acceleration of decoding of Protected Audio Video streams. When LITE is Control, choosing is LITE encryption or SERPENT encryption has to be used.
Power Management Lock	Disabled / Enabled	Enable / Disable Power Management Lock
DOP CG	Disabled / Enabled	Enable / Disable DOP Clock Gating
GTT Size	1MB / 2MB	Select the GTT (Graphics Translation Table) Size
Aperture Size	128MB / 256MB / 512MB	Use this item to set the total size of Memory that must be left to the GFX Engine
IGD - DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphic Device
IGD - DVMT Total Gfx Mem	128M / 256M / MAX	Select the size of DVMT (Dynamic Video Memory) 5.0 that the Internal Graphics Device will use
IGD Turbo	Auto / Enabled / Disabled	Enable or Disable IGD Turbo mode
IGD Thermal	Disabled / Enabled	Enabled or disable Thermal Control of IGD
Spread Spectrum clock	Disabled / Enabled	Enable or disable LVDS Spread Spectrum Clock
Backlight Control	Auto PWM-Inverted PWM-Normal	Backlight control setting

4.3.9 Chipset configuration submenu

Menu Item	Options	Description
PCI 64-bit Decode	Enabled / Disabled	Allow system to support 64-bit BAR (Base Address Register) for PCI devices.
CRID	Enabled / Disabled	Enable / Disable CRID (Configured Revision ID) register.

4.3.10 SATA configuration submenu

Menu Item	Options	Description
SATA Controller	Enabled / Disabled	Disabled: Disables SATA Controller. All following items will be disabled Enabled: Enables SATA Controller
Sata Port 0	Enabled / Disabled	Enables or disable SATA Port #0
Sata Port 1	Enabled / Disabled	Enables or disable SATA Port #1
Chipset SATA Mode	IDE AHCI	Set SATA Configuration type With AHCI, is not possible to install/boot UEFI O.S., only Legacy OS can be installed (a simpler driver is required). Setting to IDE, the controller is managed as a PCI device, so addresses reallocation and INT line sharing is possible.
SATA Speed	Gen1 / Gen2	Select SATA speed
SATA Port 0 Hot Plug Capability SATA Port 1 Hot Plug Capability	Enabled / Disabled	These items will be available only when “Chipset SATA Mode” is set to AHCI. If enabled, SATA port will be reported as Hot Plug Capable
IDE Max Transfer Mode	Auto Ultra ATA/100 Ultra ATA/66 Ultra ATA/33 PIO Mode	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Interfaces’ maximum Transfer Rate
IDE Mode	Native IDE Legacy IDE	This item will be available only when “Chipset SATA Mode” is set to IDE. Sets the IDE Working Mode
Serial ATA Port 0 / 1		Shows information related to eventual devices connected to SATA ports 0 or 1

4.3.11 Console Redirection submenu

Menu Item	Options	Description
Console Serial Redirect	Enabled / Disabled	Enable or disable Console redirection. When enabled, all the submenus of the following paragraph will appear
Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Set Console Redirection terminal type
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Set Console Redirection baud rate
Data Bits	7 bits / 8 bits	Set Console Redirection data bits
Parity	None / Even / Odd	Set Console Redirection parity bits
Stop Bits	1 bit / 2 bits	Set Console Redirection stop bits
Flow Control	None RTS/CTS XON/XOFF	Set Console Redirection flow control type
Information Wait Time	0 Seconds / 2 Seconds / 5 Seconds / 10 Seconds / 30 Seconds	Set Console Redirection port information display time
C.R. After Post	Yes / No	Console Redirection continues to work even after Bios POST.
AutoRefresh	Enabled / Disabled	When this feature is enabled, the screen will auto refresh once after detecting the connection of a remote terminal
FailSafeBaudRate		This feature will auto detect remote terminal baud rate and connect C.R serial device with detected baud rate
ACPI SPCR Table	Enabled / Disabled	Serial Port Console Redirection Table. When this feature is enabled, the SPCR table will be add-into ACPI tables.
Serial Port 0 - *Addr* IRQy Serial Port 1 - *Addr* IRQy Serial Port 2 - *Addr* IRQy Serial Port 3 - *Addr* IRQy	See following menu items	These voices will be available only when Console Serial Redirect is Enabled and if at least one LPC Super I/O is present on the carrier board. Depending on the SuperI/O(s) found on the carrier board, this item will show the serial ports that are available, with their address and IRQ (assigned). For each port it will be possible to set the paramters shown in the following lines
PortEnable	Enable / Disabled	Enable / Disable single serial Port x for the console redirection
UseGlobalSetting	Enable / Disabled	Use or not global settings for Serial Port x for the console Redirection

Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Set Console Redirection terminal type
Baud rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Set Console Redirection baud rate
Data Bits	7 bits / 8 bits	Set Console Redirection data bits
Parity	None / Even / Odd	Set Console Redirection parity bits
Stop Bits	1 bit / 2 bits	Set Console Redirection stop bits
Flow Control	None RTS/CTS XON/XOFF	Set Console Redirection flow control type

4.3.12 ACPI Table/features submenu

Menu Item	Options	Description
FACP - RTC S4 wakeup	Enabled / Disabled	Enable or disable FACP (Fixed ACPI Description Table) support for S4 wakeup from RTC
FACP - Sleep Button	Enabled / Disabled	Enable or disable the FACP flag for the Sleep Button.
DSDT - ACPI S3	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S3 State
DSDT - ACPI S4	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI S4 State
DSDT - ACPI BGRT	Enabled / Disabled	Enable or disable DSDT (Differentiated System Description Table) support for ACPI Boot Graphics Resource Table

4.3.13 SuperI/O configuration submenu

Menu Item	Options	Description
Name of the SuperI/O found		This menu item will show the name of all the Super I/Os that are found on the carrier board. By selecting the adequate SuperI/O, it will be possible to set the serial ports and possibly other parameters as shown in the following menu items. If no Super I/O is available on the Carrier Board, this menu will not be available.
Keyboard Controller	Enabled / Disabled	Enable / disable the Keyboard Controller (if the SuperI/O supports it, otherwise this item will not be available).
Serial Port 1 / Serial Port 2 / Serial Port 3 / Serial Port 4	Enabled / Disabled	Enable or Disable single serial port #1, #2, #3 or #4 (the number of serial ports depends on the Super I/O).
Address	0x3F8 / 0x2F8 / 0x3E8 / 0x2E8 / 0x3E0 / 0x2E0 / 0x338 / 0x238 / 0x220 / 0x228	Select the Base address for each Serial Port, if enabled.
IRQ	3 / 4 / 5 / 6/ 7 / 10 / 11 / 14 / 15	Select the IRQ line to assign to each Serial Port, if enabled.
Floppy Disk Controller	Enabled / Disabled	Enable / disable the Floppy Disk Controller, if the SuperI/O supports it
Parallel Port Mode	Parallel Port / External FDC	Configure the Parallel Port mode of working, if the SuperI/O supports it
LPT Port	Enabled / Disabled	When the previous item is set to “Parallel Port”, this item will allow to enable or disable the LPT port.
LPT Mode	SPP / EPP 1.9 and SPP / ECP / ECP-EPP 1.9 / Printer Mode / EPP 1.7 and SPP / ECP-EPP 1.7	When the LPT port is enabled, this item will allow to configure the LPT protocol
Hardware Monitor	Enabled / Disabled	Enable or disable the Super I/O Hardware monitor (if it is supported by the Super I/O)
Watchdog	Disabled / 1 Minute / 2 Minutes / 3 Minutes	Enable or Configure the Super I/O Watchdog (if the Super I/O Used supports it, otherwise this item will not be available)

4.3.14 INT/IRQ configuration submenu

Menu Item	Options	Description
INT A IRQ / INT B IRQ / INT C IRQ / INT D IRQ / INT E IRQ / INT F IRQ / INT G IRQ / INT H IRQ	3 / 4 / 5 / 6/ 7 / 10 / 11 / 14 / 15	Allows the selection of the IRQ o be assigned to single PCI INT lines

4.4 Security menu

Menu Item	Options	Description
Select TPM Device	Disabled TPM 1.2 TPM 2.0	Allow to disable or configure properly optional external TPM devices interfaced to LPC Bus on the Carrier Board
Set Supervisor Password		Install or Change the password for supervisor. Length of password must be greater than one character.
Power on Password	Enabled / Disabled	Available only when Supervisor Password has been set. Enabled: System will ask to input a password during P.O.S.T. phase. Disabled: system will ask to input a password only for entering Setup utility
USB Disks Signature Option	See Submenu	Allow to enable or disable USB boot from signed USB disks only

4.4.1 USB Disk Signature Option submenu

Menu Item	Options	Description
USB Disks Signature Check	Enabled / Disabled	Enable the USB disk signature check. When enabled, if the USB disk used is not signed it will be removed from the boot devices list.
One Time Signature Check Disable	Enabled / Disabled	One time disable of USB disk signature check. When enabled, then for the subsequent boot only the USB disk signature will be automatically disabled.
Signature Byte 0	0 ÷ 255	Set the value for byte 0 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 1	0 ÷ 255	Set the value for byte 1 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 2	0 ÷ 255	Set the value for byte 2 of USB disks signature. The disk's signature check is always on 4 bytes.
Signature Byte 3	0 ÷ 255	Set the value for byte 3 of USB disks signature. The disk's signature check is always on 4 bytes.
USB Password	State Unknown / Installed / Not Installed	This item shows the state of USB Disk Password for Boot
Set USB Disks Password		When a USB Disk password is set, the system will first check if the USB disk is signed. If it is not signed, then the system will ask for a password, in order to continue booting from the USB disk.

4.5 Power menu

Menu Item	Options	Description
Advanced CPU Control	See submenu	These items control various CPU parameters
EC Watchdog configuration	See submenu	Watchdog Configuration Settings
Thermal Zone configuration	See submenu	Thermal Zone Configuration: Active and Passive Cooling Settings.
Wake on PME	Enabled / Disabled	Determines whether the system must wake up or not when the system power is off and occurs a PCI Power Management Enable wake-up event (e.g. to enable Wake on LAN feature).
LID_BTN# Configuration	Force Open Force Closed Normal Polarity Inverted Polarity	Configure LID_BTN# Signal as always open or closed (i.e., Force Open / Force Closed), no matter the pin level, or configures the signal polarity: “Normal Polarity” means the signal goes High when open, “Inverted Polarity” means the signal goes Low when open
LID_BTN# Wake Configuration	No Wake Only From S3 Wake From S3/S4/S5	This item can be changed only when “LID_BTN# Configuration” is not set to Force Open or Force Closed. Configure LID_BTN# Wake capability. According to the pin configuration, when the LID is open it can cause a system wake from a sleep state
Batteryless Operation	Disabled / Enabled	Enable this option in case the CMOS Battery is not present
Power Fail Resume Type	Always ON Always OFF Last State	Determine the System Behavior after a power failure event. In case the option is “Always ON”, the board will start every time the power supply is present. When the option is “Always OFF”, the board will not start automatically when the power supply returns. Finally, if this option is set to “Last State”, the board will remember the state it had when the power supply went down: so, if the board was on, it will start again when the power returns, and will remain off if the board was in this state when the power went down.

4.5.1 Advanced CPU control submenu

Menu Item	Options	Description
Use XD Capability	Enabled / Disabled	Enable or disable processor XD (Execute Disable) capability, it allows to enable or disable the hardware feature needed for data execution prevention
Limit CPUID Max Value	Enabled / Disabled	Set this option to enabled for use with older O.S. that are not able to manage the CPUID value higher than 03h, which was typical for Intel® Pentium 4 with Hyper Threading Technology Leave disabled for newer O.S. able to manage actual CPUID value.
Bi-Directional PROCHOT#	Enabled / Disabled	PROCHOT# is the signal used to start thermal throttling. This signal can be driven by any processor cores' to signal that the processor will begin thermal throttling. If bi-directional signaling is enabled, then external components can also drive PROCHOT# signal in order to start throttling.
VTX-2	Enabled / Disabled	Enable or Disable Intel® Virtualization Technology, allowing hardware-assisted virtual machine management.
TM1 and TM2	Enabled / Disabled	Enable or Disable TM1 and TM2 Thermal management modes.
AESNI Feature	Enabled / Disabled	Enable or Disable AESNI (Advanced Encryption Standard New Instructions) set of instructions, which are used to improve the speed of applications performing encryption and decryption using the Advanced Encryption Standard (AES).
Active Processor Cores	1 / 2 / 3 / ALL	Number of cores to enable in each processor package. 1 means that multicore processing is disabled.
P-States (IST)	Enabled / Disabled	Enable or disable processor management of performance states (P-states)
Boot Performance Mode	Max Performance Low Power	Only available when P-states are enabled Allows to select which performance state must be set by BIOS before starting OS loading.
Turbo Mode	Auto / Enabled / Disabled	Only available when P-states are enabled Enable processor Turbo Mode
Force CPU Speed	Disabled *List of speeds supported by the SOC used*	Only available when P-states are enabled Force CPU speed After boot. When this feature is enabled, P-State APCI Table will be disabled. The list of the speeds shown depends on the SOC mounted on the module
C-States	Enabled / Disabled	Enable processor idle power saving states (C-States).
Max C-States	C1 / C6 / C7	Allows selection of the maximum C-State that must be supported by the OS.

4.5.2 EC Watchdog Configuration submenu

Menu Item	Options	Description
Watchdog Status	Enabled / Disabled	Enable or Disable the Watchdog Timer mechanism. When enabled, all the following items can be set.
Action on Event Time-Out Expiration	Raise WDT Signal Power Button Pulse None	Select the action that will performed when the Watchdog event time-out expires
Action on Reset Time-Out Expiration	Watchdog Reset action Power Button Override Raise WDT Signal	Select the action that will performed when the Watchdog Reset time-out expires
Watchdog Delay	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes of delay, after system power up, before the watchdog Event timeout starts counting. During the delay timeout, a refresh operation will immediately trigger to normal operations.
Event Time-Out	0 / 1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the Event action triggers. A refresh will restart this timeout
Reset Time-Out	1 / 2 / 4 / 8 / 16 / 32 / 64	It specifies the minutes without being refreshed before the reset action triggers. A refresh will restart to the beginning of the event Timeout.

4.5.3 Thermal Zone configuration submenu

Menu Item	Options	Description
Critical temperature (°C)	95 / 100 / 105 / 110 / 115	Use this item to set the maximum temperature that the CPU can reach. Above this temperature value, the system will perform a critical shutdown
Passive Cooling temperature (°C)	70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Use this item to set the temperature threshold for the CPU. Above this threshold, an ACPI aware OS will start to lower the CPU frequency.
AC0 Temperature (°C)	80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the highest temperature above which the onboard fan must work always at Full Speed
AC1 Temperature (°C)	55 / 60 / 65 / 70 / 75 / 80 / 85 / 90 / 95 / 100 / 105 / 110 / 115	Select the lowest temperature under which the onboard fan must be OFF.
FAN Duty Cycle (%) Above AC1	50 / 75 / 100	Use this item to set the Duty Cycle for the fan when the CPU temperature is between AC1 and AC0 threshold. Above AC0, the man will run at full speed.

4.6 Boot menu

Menu Item	Options	Description
Boot type	Dual boot Type Legacy Boot Type UEFI Boot Type	Allows to select if the OS must be booted using Legacy Boot Mode, UEFI Boot mode or indifferently using both modalities (depending on the OS)
Quick Boot	Enabled / Disabled	Skip certain tests while booting. This will decrease the time needed to boot the system.
Quiet Boot	Enabled / Disabled	Disables or enables booting in Text Mode.
Display ESC Key Strings	Enabled / Disabled	Display or Hide the “ESC key” strings during the BIOS boot. Disabling this configuration, no information on how to enter Setup Configuration Utility will be displayed.
Display Boot Logo	Enabled / Disabled	Enable or display the visualization of a logo during Boot phase
Logo persistence Time (s)	0 ÷ 10	This submenu is available only when “Display Boot Logo” is set to Enabled. Forced wait time in seconds during the boot logo visualization. 0 means boot as fast as possible. Even with 0 wait time. UEFI OSes supporting BGRT table will display the logo while booting.
Network Stack	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “UEFI Boot type” or “Dual Boot type”. When enabled, this option will make available the following Network Stack services: Windows 8 BitLocker Unlock UEFI: IPv4/IPv6 PXE Legacy: PXE OpROM
PXE Boot Capability	Disabled UEFI: IPv4 Legacy	This submenu is available only when “Network Stack” is Enabled Specifies the PXE (Preboot Execution Environment) Boot possibilities. When Disabled, Network Stack is supported For UEFI, it is possible to support IPv4, IPv6 or both of them In Legacy mode, only Legacy PXE OpROM is supported
PXE Boot to LAN	Enabled / Disabled	This submenu is available only when “Boot Type” is set to “Legacy Boot type”. Disables or enables the possibility for the PXE to perform the boot from LAN.
Power Up in Standby Support	Enabled / Disabled	Disable or enable Power Up in Standby Support. The PUIS feature set allows devices to be powered-up in the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot options	First / Last / Auto	Specifies the position in Boot Order for Shell, Network and Removable Disks
ACPI selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0	Using this menu item is possible to select to which specifications release the ACPI tables must be compliant.

CD/DVD Rom Boot	Enabled / Disabled	Disables or enables booting from CD/DVD
Floppy Disk Boot	Enabled / Disabled	Disables or enables booting from Floppy Disks.
USB Boot	Enabled / Disabled	Disables or enables booting from USB boot devices.
EFI/Legacy Device Order	EFI device first Legacy device first Smart Mode	This submenu is available only when “Boot Type” is set to Dual Boot Type. Determine if boot must happen first through EFI devices or through legacy devices, or in Smart Mode.
Windows® 8 Fast Boot	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type. If enabled, the system firmware does not initialize keyboard and check for firmware menu key.
USB Hot Key Support	Enabled / Disabled	This submenu is available only when “Boot Type” is set to UEFI Boot Type and “Windows® 8 Fast Boot” is Enabled. Enable or disable the support for USB HotKeys while booting. This will decrease the time needed to boot the system
Timeout	0 ÷ 60	The number of seconds that the firmware will wait before booting the original default boot selection.
Reset On No Boot Device Found	Enabled / Disabled	When this option is enabled, the system will reset itself each time that doesn’t find any valid boot device, instead of waiting indefinitely that a Boot device is plugged.
Touch Controller To Enter SCU	Enabled / Disabled	When this option is enabled, it will be possible to use a Touch screen to enter the Setup Configuration Utility, avoiding using additional external keyboard. The Touch detection will be used as hotkey
Legacy Device Fixed Order	Enabled / Disabled	Disable or enable fixed boot order for physical devices. Takes effect at the next boot of the board
Fixed Legacy Boot Order Settings	See Submenu	This submenu is available only when “Legacy Device Fixed Order” is enabled. Allows fixing the boot order by physical devices.
EFI	See Submenu	This submenu is available only when “Boot Type” is not set to “Legacy Boot type”. Entering the submenu, will show a list of EFI boot devices. Use F5 and F6 key to change order for boot priority.
Legacy	See Submenu	This submenu is available only when “Boot Type” is not set to “UEFI Boot type”. Allows setting of Legacy Boot Order

4.6.1 Fixed Legacy Boot Order Settings submenu

Menu Item	Options	Description
First / Second / Third / Fourth / Fifth / Sixth / Seventh	LAN / EHCI / XHCI / SATA0 / SATA1 / eMMC / SD / NONE	Allows selecting the boot order of the possible boot devices. If it is necessary to force the boot from a specific device only, please set is as a first boot device, and set to NONE all other devices.

4.6.2 Legacy submenu

Menu Item	Options	Description
Boot Menu	Normal / Advance	When set to Normal, this submenu will allow configuring all possible options for Legacy boot. When set to Advance, it will be possible to configure Boot Order only for bootable devices found in the system
Boot Type Order	Floppy Disk Boot Hard Disk Drive CD/DVD-ROM Drive USB Other	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will allows selecting the boot from different devices. Use the + and - Keys to change the boot order priority
Hard Disk Drive	*List of HD Drives found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority
USB	*List of USB Disks found connected*	This voice will be selectable only when “Boot menu” is set to “Normal”. The list shown under this item will show different Disk drives found connected to the module, therefore changing the boot priority for them. Use the + and - Keys to change the boot order priority

4.7 Exit menu

Menu Item	Options	Description
Exit Saving Changes		Exit system setup after saving the changes. F10 key can be used for this operation.
Save Change Without Exit		Save all changes made, but doesn't exit from setup utility.
Exit Discarding Changes		Exit system setup without saving any changes. ESC key can be used for this operation.
Load Optimal Defaults		Load Optimal Default values for all the setup items. F9 key can be used for this operation.
Load Custom Defaults		Load Custom Default values for all the setup items.
Save Custom Defaults		Save Custom Default values for all the setup items.

Chapter 5.
Appendices

- Thermal Design

5.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COMe-A41-CT6 module, offer to the user very good performances in minimal spaces, therefore allowing the system's minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsink with fan in some situation can represent the cooling solution. Indeed, when using COMe-A41-CT6 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with FAN could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COMe-A41-CT6 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
MA41-DISS-1-PK	COMe-A41-CT6 Heat Spreader (passive), packaged
MA41-DISS-3-PK	COMe-A41-CT6 Active Heatsink with FAN, packaged

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