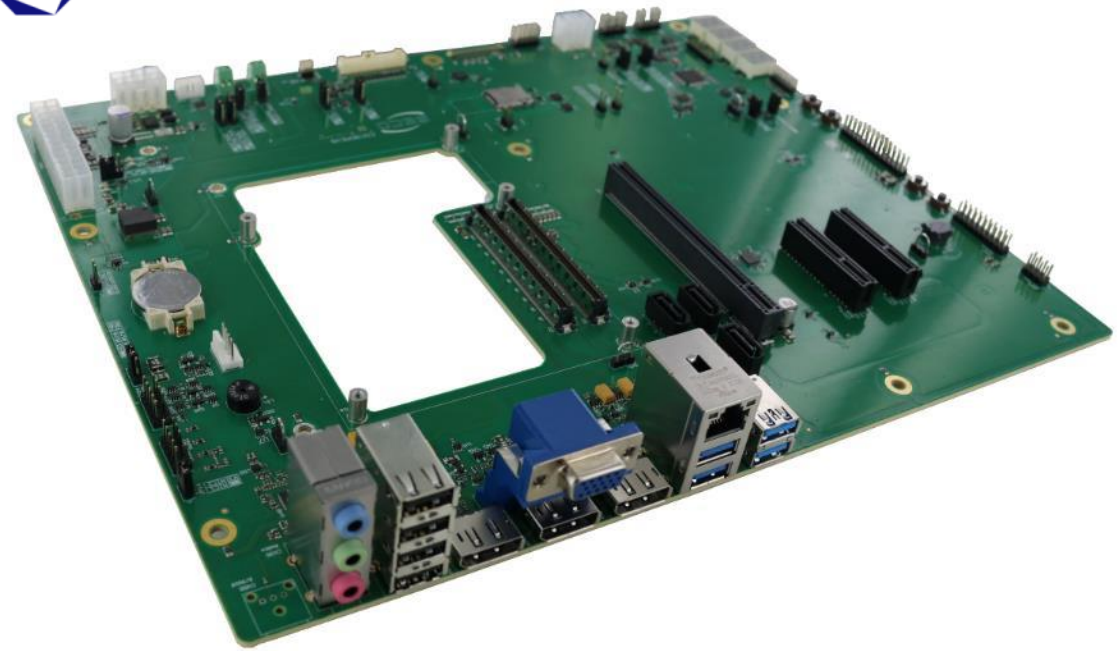
Com express

User Manual



CCOMe-C96

Carrier Board for COM-Express™ Type 6 Module
on ATX form factor

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	2nd August 2021	First release	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at https://www.seco.com/ (registration required).

Our team is ready to assist you.

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Chapter 1.
INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
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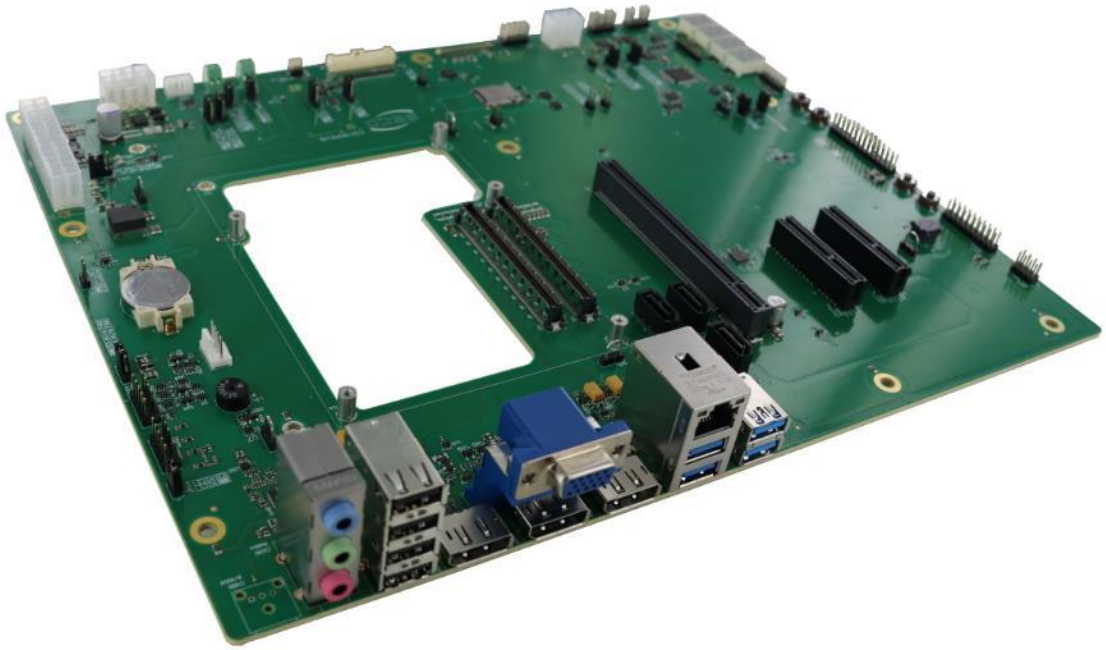
- Safety Policy
- Terminology and definitions
- Reference specifications



1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/eu/support/online-rma.html (Online RMA). The RMA Authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and must accompany the returned item.

If any of the above mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following after a technical analysis, the supplier will verify if all the requirements for which a warranty service applies are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty.

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit https://www.seco.com to receive the latest information on the product. In most cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 340434
- Repair centre: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be released within 1 working day (only for on-line RMA requests).

1.4 Safety

The CCOMe-C96 board uses only extremely-low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The CCOMe-C96 board, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

Whenever handling a CCOMe-C96 board, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The CCOMe-C96 board is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Safety Policy

In order to meet the safety requirements of EN62368-1:2014 standard for Audio/Video, information and communication technology equipment, the CCOMe-C96 Carrier Board shall be:

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the board never exceeds 100 W, even in worst-case fault);
- used inside an enclosure provided with the symbol IEC 60417-5041(element 1a according to clause 9.5.2 of the IEC 62368-1) on the external part;
- installed inside an enclosure compliant with all applicable IEC 62368-1 requirements;

The manufacturer which includes a CCOMe-C96 Carrier Board in his end-user product shall:

- verify the compliance with B.2 and B.3 clauses of the EN62368-1 standard when the module works in its own final operating condition
- prescribe temperature and humidity range for operating, transport and storage conditions;
- prescribe to perform maintenance on the board only when it is off and has already cooled down;
- prescribe that the connections from or to the board have to be compliant to ES1 requirements;
- the board in its enclosure must be evaluated for temperature and airflow considerations.

1.8 Terminology and definitions

ACPI	Advanced Configuration and Power Interface, an open industrial standard for the board's devices configuration and power management
BIOS	Basic Input / Output System, the Firmware Interface that initializes the board before the OS starts loading
CEC	Consumer Electronics Control, an HDMI feature which allows controlling more devices connected together by using only one remote control
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DP	Display Port, a type of digital video display interface
DVI	Digital Visual interface, a type of digital video display interface
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
HD Audio	High Definition Audio, most recent standard for hardware codecs developed by Intel® in 2004 for higher audio quality
HDMI	High Definition Multimedia Interface, a digital audio and video interface
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
LPC Bus	Low Pin Count Bus, a low speed interface based on a very restricted number of signals, deemed to management of legacy peripherals
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
N.A.	Not Applicable
N.C.	Not Connected
OS	Operating System
PCI-e	Peripheral Component Interface Express
PWM	Pulse Width Modulation
PWR	Power
SATA	Serial Advance Technology Attachment, a differential half duplex serial interface for Hard Disks
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows use the use of the same SD interface to drive different Input/Output

	devices, like cameras, GPS, Tuners and so on
SIM	Subscriber Identity Module, a card which stores all data of the owner necessary to allow him accessing to mobile communication networks
SM Bus	System Management Bus, a subset of the I2C bus protocol dedicated to communication with devices for system management, like a smart battery and other power supply-related devices
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line
TBM	To be measured
TMDS	Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces
TTL	Transistor-transistor Logic
UIM	User Identity Module, an extension of SIM modules.
USB	Universal Serial Bus
V_REF	Voltage reference Pin

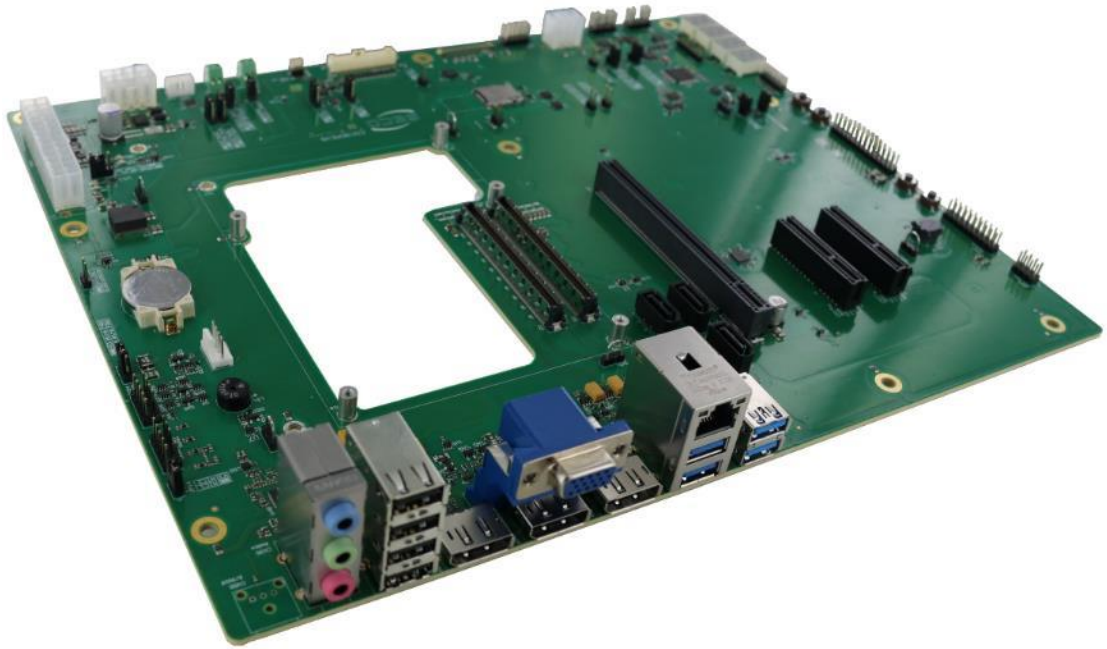
1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
ACPI	http://www.acpi.info
Com Express™	https://www.picmg.org/openstandards/com-express/
Com Express™ Carrier Design Guide	https://www.picmg.org/wp-content/uploads/PICMG_COMDG_2.0-RELEASED-2013-12-061.pdf
DDC	https://www.vesa.org/
DP, eDP	https://www.vesa.org/
Ethernet	http://standards.ieee.org/about/get/802/802.3.html
HD Audio	http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/high-definition-audio-specification.pdf
HDMI	http://www.hdmi.org/index.aspx
I2C	http://www.nxp.com/docs/en/user-guide/UM10204.pdf
Intel® Front Panel I/O connectivity DG	http://www.formfactors.org/developer/specs/A2928604-005.pdf
LPC Bus	http://www.intel.com/design/chipsets/industry/lpc.htm
LVDS	http://www.ti.com/lit/ug/snla187/snla187.pdf
PCI Express	http://www.pcisig.com/specifications/pciexpress
SATA	https://www.sata-io.org
SD Card Association	https://www.sdcard.org
SM Bus	http://www.smbus.org/specs
TMDS	http://www.latticesemi.com/view_document?document_id=38351
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb20_docs/usb_20_080117.zip
USB 3.0	http://www.usb.org/developers/docs/usb_31_080117.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram



2.1 Introduction

CCOMe-C96 is a carrier board, designed in ATX form factor, intended for the use with COM-Express™ Type 6 CPU modules.

COM-Express™ is an open industry standard defined specifically for COMs (computer on modules). Its definition provides the ability to make a smooth transition from legacy parallel interfaces to the newest technologies based on serial buses available today.

COM Express™ CPU modules integrate all the core components of a typical PC-like architecture, and make all interface available through two standardized connectors, so that COM Express™ modules become scalable. This means that once an application has been created, there is the ability to diversify the product range through the use of different performance class or form factor size modules.

Baseboard designers can use just the I/O interfaces that really need, providing, on the carrier board, the routing to the adequate interface connectors.

This versatility allows the designer to create a dense and optimised package, which results in a more reliable product while simplifying system integration.

CCOMe-C96 board can be used both as an evaluation module, to test the functionality of your COM-Express™ module and design an application specific carrier board for it, or as a complete carrier board, already suited for standard purposes, with a small space consumption.

In any case, the solutions so realised is fully scalable, and allows to the user to keep his own-designed system continuously up-to-date, since the system can be updated simply replacing the COM-Express™ module with a newer one, just unplugging the module and replacing it, without the need of redesigning it.

The robust thermal and mechanical concept, combined with extended power-management capabilities, is perfectly suited for all applications.

2.2 Technical Specifications

Supported Modules
- COM Express™ Type 6 compliant modules

Mass Storage interfaces
- 4x SATA 7p M connectors
- µSD Card slot (interface multiplexed with GPIO header)

Video Interfaces
- 3 x DP++ connectors
- VGA connector
- LVDS 24-bit Single/Dual Channel Connector
- LVDS External EDID flash socket
- eDP 4-lanes 40 poles VESA connector

Audio
- On-board HD Audio Codec (Cirrus Logic CS4207)
- Mic In + Line Out internal pin header
- HD Audio Jacks
- S/PDIF Out Optical connector

USB
- 4 x USB 3.1 Host ports on Type-A sockets
- 4 x USB 2.0 Host ports on Quad Type-A sockets

Networking
- 1x RJ-45 connector

PCI-e
- 2x PCI-e x4 Slots
- 1x PCI-e x16 Slot

Serial Ports
- 2 x RS-232 / RS-422 / RS-485 ports on internal pin header (from carrier board's LPC Dual UART controller)
- 2 x RS-232 ports on dedicated pin header (from module)

Other Interfaces
- 4 x GPI + 4 x GPO pin header (interface multiplexed with µSD slot)
- SPI Flash header
- Button / LEDs front panel header
- 4-pin tachometric FAN connector
- I2C + SM Bus on feature Pin header
- FuSa Header
- I2C Flash Socket
- JTAG connector
- LPC internal header
- USB overcurrent header
- SM Bus Smart Battery Connector
- 4 x 7-segment LCD displays for POST codes
- LPC/eSPI internal header

Power supply: ATX 24 poles connector for carrier board working only
- Auxiliary 12V connector for carrier board working only
- 12 V_{DC} power in connector for COM Express™ module's working
- Coin-cell holder for RTC

Operating temperature: 0°C ÷ +60°C * (Commercial version)

Dimensions: 305x244mm (ATXform factor, 12" x 9.6")

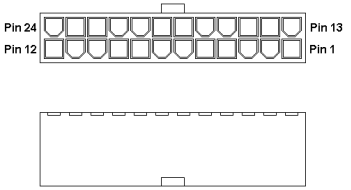
! ** Temperature ranges indicated mean that all components available onboard are certified for working with a Tcase included in these temperature ranges. This means that it is customer's responsibility to ensure that all components' Tcases remain in the range above indicated. Please also check paragraph 4.1.*

2.3 Electrical Specifications

CCOMe-C96 board needs to be supplied using a standard ATX Power Supply, which can, however, also be configured to work in AT mode.

ATX/ AT Power Connector – CN10			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_RUN	13	+3.3V_RUN
2	+3.3V_RUN	14	---
3	GND	15	GND
4	+5V_RUN	16	PS_ON#
5	GND	17	GND
6	+5V_RUN	18	GND
7	GND	19	GND
8	PWR_OK_ATX	20	---
9	+5V_ALW	21	+5V_RUN
10	+12V_RUN	22	+5V_RUN
11	+12V_RUN	23	+5V_RUN
12	+3.3V_RUN	24	GND

Power Connector CN10 is type Molex Mini-Fit Jr. connector, p/n 39-28-1243, or equivalent, with the pin-out indicated in the table here on the left (it is the standard 24-pin ATX pin-out).



Mating Connector, MOLEX p/n 39-01-2240 or equivalent, with female crimp terminal MOLEX series 5566.

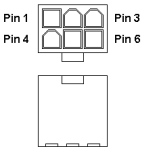
PS_ON#: this signal is present only if the board is configured, via CN11 and J2, to work in ATX mode. If working in AT mode, this pin is connected directly to Ground.

Power connector can be set to work in ATX mode or AT mode by using dedicated jumpers CN11 and J2, which are a standard pin headers, P2.54mm, 1x3 pin.

CN11 position	J2 position	Power mode
2-3	Not Care	AT mode
1-2	1-2	ATX mode
1-2	2-3	AT mode

Auxiliary Power Connector – CN7			
Pin	**Signal**	**Pin**	**Signal**
1	+12V_RUN	5	GND
2	+12V_RUN	6	GND
3	+12V_RUN	7	GND

The board has an Auxiliary Power connector CN7 providing +12V_RUN for the carrier board section only, in case multiple PCI-e modules are connected.



CN7 is 6-poles connector, type MOLEX mini-Fit Jr. p/n 39-28-1063 or equivalent.

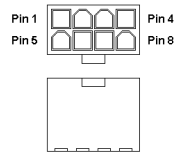
Mating Connector, MOLEX p/n 39-01-2060 or equivalent, with female crimp terminal MOLEX series 5566.

CPU Power Connector – CN8			
Pin	Signal	Pin	Signal
1	GND	5	+12V_RUN
2	GND	6	+12V_RUN
3	GND	7	+12V_RUN
4	GND	8	+12V_RUN

The board has a CPU Power Connector CN8 providing +12V_RUN for the COM Express™ module only.

CN8 is a Molex Mini-Fit jr. 8 poles connector, p/n 39-28-1083 or equivalent.

Mating Connector, MOLEX p/n 39-01-2080 or equivalent, with female crimp terminal MOLEX series 5566.



The use of wires with section 18 AWG is recommended, in order to ensure the proper amperage of the power section.

JP2 position	+5V_ALW Current monitor selector
Not inserted	Current measurement enabled
Inserted	Current measurement disabled

The power consumption on +5V_ALW can be monitored by removing 2 way jumper JP2 and inserting a tester set as ammeter.

Alternatively, the consumption on +5V_ALW can be monitored by inserting a tester set as ammeter between pin 1 and 2 of +5V_ALW Sense Connector CN4.

CN4 is a dedicated 2 position Wire to Board Terminal Block, type Wurth p/n 691210910002.

CN3 position	Power Ok management
1-2	PSU PWR_OK enabled
2-3	PWR_OK always high

The COM Express™ card edge connector has a PWR_OK signal from main power supplied by Carrier Board to the module, indicating that all the power supplies to the Module are stable within specified ranges. The Module will typically not power up until the PWR_OK signal goes active.

CN3 is a standard pin header, P2.54mm, 1x3 pin, dedicated to manage this power status signal for the Module. For normal operation, set the jumper in 1-2 position, otherwise set in 2-3 position to fix its level high and have it always activated.

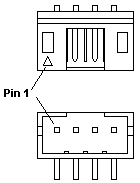
Diode LED D17 is present on Carrier Board to notify the system has been correctly powered-up, directly driven through an High-Speed Buffer by PWR_OK signal.

Another diode LED D16, complementary to D17, is used to notify the Reset Output from Module to Carrier Board, directly driven through an High-Speed Buffer by CB_RESET# signal.

2.3.1 Smart Battery SM Bus Connector

Smart Battery SM Bus Connector – CN29			
Pin	**Signal**	**Pin**	**Signal**
1	SB_SMB_CLK	3	SMB_ALERT#
2	SB_SMB_DAT	4	GND

The SM bus coming from COM Express™ module is carried directly both to the Feature header (see par.3.3.8) and to a JST 4-pin connector CN29, p/n B4B-PH-K-S(LF)(SN), or equivalent, which can be used for the connection of external Smart battery controllers. Pinout as indicated in the left table.



SB_SMB_CLK: Smart Battery System Management bus bidirectional clock line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_CK signal

SB_SMB_DAT: Smart Battery System Management bus bidirectional data line, +3.3V_ALW electrical level with 10kΩ pull up resistor derived by SMB_DAT signal

SMB_ALERT#: System Management Bus Alert, active low input to the module that can be used to generate an Interrupt or to wake the system.

2.3.2 RTC Battery

For the occurrences when the System (Carrier board + COM Express™ module) is not powered with an external power supply, on board there is a RTC Coin Cell Battery holder CN9, for the use of standard coin battery type CR2032 with a nominal capacity of 220mAh, to supply, with a 3V voltage, the Real Time Clock and CMOS memory mounted on the COM Express™ module.

The batteries should only be replaced with devices of the same type. Always check the orientation before inserting and make sure that they are aligned correctly and are not damaged or leaking.

! CAUTION: handling batteries incorrectly or replacing with not-approved devices may present a risk of fire or explosion.

Never allow the batteries to become short-circuited during handling. Batteries supplied with C96 board are compliant to requirements of European Directive 2006/66/EC regarding batteries and accumulators. When putting out of order C96 board, remove the batteries from the board in order to collect and dispose them according to the requirement of the same European Directive above mentioned. Even when replacing the batteries, the disposal has to be made according to these requirements.

CN6 position	RTC Battery enable
1-2	Battery disconnected
2-3	Battery connected
NO jumper	Current measurement

It is possible to monitor the consumption on VCC_RTC battery by removing the jumper from CN6 connector and inserting a tester in series set as ammeter between 2-3 position.

Alternatively, the consumption on VCC_RTC can be monitored by inserting a tester set as ammeter between pin 1 and 2 of RTC Battery Sense Connector CN5.

CN5 is a dedicated 2 position Wire to Board Terminal Block, type Wurth p/n 691210910002

RTC battery can be enabled/disabled using dedicated jumper on CN6, which is a standard pin header, P2.54mm, 1x3 pin.

JP1 position	Battery Low Indicator enable
Not inserted	Indicator disabled
Inserted	Indicator enabled

The RTC battery voltage level is monitored through a comparator inside the board. Battery low status signal (BATLOW#) is carried to COM-express™ module to be managed.

JP1 is a 2-way jumper to enable/disable this indicator.

2.3.3 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

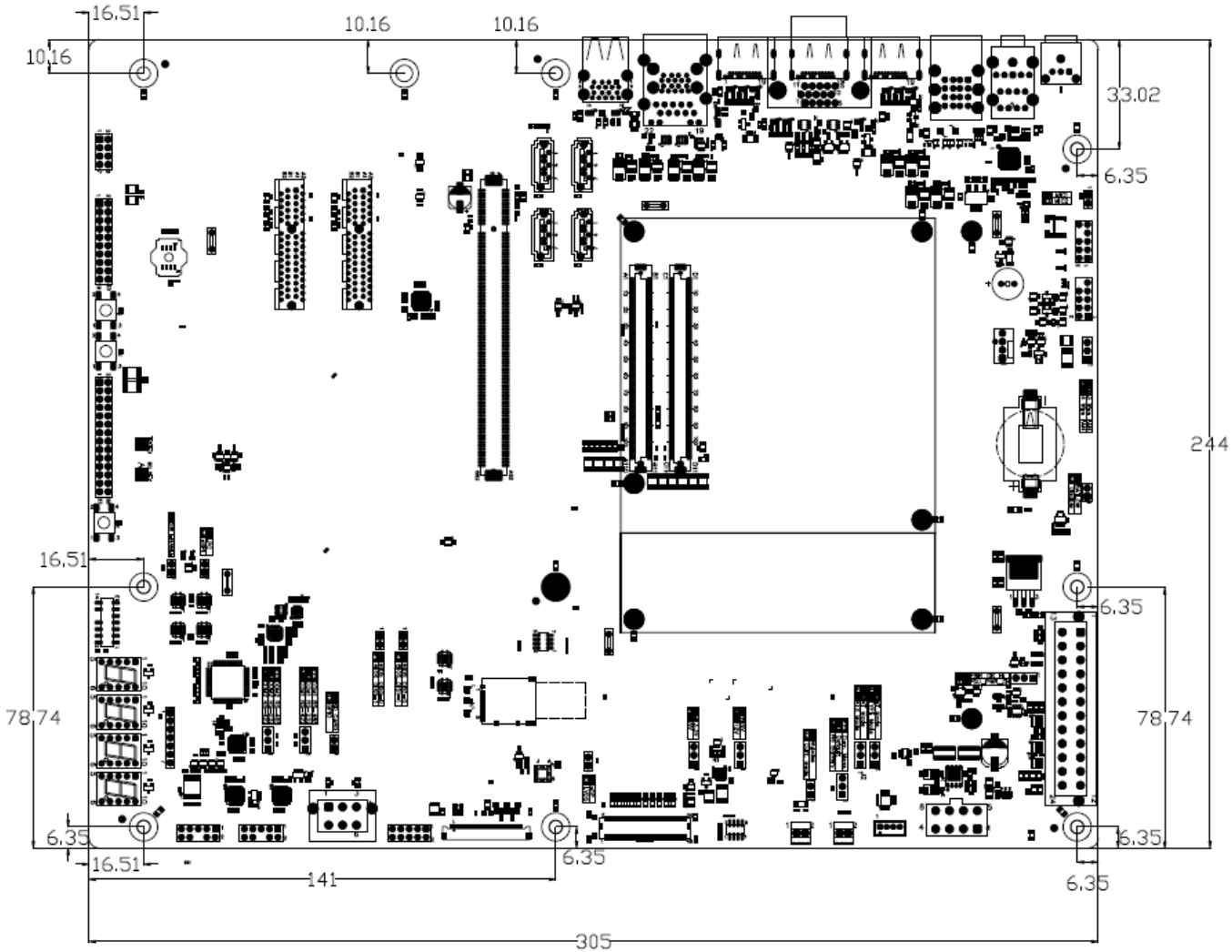
_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

2.4 Mechanical Specifications

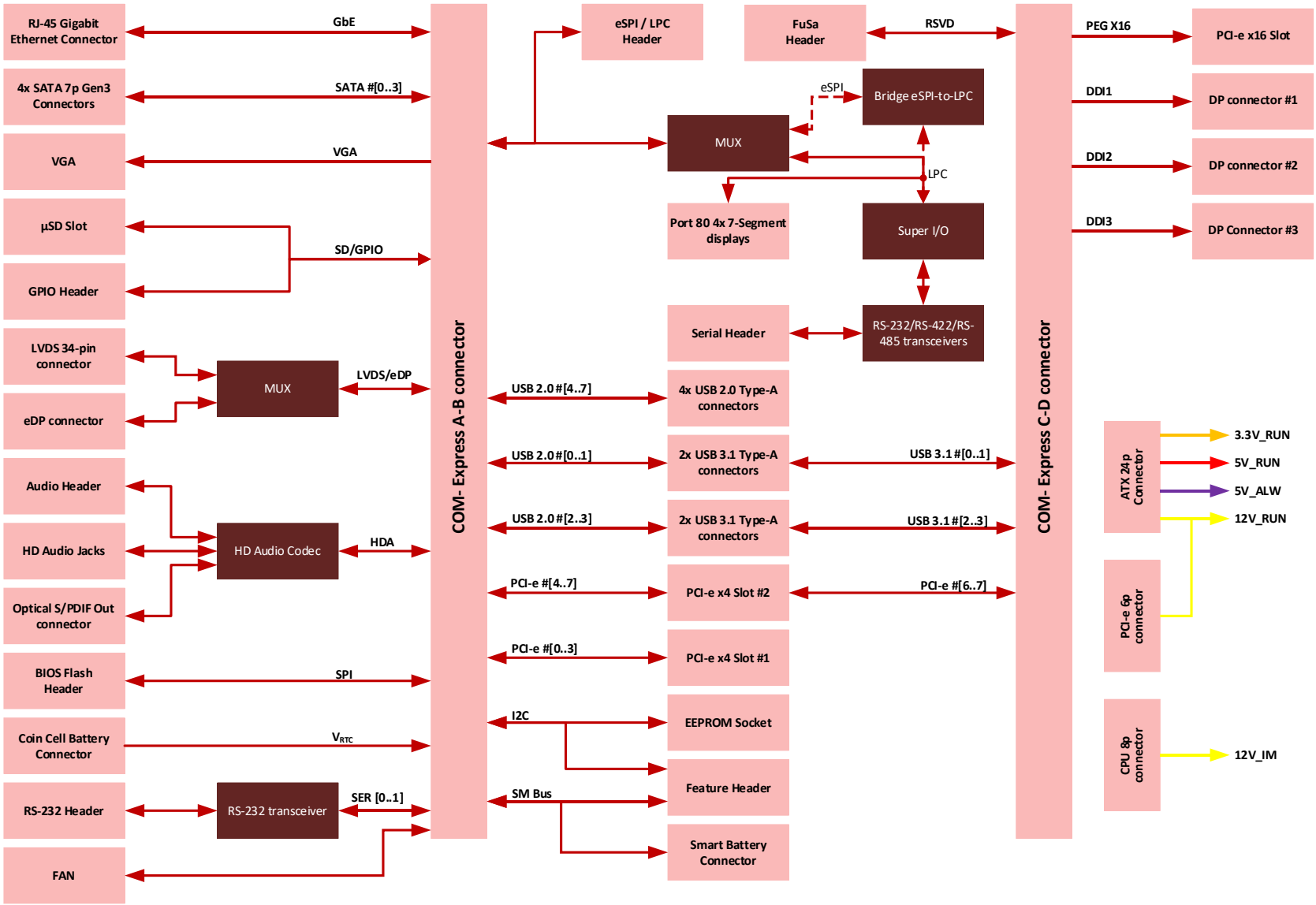
According to ATX form factor, board dimensions are 305 x 244 mm (12” x 9.6”).

The printed circuit of the board is made of twelve layers, some of them are ground planes, for disturbance rejection.

In order to fix the COM Express™ module to the carrier board, on CCOMe-C96 have been soldered six metallic spacers, height 8mm, 2.5mm diameter.

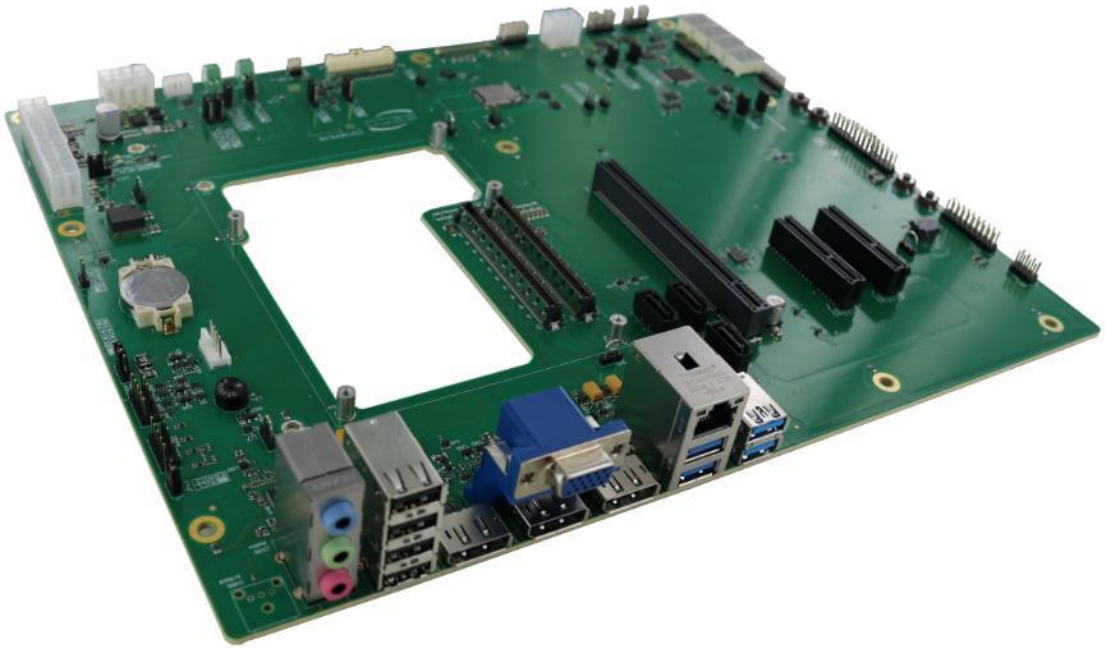


2.5 Block Diagram



Chapter 3. CONNECTORS

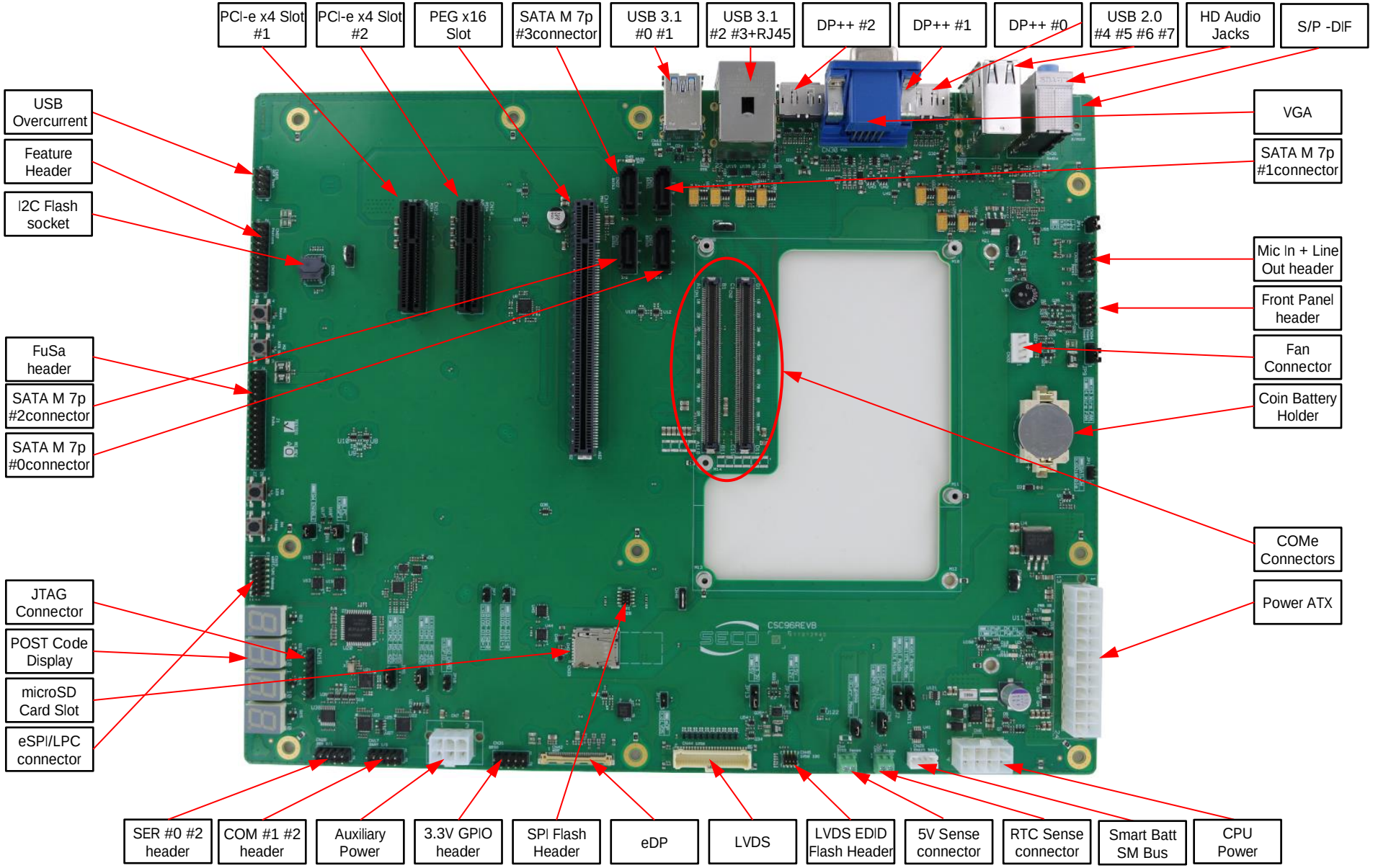
- Connectors placement
- Connectors overview
- Connectors description



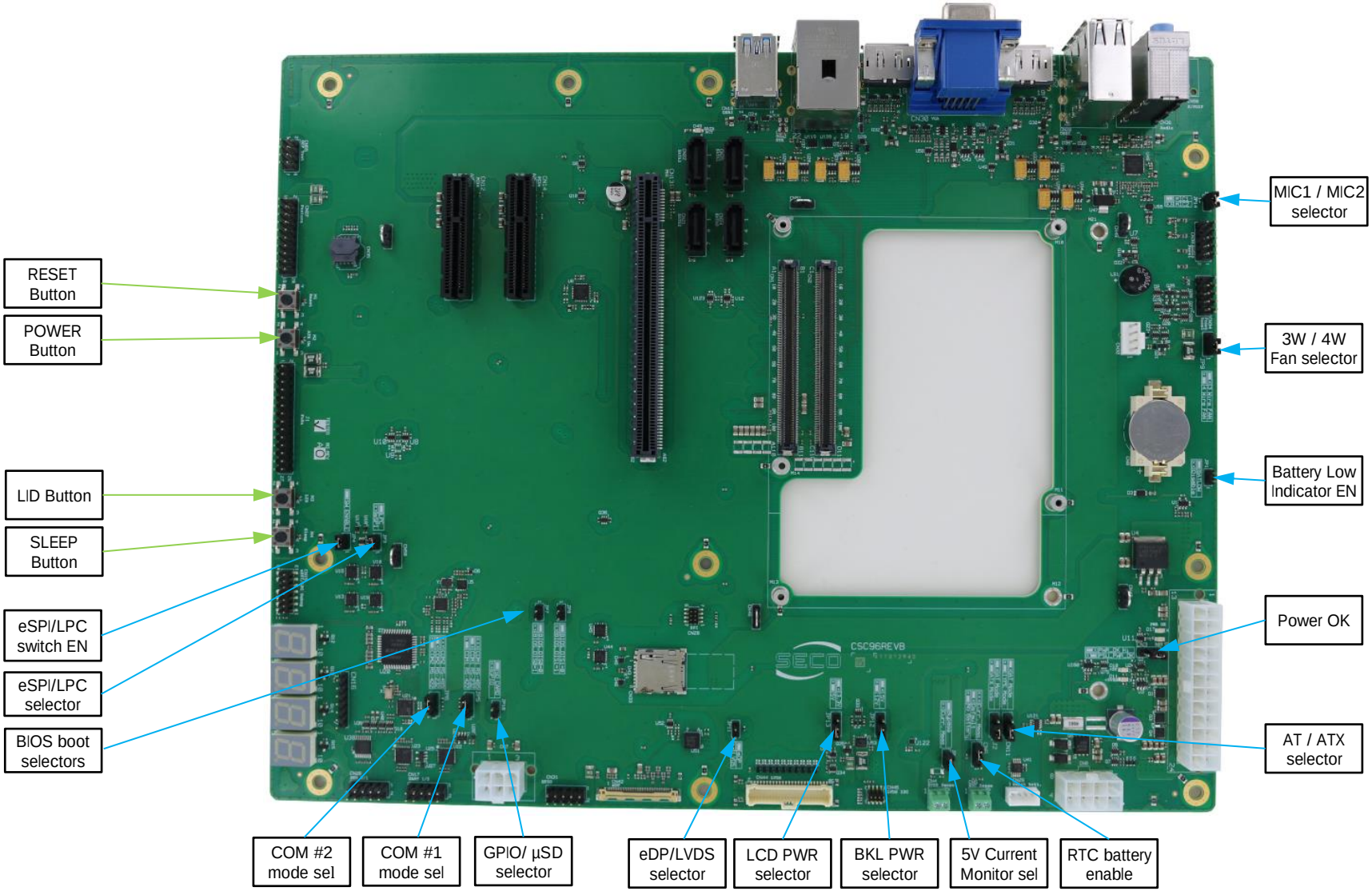
3.1 Connectors placement

On CCOMe-C96 carrier board, there are several connectors. Some of them are standard connectors, like Display Port, Gigabit Ethernet, USB ports, and are placed on the same side of the board, so that they can be placed on a panel of a possible enclosure.

In the following picture it is possible to see the position of each connector.



JUMPER POSITION



3.2 Connectors overview

3.2.1 Connectors list

Name	Description	Name	Description
CN1	Com Express™, A-B rows Connector	CN28	External BIOS SPI Flash Header
CN2	Com Express™, C-D rows Connector	CN29	Smart Battery SM Bus Connector
CN4	+5V_ALW Sense Connector	CN30	VGA Connector
CN5	RTC Battery Sense Connector	CN31	GPIO pin Header
CN7	Auxiliary Power Connector	CN32	FAN Connector
CN8	CPU Power Connector	CN33	microSD Card Slot
CN9	RTC Coin Cell Battery Connector	CN34	Front Panel Header
CN10	Power ATX Connector	CN35	External EEPROM I2C Flash socket
CN12	PCI-e x4 slot #1	CN36	HD Audio Jacks
CN13	PCI-e Graphics (PEG) x16 slot	CN38	Mic In + Line Out internal pin Header
CN14	PCI-e x4 slot #2	CN42	eDP Connector
CN15	eSPI/LPC Debug Connector	CN44	LVDS Connector
CN16	JTAG Connector	CN45	LVDS External EDID Flash Header
CN17	COM ports Internal pin Header	CN52	DP++ #0 Connector
CN18	USB 3.1 ports #0 #1 Dual Type-A socket	CN53	DP++ #1 Connector
CN19	Combo USB 3.1 ports #2 #3 Dual Type-A socket + RJ45 Connector	CN54	DP++ #2 Connector
CN20	USB 2.0 ports #4 #5 #6 #7 Quad Type-A socket	CN55	USB Overcurrent Header
CN21	SATA M 7-p #2 Connector	CN56	S/P-DIF Out Connector
CN22	SATA M 7-p #3 Connector	J1	FuSa Header
CN24	SATA M 7-p #0 Connector		
CN25	SATA M 7-p #1 Connector		
CN26	RS-232 ports Internal pin Header		
CN27	Feature pin Header		

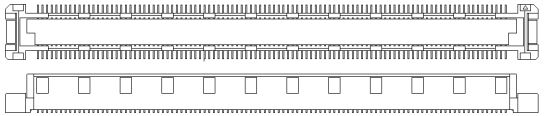
3.2.2 Jumpers and switch list

Name	Description
CN3	Power OK management
CN6	RTC Battery enable
CN11 / J2	AT/ATX mode selectors
JP1	RTC Battery Low Indicator enable
JP2	+5V_ALW Current monitor selector
JP3	eSPI/LPC selector
JP4	eSPI/LPC switch enable
JP5	COM 1 mode selector
JP6	COM 2 mode selector
JP7 / JP8	BIOS Boot selectors
JP9	FAN driver mode selector
JP10	GPIO/SD Card selector
JP11	eDP/LVDS selector
JP12	Backlight Power selector
JP13	LCD Power selector
JP14	MIC1 / MIC2 selector

3.3 Connectors description

3.3.1 COM Express™ module connectors

For the connection of COM Express™ CPU modules, on board there are two connectors, type TYCO 3-6318491-6 (220 pin dual row plug, ultra thin, 0.5mm pitch, h=8mm), as requested by COM Express™ specifications.



The pinout of these connectors will be briefly described in the following paragraphs. Please refer to COM Express™ standard for a better description of each signal.

COM Express™ Connector CN1 - Rows A & B

Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
Power Ground	GND	A1	B1	GND	Power Ground
GbEthernet Differential pair 3-	GBE0_MDI3-	A2	B2	GBE0_ACT#	GbEth Activity indicator
GbEthernet Differential pair 3+	GBE0_MDI3+	A3	B3	LPC_FRAME# / ESPI_CS0#	LPC Frame Indicator / eSPI Chip Select
GbEthernet 100Mb/s link ind.	GBE0_LINK100#	A4	B4	LPC_AD0 / ESPI_IO_0	LPC Address / Data Bus 0 eSPI Master Data Input / Output 0
GbEthernet 1000Mb/s link ind.	GBE0_LINK1000#	A5	B5	LPC_AD1 / ESPI_IO_1	LPC Address / Data Bus 1 eSPI Master Data Input / Output 1
GbEthernet differential pair 2-	GBE0_MDI2-	A6	B6	LPC_AD2 / ESPI_IO_2	LPC Address / Data Bus 2 eSPI Master Data Input / Output 2
GbEthernet Differential pair 2+	GBE0_MDI2+	A7	B7	LPC_AD3 / ESPI_IO_3	LPC Address / Data Bus 3 eSPI Master Data Input / Output 3
Not connected	N.C.	A8	B8	LPC_DRQ0# / ESPI_ALERT0#	LPC serial DMA request eSPI Alert request service signal
GbEthernet Differential pair 1-	GBE0_MDI1-	A9	B9	N.C.	Not connected
GbEthernet Differential pair 1+	GBE0_MDI1+	A10	B10	LPC_CLK / ESPI_CK	LPC Clock Output 33MHz eSPI Master Clock Output
Power Ground	GND	A11	B11	GND	Power Ground
GbEthernet Differential pair 0-	GBE0_MDI0-	A12	B12	PWRBTN#	Power Button
GbEthernet Differential pair 0+	GBE0_MDI0+	A13	B13	SMB_CK	SM Bus Clock
GbEthernet Reference Voltage	GBE0_CTREF	A14	B14	SMB_DAT	SM Bus Data
Suspend to RAM (S3) signal	SUS_S3#	A15	B15	SMB_ALERT#	SM Bus Alert signal

SATA0 Transmit Data +	SATA0_TX+	A16	B16	SATA1_TX+	SATA1 Transmit Data +
SATA0 Transmit Data -	SATA0_TX-	A17	B17	SATA1_TX-	SATA1 Transmit Data -
Suspend to Disk (S4) signal	SUS_S4#	A18	B18	SUS_STAT# / ESPI_RESET#	LPC Suspend Mode Indicator eSPI Reset
SATA0 Receive Data +	SATA0_RX+	A19	B19	SATA1_RX+	SATA1 Receive Data +
SATA0 Receive Data -	SATA0_RX-	A20	B20	SATA1_RX-	SATA1 Receive Data -
Power Ground	GND	A21	B21	GND	Power Ground
SATA2 Transmit Data +	SATA2_TX+	A22	B22	SATA3_TX+	SATA3 Transmit Data +
SATA2 Transmit Data -	SATA2_TX-	A23	B23	SATA3_TX-	SATA3 Transmit Data -
Soft Off (S5) Signal	SUS_S5#	A24	B24	PWR_OK	Power OK signal
SATA2 Receive Data +	SATA2_RX+	A25	B25	SATA3_RX+	SATA3 Receive Data +
SATA2 Receive Data -	SATA2_RX-	A26	B26	SATA3_RX-	SATA3 Receive Data -
Low Battery Status Indicator Input	BATLOW#	A27	B27	WDT	Watchdog Event indicator Output
SATA LED	SATA_ACT#	A28	B28	N.C.	Not connected
HD Audio Sync signal	AC/HDA_SYNC	A29	B29	N.C.	Not Connected
HD Audio Reset	AC/HDA_RST#	A30	B30	HDA_SDIN0	HD Audio Serial TDM Input 0
Power Ground	GND	A31	B31	GND	Power Ground
HD Audio Bit Clock	AC/HDA_BITCLK	A32	B32	SPKR	Speaker
HD Audio Serial TDM Output	AC/HDA_SDOUT	A33	B33	I2C_CK	I2C Clock
BIOS boot device select 0 signal	BIOS_DIS0#	A34	B34	I2C_DAT	I2C Data
Thermal shutdown Status Indicator Output	THRMTRIP#	A35	B35	THRM#	Thermal Alarm Input
USB Data Port 6 -	USB6-	A36	B36	USB7-	USB Data Port 7-
USB Data Port 6 +	USB6+	A37	B37	USB7+	USB Data Port 7+
USB Over Current Ports 6/7	USB_6_7_OC#	A38	B38	USB_4_5_OC#	USB Over Current Ports 4/5
USB Data Port 4 -	USB4-	A39	B39	USB5-	USB Data Port 5-
USB Data Port 4 +	USB4+	A40	B40	USB5+	USB Data Port 5+
Power Ground	GND	A41	B41	GND	Power Ground
USB Data Port 2 -	USB2-	A42	B42	USB3-	USB Data Port 3-
USB Data Port 2 +	USB2+	A43	B43	USB3+	USB Data Port 3+
USB Over Current Ports 2/3	USB_2_3_OC#	A44	B44	USB_0_1_OC#	USB Over Current Ports 0/1

USB Data Port 0 -	USB0-	A45	B45	USB1-	USB Data Port 1-
USB Data Port 0 +	USB0+	A46	B46	USB1+	USB Data Port 1+
Real Time Clock power line	VCC_RTC	A47	B47	EXCD1_PERST#	eSPI enable Input
Not Connected	N.C.	A48	B48	N.C.	Not Connected
Not Connected	N.C.	A49	B49	SYS_RESET#	Reset Button Input
LPC serial interrupt request	LPC_SERIRQ	A50	B50	CB_RESET#	Board Reset Output
Power Ground	GND	A51	B51	GND	Power Ground
PCI-E lane 5 transmit +	PCIE_TX5+	A52	B52	PCIE_RX5+	PCI-E lane 5 receive +
PCI-E lane 5 transmit -	PCIE_TX5-	A53	B53	PCIE_RX5-	PCI-E lane 5 receive -
GP Input 0 / SDIO data signal 0	GPI0/SD_DATA0	A54	B54	GPO1/SD_CMD	GP Output 1 / SDIO CMD output
PCI-E lane 4 transmit +	PCIE_TX4+	A55	B55	PCIE_RX4+	PCI-E lane 4 receive +
PCI-E lane 4 transmit -	PCIE_TX4-	A56	B56	PCIE_RX4-	PCI-E lane 4 receive -
Power Ground	GND	A57	B57	GPO2/SD_WP	GP Output 2 / SDIO WP input
PCI-E lane 3 transmit +	PCIE_TX3+	A58	B58	PCIE_RX3+	PCI-E lane 3 receive +
PCI-E lane 3 transmit -	PCIE_TX3-	A59	B59	PCIE_RX3-	PCI-E lane 3 receive -
Power Ground	GND	A60	B60	GND	Power Ground
PCI-E lane 2 transmit +	PCIE_TX2+	A61	B61	PCIE_RX2+	PCI-E lane 2 receive +
PCI-E lane 2 transmit -	PCIE_TX2-	A62	B62	PCIE_RX2-	PCI-E lane 2 receive -
GP Input 1 / SDIO data signal 1	GPI1/SD_DATA1	A63	B63	GPO3/SD_CD#	GP Output 3 / SDIO CD# input
PCI-E lane 1 transmit +	PCIE_TX1+	A64	B64	PCIE_RX1+	PCI-E lane 1 receive +
PCI-E lane 1 transmit -	PCIE_TX1-	A65	B65	PCIE_RX1-	PCI-E lane 1 receive -
Power Ground	GND	A66	B66	WAKE0#	PCI-express wake up signal
GP Input 2 / SDIO data signal 2	GPI2/SD_DATA2	A67	B67	WAKE1#	General purpose wake up signal
PCI-E lane 0 transmit +	PCIE_TX0+	A68	B68	PCIE_RX0+	PCI-E lane 0 receive +
PCI-E lane 0 transmit -	PCIE_TX0-	A69	B69	PCIE_RX0-	PCI-E lane 0 receive -
Power Ground	GND	A70	B70	GND	Power Ground
LVDS Ch. A Data 0 + / eDP Ch. Data 2+	LVDS_A0+/eDP_TX2+	A71	B71	LVDS_B0+	LVDS Ch. B Data 0 +
LVDS Ch. A Data 0 - / eDP Ch. Data 2-	LVDS_A0-/eDP_TX2-	A72	B72	LVDS_B0-	LVDS Ch. B Data 0 -
LVDS Ch. A Data 1+ / eDP Ch. Data 1+	LVDS_A1+/eDP_TX1+	A73	B73	LVDS_B1+	LVDS Ch. B Data 1 +
LVDS Ch. A Data 1- / eDP Ch. Data 1-	LVDS_A1-/eDP_TX1-	A74	B74	LVDS_B1-	LVDS Ch. B Data 1 -

LVDS Ch. A Data 2+ / eDP Ch. Data 0+	LVDS_A2+/eDP_TX0+	A75	B75	LVDS_B2+	LVDS Ch. B Data 2 +
LVDS Ch. A Data 2- / eDP Ch. Data 0-	LVDS_A2-/eDP_TX0+	A76	B76	LVDS_B2-	LVDS Ch. B Data 2 -
LVDS Panel Power Enable	LVDS_VDD_EN	A77	B77	LVDS_B3+	LVDS Ch. B Data 3 +
LVDS Ch. A Data 3 +	LVDS_A3+	A78	B78	LVDS_B3-	LVDS Ch. B Data 3 -
LVDS Ch. A Data 3 -	LVDS_A3-	A79	B79	LVDS_BKLT_EN	LVDS Panel Backlight ON
Power Ground	GND	A80	B80	GND	Power Ground
LVDS Ch. A Clock + / eDP Ch. Data 3+	LVDS_A_CK+/eDP_TX3+	A81	B81	LVDS_B_CK+	LVDS Ch. B Clock +
LVDS Ch. A Clock - / eDP Ch. Data 3-	LVDS_A_CK-/eDP_TX3-	A82	B82	LVDS_B_CK-	LVDS Ch. B Clock -
LVDS I2C Clock / eDP Ch. Aux +	LVDS_I2C_CK/eDP_AUX+	A83	B83	LVDS_BKLT_CTRL	LVDS Backlight Brightness
LVDS I2C Data / eDP Ch. Aux -	LVDS_I2C_DAT/eDP_AUX-	A84	B84	+5V_A	+5V Standby power line
GP Input 3 / SDIO data signal 3	GPI3/SD_DATA3	A85	B85	+5V_A	+5V Standby power line
Not Connected	RSVD	A86	B86	+5V_A	+5V Standby power line
eDP Hot Plug Detect Signal	eDP_HPD	A87	B87	+5V_A	+5V Standby power line
PCI-E Clock reference +	PCIE_CK_REF+	A88	B88	BIOS_DIS1#	BIOS boot device select 1 signal
PCI-E Clock reference -	PCIE_CK_REF-	A89	B89	VGA_RED	VGA Red for monitor Output
Power Ground	GND	A90	B90	GND	Power Ground
Power supply for Carrier Board SPI Device	SPI_POWER	A91	B91	VGA_GRN	VGA Green for monitor Output
Data in to Module from Carrier SPI Device	SPI_MISO	A92	B92	VGA_BLU	VGA Blu for monitor Output
GP Output 0 / SDIO Clock	GPO0 / SD_CLK	A93	B93	VGA_HSYNC	VGA Horizontal sync output
Clock from Module to Carrier SPI Device	SPI_CLK	A94	B94	VGA_VSYNC	VGA Vertical sync output
Data out from Module to carrier SPI device	SPI_MOSI	A95	B95	VGA_I2C_CK	DDC clock line
TPM Physical Presence pin, Active High Input for optional on-board TPM device	TPM_PP	A96	B96	VGA_I2C_DAT	DDC data line
Type10 signal: Not connected	Type10#	A97	B97	SPI_CS#	SPI Chip Select signal
Module's serial port 0 TX	SER0_TX	A98	B98	RSVD	Not Connected
Module's serial port 0 RX	SER0_RX	A99	B99	RSVD	Not Connected
Power Ground	GND	A100	B100	GND	Power Ground
Module's serial port 1 TX	SER1_TX	A101	B101	FAN_PWMOUT	FAN Speed control
Module's serial port 1 RX	SER1_RX	A102	B102	FAN_TACHIN	FAN tachometer input
LID button input	LID#	A103	B103	SLEEP#	Sleep Button Input
+12V switched power supply	+12V_S	A104	B104	+12V_S	+12V switched power supply

+12V switched power supply	+12V_S	A105	B105	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	A106	B106	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	A107	B107	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	A108	B108	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	A109	B109	+12V_S	+12V switched power supply
Power Ground	GND	A110	B110	GND	Power Ground

COM Express™ Connector CN3 - Rows C & D

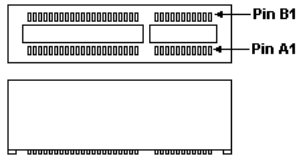
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
Power Ground	GND	C1	D1	GND	Power Ground
Power Ground	GND	C2	D2	GND	Power Ground
SuperSpeed USB receive pair 0-	USB_SSRX0-	C3	D3	USB_SSTX0-	SuperSpeed USB transmit pair 0-
SuperSpeed USB receive pair 0+	USB_SSRX0+	C4	D4	USB_SSTX0+	SuperSpeed USB transmit pair 0+
Power ground	GND	C5	D5	GND	Power ground
SuperSpeed USB receive pair 1-	USB_SSRX1-	C6	D6	USB_SSTX1-	SuperSpeed USB transmit pair 1-
SuperSpeed USB receive pair 1+	USB_SSRX1+	C7	D7	USB_SSTX1+	SuperSpeed USB transmit pair 1+
Power ground	GND	C8	D8	GND	Power ground
SuperSpeed USB receive pair 2-	USB_SSRX2-	C9	D9	USB_SSTX2-	SuperSpeed USB transmit pair 2-
SuperSpeed USB receive pair 2+	USB_SSRX2+	C10	D10	USB_SSTX2+	SuperSpeed USB transmit pair 2+
Power Ground	GND	C11	D11	GND	Power Ground
SuperSpeed USB receive pair 3-	USB_SSRX3-	C12	D12	USB_SSTX3-	SuperSpeed USB transmit pair 3-
SuperSpeed USB receive pair 3+	USB_SSRX3+	C13	D13	USB_SSTX3+	SuperSpeed USB transmit pair 3+
Power Ground	GND	C14	D14	GND	Power Ground
Not Connected	N.C.	C15	D15	DDI1_CTRLCLK_AUX+	DP1 Aux+ or TMDS1 I2C_CLK
Not Connected	N.C.	C16	D16	DDI1_CTRLDATA_AUX-	DP1 Aux- or TMDS1 I2C_DAT
Reserved Purpose Signal	RSVD#C17	C17	D17	RSVD#D17	Reserved Purpose Signal
Reserved Purpose Signal	RSVD#C18	C18	D18	RSVD#D18	Reserved Purpose Signal
PCI Express Receive Pair 6+	PCIE_RX6+	C19	D19	PCIE_TX6+	PCI Express Transmit Pair 6+
PCI Express Receive Pair 6-	PCIE_RX6-	C20	D20	PCIE_TX6-	PCI Express Transmit Pair 6-
Power Ground	GND	C21	D21	GND	Power Ground
PCI Express Receive Pair 7+	PCIE_RX7+	C22	D22	PCIE_TX7+	PCI Express Transmit Pair 7+

PCI Express Receive Pair 7-	PCIE_RX7-	C23	D23	PCIE_TX7-	PCI Express Transmit Pair 7-
Digital Display Interface 1 Hot-Plug Detect	DDI1_HPD	C24	D24	RSVD#D24	Reserved Purpose Signal
Not Connected	N.C.	C25	D25	RSVD#D25	Reserved Purpose Signal
Not Connected	N.C.	C26	D26	DDI1_PAIR0+	Digital Display interface 1 pair 0+
Reserved Purpose Signal	RSVD#C27	C27	D27	DDI1_PAIR0-	Digital Display interface 1 pair 0-
Reserved Purpose Signal	RSVD#C28	C28	D28	RSVD#D28	Reserved Purpose Signal
Not Connected	N.C.	C29	D29	DDI1_PAIR1+	Digital Display interface 1 pair 1+
Not Connected	N.C.	C30	D30	DDI1_PAIR1-	Digital Display interface 1 pair 1-
Power Ground	GND	C31	D31	GND	Power Ground
DP2 Aux+ or TMDS2 I2C_CLK	DDI2_CTRLCLK_AUX+	C32	D32	DDI1_PAIR2+	Digital Display interface 1 pair 2+
DP2 Aux- or TMDS2 I2C_DAT	DDI2_CTRLDATA_AUX-	C33	D33	DDI1_PAIR2-	Digital Display interface 1 pair 2-
DP2 or TMDS2 selector	DDI2_DDC_AUX_SEL	C34	D34	DDI1_DDC_AUX_SEL	DP1 or TMDS1 selector
Reserved Purpose Signal	RSVD#C35	C35	D35	RSVD#D35	Reserved Purpose Signal
DP3 Aux+ or TMDS3 I2C_CLK	DDI3_CTRLCLK_AUX+	C36	D36	DDI1_PAIR3+	Digital Display interface 1 pair 3+
DP3 Aux- or TMDS3 I2C_DAT	DDI3_CTRLDATA_AUX-	C37	D37	DDI1_PAIR3-	Digital Display interface 1 pair 3-
DP3 or TMDS3 selector	DDI3_DDC_AUX_SEL	C38	D38	RSVD#D38	Reserved Purpose Signal
Digital Display interface 3 pair 0+	DDI3_PAIR0+	C39	D39	DDI2_PAIR0+	Digital Display interface 2 pair 0+
Digital Display interface 3 pair 0-	DDI3_PAIR0-	C40	D40	DDI2_PAIR0-	Digital Display interface 2 pair 0-
Power Ground	GND	C41	D41	GND	Power Ground
Digital Display interface 3 pair 1+	DDI3_PAIR1+	C42	D42	DDI2_PAIR1+	Digital Display interface 2 pair 1+
Digital Display interface 3 pair 1-	DDI3_PAIR1-	C43	D43	DDI2_PAIR1-	Digital Display interface 2 pair 1-
Digital Display Interface 3Hot-Plug Detect	DDI3_HPD	C44	D44	DDI2_HPD	Digital Display Interface 2 Hot-Plug Detect
Reserved Purpose Signal	RSVD#C45	C45	D45	RSVD#D45	Reserved Purpose Signal
Digital Display interface 3 pair 2+	DDI3_PAIR2+	C46	D46	DDI2_PAIR2+	Digital Display interface 2 pair 2+
Digital Display interface 3 pair 2-	DDI3_PAIR2-	C47	D47	DDI2_PAIR2-	Digital Display interface 2 pair 2-
Reserved Purpose Signal	RSVD#C48	C48	D48	RSVD#D48	Reserved Purpose Signal
Digital Display interface 3 pair 3+	DDI3_PAIR3+	C49	D49	DDI2_PAIR3+	Digital Display interface 2 pair 3+
Digital Display interface 3 pair 3-	DDI3_PAIR3-	C50	D50	DDI2_PAIR3-	Digital Display interface 2 pair 3-
Power Ground	GND	C51	D51	GND	Power Ground
PCIe Graphics receive pair 0+	PEG_RX0+	C52	D52	PEG_TX0+	PCIe Graphics transmit pair 0+

PCIe Graphics receive pair 0-	PEG_RX0-	C53	D53	PEG_TX0-	PCIe Graphics transmit pair 0-
Type0 signal: Not Connected	TYPE0#	C54	D54	N.C.	Not Connected
PCIe Graphics receive pair 1+	PEG_RX1+	C55	D55	PEG_TX1+	PCIe Graphics transmit pair 1+
PCIe Graphics receive pair 1-	PEG_RX1-	C56	D56	PEG_TX1-	PCIe Graphics transmit pair 1-
Type1 signal: Not Connected	TYPE1#	C57	D57	TYPE2#	Type2 signal: +5V_A
PCIe Graphics receive pair 2+	PEG_RX2+	C58	D58	PEG_TX2+	PCIe Graphics transmit pair 2+
PCIe Graphics receive pair 2-	PEG_RX2-	C59	D59	PEG_TX2-	PCIe Graphics transmit pair 2-
Power Ground	GND	C60	D60	GND	Power Ground
PCIe Graphics receive pair 3+	PEG_RX3+	C61	D61	PEG_TX3+	PCIe Graphics transmit pair 3+
PCIe Graphics receive pair 3-	PEG_RX3-	C62	D62	PEG_TX3-	PCIe Graphics transmit pair 3-
Reserved Purpose Signal	RSVD#C63	C63	D63	RSVD#D63	Reserved Purpose Signal
Reserved Purpose Signal	RSVD#C64	C64	D64	RSVD#D64	Reserved Purpose Signal
PCIe Graphics receive pair 4+	PEG_RX4+	C65	D65	PEG_TX4+	PCIe Graphics transmit pair 4+
PCIe Graphics receive pair 4-	PEG_RX4-	C66	D66	PEG_TX4-	PCIe Graphics transmit pair 4-
Not Connected	RSVD#C67	C67	D67	GND	Power Ground
PCIe Graphics receive pair 5+	PEG_RX5+	C68	D68	PEG_TX5+	PCIe Graphics transmit pair 5+
PCIe Graphics receive pair 5-	PEG_RX5-	C69	D69	PEG_TX5-	PCIe Graphics transmit pair 5-
Power Ground	GND	C70	D70	GND	Power Ground
PCIe Graphics receive pair 6+	PEG_RX6+	C71	D71	PEG_TX6+	PCIe Graphics transmit pair 6+
PCIe Graphics receive pair 6-	PEG_RX6-	C72	D72	PEG_TX6-	PCIe Graphics transmit pair 6-
Power Ground	GND	C73	D73	GND	Power Ground
PCIe Graphics receive pair 7+	PEG_RX7+	C74	D74	PEG_TX7+	PCIe Graphics transmit pair 7+
PCIe Graphics receive pair 7-	PEG_RX7-	C75	D75	PEG_TX7-	PCIe Graphics transmit pair 7-
Power Ground	GND	C76	D76	GND	Power Ground
Reserved Purpose Signal	RSVD#C77	C77	D77	RSVD#D77	Not Connected
PCIe Graphics receive pair 8+	PEG_RX8+	C78	D78	PEG_TX8+	PCIe Graphics transmit pair 8+
PCIe Graphics receive pair 8-	PEG_RX8-	C79	D79	PEG_TX8-	PCIe Graphics transmit pair 8-
Power Ground	GND	C80	D80	GND	Power Ground
PCIe Graphics receive pair 9+	PEG_RX9+	C81	D81	PEG_TX9+	PCIe Graphics transmit pair 9+
PCIe Graphics receive pair 9-	PEG_RX9-	C82	D82	PEG_TX9-	PCIe Graphics transmit pair 9-

Not Connected	RSVD#C83	C83	D83	RSVD#D83	Not Connected
Power Ground	GND	C84	D84	GND	Power Ground
PCIe Graphics receive pair 10+	PEG_RX10+	C85	D85	PEG_TX10+	PCIe Graphics transmit pair 10+
PCIe Graphics receive pair 10-	PEG_RX10-	C86	D86	PEG_TX10-	PCIe Graphics transmit pair 10-
Power Ground	GND	C87	D87	GND	Power Ground
PCIe Graphics receive pair 11+	PEG_RX11+	C88	D88	PEG_TX11+	PCIe Graphics transmit pair 11+
PCIe Graphics receive pair 11-	PEG_RX11-	C89	D89	PEG_TX11-	PCIe Graphics transmit pair 11-
Power Ground	GND	C90	D90	GND	Power Ground
PCIe Graphics receive pair 12+	PEG_RX12+	C91	D91	PEG_TX12+	PCIe Graphics transmit pair 12+
PCIe Graphics receive pair 12-	PEG_RX12-	C92	D92	PEG_TX12-	PCIe Graphics transmit pair 12-
Power Ground	GND	C93	D93	GND	Power Ground
PCIe Graphics receive pair 13+	PEG_RX13+	C94	D94	PEG_TX13+	PCIe Graphics transmit pair 13+
PCIe Graphics receive pair 13-	PEG_RX13-	C95	D95	PEG_TX13-	PCIe Graphics transmit pair 13-
Power Ground	GND	C96	D96	GND	Power Ground
Not Connected	RSVD#C97	C97	D97	RSVD#D97	Not Connected
PCIe Graphics receive pair 14+	PEG_RX14+	C98	D98	PEG_TX14+	PCIe Graphics transmit pair 14+
PCIe Graphics receive pair 14-	PEG_RX14-	C99	D99	PEG_TX14-	PCIe Graphics transmit pair 14-
Power Ground	GND	C100	D100	GND	Power Ground
PCIe Graphics receive pair 15+	PEG_RX15+	C101	D101	PEG_TX15+	PCIe Graphics transmit pair 15+
PCIe Graphics receive pair 15-	PEG_RX15-	C102	D102	PEG_TX15-	PCIe Graphics transmit pair 15-
Power Ground	GND	C103	D103	GND	Power Ground
+12V switched power supply	+12V_S	C104	D104	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	C105	D105	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	C106	D106	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	C107	D107	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	C108	D108	+12V_S	+12V switched power supply
+12V switched power supply	+12V_S	C109	D109	+12V_S	+12V switched power supply
Power Ground	GND	C110	D110	GND	Power Ground

3.3.2 PCI-e x4 Slots



CCOMe-C96 board offer a possibility of expansion through two standard PCI-e x4 card edge connectors, type WINWIN p/n WPES-064AN41B22UWC or equivalent, with the pinout shown in the following table.

On first slot CN12, are carried out PCI-e lanes #0..#3 coming from COM Express™ connector (rows A-B).

On second slot CN14, are carried out PCI-e lanes #4..#7 coming from COM Express™ connector (rows A-B-C-D).

Please be aware that availability of all eight PCI express lanes depends on the COM Express™ module used.

Please check the User Manual of the COM Express™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

On CCOMe-C96 carrier board, the PCI-express compatibility is ensured with devices up to Gen3.

PCI-e x 4 Slot CN12					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_1_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground

Power Ground	GND	B13	A13	PCIEx4_1_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 0+	PCIE_TX0+	B14	A14	PCIEx4_1_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 0-	PCIE_TX0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX0+	PCI-e Receiver lane 0+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX0-	PCI-e Receiver lane 0-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 1+	PCIE_TX1+	B19	A19	RSVD	Not Connected
PCI-e Transmitter lane 1-	PCIE_TX1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX1+	PCI-e Receiver lane 1+
Power Ground	GND	B22	A22	PCIE_RX1-	PCI-e Receiver lane 1-
PCI-e Transmitter lane 2+	PCIE_TX2+	B23	A23	GND	Power Ground
PCI-e Transmitter lane 2-	PCIE_TX2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX2+	PCI-e Receiver lane 2+
Power Ground	GND	B26	A26	PCIE_RX2-	PCI-e Receiver lane 2-
PCI-e Transmitter lane 3+	PCIE_TX3+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 3-	PCIE_TX3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX3+	PCI-e Receiver lane 3+
Not Connected	RSVD	B30	A30	PCIE_RX3-	PCI-e Receiver lane 3-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

PCI-e x 4 Slot CN14

Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	PRSNT1#	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail

+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	Not connected
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	Not connected
Power Ground	GND	B7	A7	JTAG4	Not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	Not connected
Not Connected	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PCIEx4_2_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PCIEx4_2_CLK_P	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer
PCI-e Transmitter lane 4+	PCIE_TX4+	B14	A14	PCIEx4_2_CLK_N	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Transmitter lane 4-	PCIE_TX4-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PCIE_RX4+	PCI-e Receiver lane 4+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B17	A17	PCIE_RX4-	PCI-e Receiver lane 4-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Transmitter lane 5+	PCIE_TX5+	B19	A19	RSVD	Not Connected
PCI-e Transmitter lane 5-	PCIE_TX5-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PCIE_RX5+	PCI-e Receiver lane 5+
Power Ground	GND	B22	A22	PCIE_RX5-	PCI-e Receiver lane 5-
PCI-e Transmitter lane 6+	PCIE_TX6+	B23	A23	GND	Power Ground

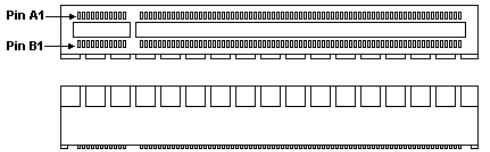
PCI-e Transmitter lane 6-	PCIE_TX6-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PCIE_RX6+	PCI-e Receiver lane 6+
Power Ground	GND	B26	A26	PCIE_RX6-	PCI-e Receiver lane 6-
PCI-e Transmitter lane 7+	PCIE_TX7+	B27	A27	GND	Power Ground
PCI-e Transmitter lane 7-	PCIE_TX7-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PCIE_RX7+	PCI-e Receiver lane 7+
Not Connected	RSVD	B30	A30	PCIE_RX7-	PCI-e Receiver lane 7-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT2#	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not Connected

!

Please be aware that PCI-e management on CCOMe-C96 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.3 PEG (PCI Express Graphics x16) Connector



According to COM Express™ specifications, it is possible to expand the graphical capabilities of the board by using the dedicated PCI Express Graphics x16 bus (PEG) interface, which can be accessed through a card edge connector type LOTES p/n APCI0470-P002C or equivalent, with the pinout shown in the following table.

Please check the User Manual of the COM Express™ module used for details about the availability of these lanes.

Please be aware that availability of these PCI express lanes depends on the COM Express™ module used.

Please check the User Manual of the COM Express™ module used for details about the availability of these lanes and all possible groupings that can be applied to these lanes.

PCI Express Graphics x16 Slot- CN13					
Description	Pin name	Pin nr.	Pin nr.	Pin name	Description
+12V Power Rail	+12V_RUN	B1	A1	GND	Hot Plug presence detect (tied to GND)
+12V Power Rail	+12V_RUN	B2	A2	+12V_RUN	+12V Power Rail
+12V Power Rail	+12V_RUN	B3	A3	+12V_RUN	+12V Power Rail
Power Ground	GND	B4	A4	GND	Power Ground
SM Bus Clock line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_CK with mosfet voltage level converter	PCIE_ SMB_CLK	B5	A5	JTAG2	TCK, tied to GND with 4K7Ω resistor
SM Bus Data line. +3.3V_RUN electrical level with 10kΩ pull up resistor, derived by SMB_DAT with mosfet voltage level converter	PCIE_ SMB_DAT	B6	A6	JTAG3	TDI, tied to +3.3V_RUN with 4K7Ω resistor
Power Ground	GND	B7	A7	JTAG4	Test Data Out, not connected
+3.3V Power Rail	+3.3V_RUN	B8	A8	JTAG5	TMS, tied to +3.3V_RUN with 4K7Ω resistor
TRST#, tied to GND with 4K7Ω resistor	JTAG1	B9	A9	+3.3V_RUN	+3.3V Power Rail
+3.3V Auxiliary Power Rail	+3.3V_ALW	B10	A10	+3.3V_RUN	+3.3V Power Rail
Wake signal for link reactivation	WAKE0#	B11	A11	PEG_RST#	Reset signal to the add-in card, derived by CB_RESET# using a Ultra High Speed CMOS buffer. Active low signal, +3.3V_ALW electrical level with a 100kΩ pull down resistor.
Not Connected	RSVD	B12	A12	GND	Power Ground
Power Ground	GND	B13	A13	PEG_CLK+	PCI-e reference clock lane +, derived by PCIE_CK_REF+ using a Clock Buffer

PCI-e Graphics Transmitter lane 0+	PEG_TX0+	B14	A14	PEG_CLK-	PCI-e reference clock lane +, derived by PCIE_CK_REF- using a Clock Buffer
PCI-e Graphics Transmitter lane 0-	PEG_TX0-	B15	A15	GND	Power Ground
Power Ground	GND	B16	A16	PEG_RX0+	PCI-e Graphics Receiver lane 0+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT#2	B17	A17	PEG_RX0-	PCI-e Graphics Receiver lane 0-
Power Ground	GND	B18	A18	GND	Power Ground
PCI-e Graphics Transmitter lane 1+	PEG_TX1+	B19	A19	RSVD	Not connected
PCI-e Graphics Transmitter lane 1-	PEG_TX1-	B20	A20	GND	Power Ground
Power Ground	GND	B21	A21	PEG_RX1+	PCI-e Graphics Receiver lane 1+
Power Ground	GND	B22	A22	PEG_RX1-	PCI-e Graphics Receiver lane 1-
PCI-e Graphics Transmitter lane 2+	PEG_TX2+	B23	A23	GND	Power Ground
PCI-e Graphics Transmitter lane 2-	PEG_TX2-	B24	A24	GND	Power Ground
Power Ground	GND	B25	A25	PEG_RX2+	PCI-e Graphics Receiver lane 2+
Power Ground	GND	B26	A26	PEG_RX2-	PCI-e Graphics Receiver lane 2-
PCI-e Graphics Transmitter lane 3+	PEG_TX3+	B27	A27	GND	Power Ground
PCI-e Graphics Transmitter lane 3-	PEG_TX3-	B28	A28	GND	Power Ground
Power Ground	GND	B29	A29	PEG_RX3+	PCI-e Graphics Receiver lane 3+
Not Connected	RSVD	B30	A30	PEG_RX3-	PCI-e Graphics Receiver lane 3-
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT#2	B31	A31	GND	Power Ground
Power Ground	GND	B32	A32	RSVD	Not connected
PCI-e Graphics Transmitter lane 4+	PEG_TX4+	B33	A33	RSVD	Not connected
PCI-e Graphics Transmitter lane 4-	PEG_TX4-	B34	A34	GND	Power Ground
Power Ground	GND	B35	A35	PEG_RX4+	PCI-e Graphics Receiver lane 4+
Power Ground	GND	B36	A36	PEG_RX4-	PCI-e Graphics Receiver lane 4-
PCI-e Graphics Transmitter lane 5+	PEG_TX5+	B37	A37	GND	Power Ground
PCI-e Graphics Transmitter lane 5-	PEG_TX5-	B38	A38	GND	Power Ground

Power Ground	GND	B39	A39	PEG_RX5+	PCI-e Graphics Receiver lane 5+
Power Ground	GND	B40	A40	PEG_RX5-	PCI-e Graphics Receiver lane 5-
PCI-e Graphics Transmitter lane 6+	PEG_TX6+	B41	A41	GND	Power Ground
PCI-e Graphics Transmitter lane 6-	PEG_TX6-	B42	A42	GND	Power Ground
Power Ground	GND	B43	A43	PEG_RX6+	PCI-e Graphics Receiver lane 6+
Power Ground	GND	B44	A44	PEG_RX6-	PCI-e Graphics Receiver lane 6-
PCI-e Graphics Transmitter lane 7+	PEG_TX7+	B45	A45	GND	Power Ground
PCI-e Graphics Transmitter lane 7-	PEG_TX7-	B46	A46	GND	Power Ground
Power Ground	GND	B47	A47	PEG_RX7+	PCI-e Graphics Receiver lane 7+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT#2	B48	A48	PEG_RX7-	PCI-e Graphics Receiver lane 7-
Power Ground	GND	B49	A49	GND	Power Ground
PCI-e Graphics Transmitter lane 8+	PEG_TX8+	B50	A50	RSVD	Not connected
PCI-e Graphics Transmitter lane 8-	PEG_TX8-	B51	A51	GND	Power Ground
Power Ground	GND	B52	A52	PEG_RX8+	PCI-e Graphics Receiver lane 8+
Power Ground	GND	B53	A53	PEG_RX8-	PCI-e Graphics Receiver lane 8-
PCI-e Graphics Transmitter lane 9+	PEG_TX9+	B54	A54	GND	Power Ground
PCI-e Graphics Transmitter lane 9-	PEG_TX9-	B55	A55	GND	Power Ground
Power Ground	GND	B56	A56	PEG_RX9+	PCI-e Graphics Receiver lane 9+
Power Ground	GND	B57	A57	PEG_RX9-	PCI-e Graphics Receiver lane 9-
PCI-e Graphics Transmitter lane 10+	PEG_TX10+	B58	A58	GND	Power Ground
PCI-e Graphics Transmitter lane 10-	PEG_TX10-	B59	A59	GND	Power Ground
Power Ground	GND	B60	A60	PEG_RX10+	PCI-e Graphics Receiver lane 10+
Power Ground	GND	B61	A61	PEG_RX10-	PCI-e Graphics Receiver lane 10-
PCI-e Graphics Transmitter lane 11+	PEG_TX11+	B62	A62	GND	Power Ground
PCI-e Graphics Transmitter lane 11-	PEG_TX11-	B63	A63	GND	Power Ground
Power Ground	GND	B64	A64	PEG_RX11+	PCI-e Graphics Receiver lane 11+
Power Ground	GND	B65	A65	PEG_RX11-	PCI-e Graphics Receiver lane 11-
PCI-e Graphics Transmitter lane 12+	PEG_TX12+	B66	A66	GND	Power Ground

PCI-e Graphics Transmitter lane 12-	PEG_TX12-	B67	A67	GND	Power Ground
Power Ground	GND	B68	A68	PEG_RX12+	PCI-e Graphics Receiver lane 12+
Power Ground	GND	B69	A69	PEG_RX12-	PCI-e Graphics Receiver lane 12-
PCI-e Graphics Transmitter lane 13+	PEG_TX13+	B70	A70	GND	Power Ground
PCI-e Graphics Transmitter lane 13-	PEG_TX13-	B71	A71	GND	Power Ground
Power Ground	GND	B72	A72	PEG_RX13+	PCI-e Graphics Receiver lane 13+
Power Ground	GND	B73	A73	PEG_RX13-	PCI-e Graphics Receiver lane 13-
PCI-e Graphics Transmitter lane 14+	PEG_TX14+	B74	A74	GND	Power Ground
PCI-e Graphics Transmitter lane 14-	PEG_TX14-	B75	A75	GND	Power Ground
Power Ground	GND	B76	A76	PEG_RX14+	PCI-e Graphics Receiver lane 14+
Power Ground	GND	B77	A77	PEG_RX14-	PCI-e Graphics Receiver lane 14-
PCI-e Graphics Transmitter lane 15+	PEG_TX15+	B78	A78	GND	Power Ground
PCI-e Graphics Transmitter lane 15-	PEG_TX15-	B79	A79	GND	Power Ground
Power Ground	GND	B80	A80	PEG_RX15+	PCI-e Graphics Receiver lane 15+
Hot Plug presence detect. Input Signal from add in card used to enable the reference clock of this slot. Active low signal, +3.3V_RUN electrical level with a 10kΩ pull down resistor.	PRSNT#2	B81	A81	PEG_RX15-	PCI-e Graphics Receiver lane 15-
Not Connected	RSVD	B82	A82	GND	Power Ground

Please be aware that PCI-e management on CCOMe-C96 carrier board requires that the add-in card placed on this slot manages the Presence Detect pins (B81/B48/B31/B17 and A1). More exactly, according to the PCI Express™ Card Electromechanical Specification v3.0, it is required that these pins are tied together on the ADD-in Card (at least, it is needed that pin A1 is connected with pin B81 or B48 or B17 or pin B31).

In case that these pins are not tied together on the add-in card, then the carrier board will not acknowledge the presence of the card in the slot, and will not enable the reference clock (and the add-in card will not work).

3.3.4 eSPI/LPC Debug Connector

eSPI/LPC Debug Connector – CN15			
Pin	**Signal**	**Pin**	**Signal**
1	LPC_CLK/ESPI_CK	2	SUS_STAT#/ESPI_RESET#
3	LPC_RST#	4	+3.3V_RUN
5	LPC_AD0/ESPI_IO_0	6	LPC_DRQ0#/ESPI_ALERT0#
7	LPC_AD1/ESPI_IO_1	8	LPC_SERIRQ#/ESPI_CS1#
9	LPC_AD2/ESPI_IO_2		
11	LPC_AD3/ESPI_IO_3	12	GND
13	LPC_FRAME#/ESPI_CS0#	14	GND

The COM Express™ card edge connector shares on the same pins both the LPC and the eSPI interface. Please check the COM Express™ module to see whether LPC or eSPI interface is made available.

The signals of these pins are first of all carried directly to an internal dual row 6+7 pin header CN15, type NELTRON p/n 2208SM-14G-E10-CR or equivalent, with the pinout shown in the table on the left.

If LPC bus is available from selected COM Express™ module, then following signals will be present:

LPC_CLK: LPC Clock Output 33MHz

LPC_RST#: when jumper JP3 is inserted, this signal is derived by CB_RESET# signal or simply by biasing it using a Ultra High Speed CMOS buffer. When jumper JP3 is not inserted, this signal is derived by an eSPI to LPC bridge placed on carrier board

LPC_AD[0:3]: LPC address, command and data bus, bidirectional signal

LPC_FRAME#: LPC Frame indicator, active low output signal. This signal is used to signal the start of a new cycle of transmission, or the termination of existing cycles due to abort or time-out condition.

SUS_STAT#: Signal indicating suspend status output, active low signal. It is used to notify LPC devices that the module is going to enter in one of possible ACPI low-power states

LPC_DRQ0#: LPC serial DMA request input signal

LPC_SERIRQ#: LPC Serialised IRQ request, bidirectional signal

Otherwise, if eSPI interface is available from selected COM Express™ module, then following signals will be present:

ESPI_CK: eSPI Master Clock Output

ESPI_IO_[0:3]: eSPI Master Data Input / Outputs. These are bi-directional input/output signals used to transfer data between master and slaves.

ESPI_CS0#: eSPI Master Chip Select #0. Active low output signal.

ESPI_CS1#: eSPI Master Chip Select #1. Active low output signal.

ESPI_RESET#: eSPI Reset Signal for both master and slaves devices

ESPI_ALERT0#: eSPI signal used by eSPI slave to request service from the eSPI master

JP4 position	JP3 position	eSPI/LPC interface
Not inserted	Not Care	eSPI/LPC interface disabled
Inserted	Not inserted	eSPI interface from COM Express™ module
Inserted	Inserted	LPC interface from COM Express™ module

LPC /eSPI interface, in addition to eSPI/LPC Debug Connector CN15, is carried to the rest of the carrier board and its routing is managed by JP3 and JP4 selection 2-way jumpers.

JP4 selection jumper is used to enable / disable the eSPI/LPC interface for the rest of the carrier board, meaning that when not inserted this interface is made available only at CN15 debug connector.

If the eSPI/LPC interface is enabled with JP4 inserted, JP3 is the selector for the type of interface coming from COM Express™ module. When not inserted, meaning that eSPI interface is available from COM Express™ module, LPC bus is implemented by using an eSPI-to-LPC bridge. Otherwise, when inserted, meaning that LPC bus is directly available, without the need of the bridge. For both cases, on this LPC bus are then available a Dual LPC UART bridge, which allows the implementation of two legacy COM Ports, and a CPLD, which manages four seven-segment LCD display, used to show the POST codes transmitted on ports 80h and 84h.

3.3.5 COM ports and RS232 ports Internal pin Headers

COM ports Internal pin Header - CN17			
Pin	**Signal RS-232 mode**	**Signal RS-422 mode**	**Signal RS-485 mode**
1	COM1_RxD	COM1_Rx+	
2	COM2_RxD	COM2_Rx+	
3	COM1_TxD	COM1_Tx-	COM1_Rx-/COM1_Tx-
4	COM2_TxD	COM2_Tx-	COM2_Rx-/COM2_Tx-
5		GND	
7	COM1_RTS#	COM1_Tx+	COM1_Rx+/COM1_Tx+
8	COM2_RTS#	COM2_Tx+	COM2_Rx+/COM2_Tx+
9	COM1_CTS#	COM1_Rx-	
10	COM2_CTS#	COM2_Rx-	

Interfaced to the LPC Bus coming from the COM Express™ module, on CCOMe-C96 Carrier board there is a Dual LPC UART bridge, which allows the implementation of two legacy COM Ports.

These two COM ports are made externally accessible through two multistandard transceivers, which allow using them in RS-232, RS-422 or RS-485 mode.

These ports are available on dedicated connector CN17, which is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

Selection of working mode is made using jumpers JP5 and JP6, which are standard pin headers, P2.54mm, 1x3 pin.

According to the working mode selected via jumpers JP5 and JP6, the pinout of the connector (a dual row p.254mm 9-pin header) is as described in the left table.

JP5 position	COM #1 Working Mode
1-2	RS-422
2-3	RS-232
Not Inserted	RS-485

JP6 position	COM #2 Working Mode
1-2	RS-422
2-3	RS-232
Not Inserted	RS-485

Please be aware that for proper RS-485 working, the RTS# signals must be used as a handshaking signal, i.e. it is used to control the data flow direction. When RTS# signal is driven low, then the RS-485 port is in receiving mode, when RTS# signal is driven high then the RS-485 port is in transmitting mode.

Signals Description

COM1_RxD/COM2_RxD: COM port #1 / #2 RS-232 Receive data

COM1_TxD/COM2_TxD: COM port #1 / #2 RS-232 Transmit data

COM1_RTS#/COM2_RTS#: COM port #1 / #2 RS-232 Request to Send handshaking signal.

COM1_CTS#/COM2_CTS#: COM port #1 / #2 RS-232 Clear To Send handshaking signal

COM1_RX+/COM1_RX-: COM port #1 RS-422 Receive differential pair

COM1_TX+/COM1_TX-: COM port #1 RS-422 Transmit differential pair

COM2_RX+/COM2_RX-: COM port #2 Full Duplex RS-485 (RS-422) Receive differential pair

COM2_TX+/COM2_TX-: COM port #2 Full Duplex RS-485 (RS-422) Transmit differential pair

COM1_Data+/COM1_Data-: COM Port #1 Half Duplex RS-485 Differential Pair

COM2_Data+/COM2_Data-: COM Port #2 Half Duplex RS-485 Differential Pair

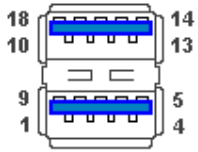
RS232 Internal pin Header- CN26			
Pin	Signal	Pin	Signal
1	UART0_232_RX	2	UART1_232_RX
3	UART0_232_TX	4	UART1_232_TX
5	GND		
7	N.C.	8	N.C.
9	N.C.	10	N.C.

In addition, COM Express™ modules foresee a maximum of 2 Serial Ports with only Tx and Rx signals (SER #0 and SER #1).

These two ports are managed though a single RS-232 transceiver, and the output is available on an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E06 or equivalent.

3.3.6 USB and Gigabit Ethernet ports

USB 3.1 ports #0 / #1- CN18			
Pin	**Signal**	**Pin**	**Signal**
1	$+5V_{USB0}$	10	$+5V_{USB1}$
2	USB_0-	11	USB_1-
3	USB_0+	12	USB_1+
4	GND	13	GND
5	USB_SSRX0-	14	USB_SSRX1-
6	USB_SSRX0+	15	USB_SSRX1+
7	GND	16	GND
8	USB_SSTX0-	17	USB_SSTX1-
9	USB_SSTX0+	18	USB_SSTX1+



The CCOMe-C96 Carrier board offers the possibility of using all the possible USB ports that are foreseen for COM Express™ Type 6 modules.

The signals of USB 3.0 ports #0 ÷ #1 are carried to a double type-A USB 3.1 stacked receptacle, type Winning p/n WDU3R-18F1B4PBUW3 or equivalent.

More specifically, USB 3.1 port #0 is carried to the lower USB receptacle of CN18, while USB 3.1 port #1 is carried to the upper USB receptacle of CN18.

Since this connector is a standard type receptacle, it can be connected to all types of USB 1.1 / USB 2.0 / USB 3.0 devices using Standard-A USB 3.0 or USB 2.0 plugs.

For USB 3.0 connections it is mandatory the use of SuperSpeed certified cables, whose SuperSpeed differential pairs are individually shielded inside the global cable's external shielding.

Signal description:

USB_0+/USB_0-: USB 2.0 Port #0 differential pair

USB_SSRX0+/USB_SSRX0-: USB Super Speed Port #0 receive differential pair

USB_SSTX0+/USB_SSTX0-: USB Super Speed Port #0 transmit differential pair

USB_1+/USB_1-: USB 2.0 Port #1 differential pair

USB_SSRX1+/USB_SSRX1-: USB Super Speed Port #1 receive differential pair

USB_SSTX1+/USB_SSTX1-: USB Super Speed Port #1 transmit differential pair

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

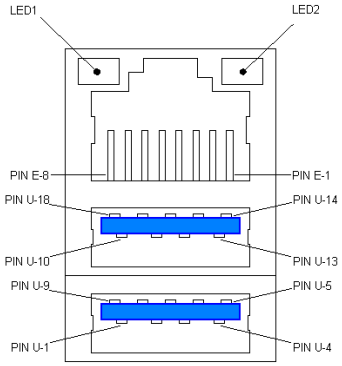
$+5V_{USB0}$ and $+5V_{USB1}$ are derived from +5V_ALW through a 1A current limited power switch.

Combo USB 3.1 ports #2 #3 Dual Type-A socket + RJ45 - CN19			
Pin	**Signal**	**Pin**	**Signal**
U1	$+5V_{USB2}$	U10	$+5V_{USB3}$
U2	USB_2-	U11	USB_3-
U3	USB_2+	U12	USB_3+
U4	GND	U13	GND
U5	USB_SSRX2-	U14	USB_SSRX3-
U6	USB_SSRX2+	U15	USB_SSRX3+
U7	GND	U16	GND
U8	USB_SSTX2-	U17	USB_SSTX3-
U9	USB_SSTX2+	U18	USB_SSTX3+
E1	GBE0_MDI0+	E5	GBE0_MDI2-
E2	GBE0_MDI0-	E6	GBE0_MDI1-
E3	GBE0_MDI1+	E7	GBE0_MDI3+
E4	GBE0_MDI2+	E8	GBE0_MDI3-

The signals of USB 3.0 ports #2 ÷ #3 ports are carried to a Combo Connector CN19, type LOTES p/n AJKM0030 or equivalent, composed by a double type A USB 3.1 receptacle socket and one Gigabit Ethernet RJ-45 connector, directly managed by the COM Express™ module.

On this connector there are also two bicolour Green/Yellow LEDs: LED1 (Left LED) shows 10/100 or 1000 connection: green means 100Mbps connection, yellow means 1000Mpbs connection, when the LED is Off then 10Mpbs or no connection is available. LED2 (Right LED) shows ACTIVITY presence.

This interface is compatible both with Gigabit Ethernet (1000Mbps) and with Fast Ethernet (10/100Mbps) Networks. It will configure automatically to work with the existing network.



Please be aware that it will work in Gigabit mode only in case that it is connected to Gigabit Ethernet switches/hubs/routers. For the connection, cables category Cat5e or better are required. Cables category Cat6 are recommended for noise reduction and EMC compatibility issues, especially when the length of the cable is significant.

Signal description:

USB_2+/USB_2-: USB 2.0 Port #2 differential pair

USB_SSRX2+/USB_SSRX2-: USB Super Speed Port #2 receive differential pair

USB_SSTX2+/USB_SSTX2-: USB Super Speed Port #2 transmit differential pair

USB_3+/USB_3-: USB 2.0 Port #3 differential pair

USB_SSRX3+/USB_SSRX3-: USB Super Speed Port #3 receive differential pair

USB_SSTX3+/USB_SSTX3-: USB Super Speed Port #3 transmit differential pair

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

$+5V_{USB2}$ and $+5V_{USB3}$ are derived from +5V_ALW through a 1A current limited power switch.

GBE0_MDI0+/GBE0_MDI0-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #0. It is the first differential pair in Gigabit Ethernet mode, and the Transmit differential pair in 10/100 Mbps modes.

GBE0_MDI1+/GBE0_MDI1-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #1. It is the second differential pair in Gigabit Ethernet mode, and the Receive differential pair in 10/100 Mbps modes.

GBE0_MDI2+/GBE0_MDI2-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #2. It is the third differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

GBE0_MDI3+/GBE0_MDI3-: Ethernet Controller #0 Media Dependent Interface (MDI) I/O differential pair #3. It is the fourth differential pair in Gigabit Ethernet mode; it is not used in 10/100Mbps modes.

! Please be aware that USB 3.0 connectivity can be obtained only in case that it is supported by the COM Express™ module plugged onto the Carrier Board.

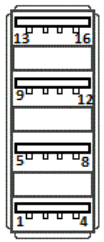
In case the COM Express™ module used doesn't offer USB 3.0 ports, it will be always possible to use USB 2.0 ports, simply by plugging an USB 2.0 cable.

Avoid using USB 3.0 cables if the COM Express™ module used doesn't offer such an interface.

USB 2.0 ports #4#5#6#7 Quad Type-A socket - CN20

Pin	Signal	Pin	Signal
1	$+5V_{USB4}$	5	$+5V_{USB5}$
2	USB_4-	6	USB_5-
3	USB_4+	7	USB_5+
4	GND	8	GND
9	$+5V_{USB6}$	13	$+5V_{USB7}$
10	USB_6-	14	USB_7-
11	USB_6+	15	USB_7+
12	GND	16	GND

Other than the USB 3.0 ports available through the standard connectors CN18 and CN19, there are other four USB 2.0 ports (#4, #5 #6 and #7) coming out from COM Express™ module that can be used for the connection of external devices.



These four USB 2.0 ports are available on a standard quad Type-A receptacle socket, type Adam Tech p/n USB-A-Q-RA.

More specifically, USB 2.0 port #4 is carried to the lower USB receptacle of CN20, USB 2.0 port #5 is carried to the above receptacle and so on, up to USB 2.0 port #7 that is carried to the upper level of USB receptacle CN20.

Signal description:

USB_4+/USB_4-: USB 2.0 Port #4 differential pair

USB_5+/USB_5-: USB 2.0 Port #5 differential pair

USB_6+/USB_6-: USB 2.0 Port #6 differential pair

USB_7+/USB_7-: USB 2.0 Port #7 differential pair

Common mode chokes are placed on all USB differential pairs for EMI compliance.

For ESD protection, on all data and voltage lines are placed clamping diodes for voltage transient suppression.

$+5V_{USB4}$, $+5V_{USB5}$, $+5V_{USB6}$, $+5V_{USB7}$, are derived from +5V_ALW through a 600mA current limited power switch.

USB Overcurrent header – CN55			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	USB_0_1_OC#
3	GND	4	USB_2_3_OC#
5	GND	6	USB_4_5_OC#
7	GND	8	USB_6_7_OC#

For debugging purposes, onboard it is also available an 8-pin connector, type Adimpex p/n LE008208-R or equivalent, for the connection of USBx_EN_OC# signals.

USB_0_1_OC#: USB over-current sense signal for USB channels #0 and #1. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

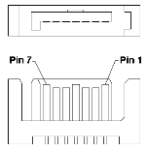
USB_2_3_OC#: USB over-current sense signal for USB channels #2 and #3. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

USB_4_5_OC#: USB over-current sense signal for USB channels #4 and #5. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

USB_6_7_OC#: USB over-current sense signal for USB channels #6 and #7. Active Low Input Signal, electrical level +3.3V_ALW, manged by COM Express™ module.

3.3.7 S-ATA Connectors

For the connection of external Mass Storage Devices, there are four standard male 7 poles SATA connectors, CN21,CN22,CN24,CN25, type WINNING p/n WATM-07ABN4B2B8UW or equivalent.



These connectors carry out directly SATA port #0 #1 #2 and #3 signals coming from COM Express™ module's connector. Each SATA channel is composed by two differential pairs, SATA_TxX and SATA_RxX.

Please notice that each SATA connector will work only in case the COM Express™ module carries out SATA Channel #0 #1 #2 #3 on COM Express™ connector

In case the COM Express™ module used doesn't have these signals connected, then one or more of these connectors will not be usable.

SATA #0 Connector – CN24	
Pin	Signal
1	GND
2	SATA0_Tx+
3	SATA0_Tx-
4	GND
5	SATA0_Rx-
6	SATA0_Rx+
7	GND

SATA #1 Connector – CN25	
Pin	Signal
1	GND
2	SATA1_Tx+
3	SATA1_Tx-
4	GND
5	SATA1_Rx-
6	SATA1_Rx+
7	GND

SATA #2 Connector – CN21	
Pin	Signal
1	GND
2	SATA2_Tx+
3	SATA2_Tx-
4	GND
5	SATA2_Rx-
6	SATA2_Rx+
7	GND

SATA #3 Connector – CN22	
Pin	Signal
1	GND
2	SATA3_Tx+
3	SATA3_Tx-
4	GND
5	SATA3_Rx-
6	SATA3_Rx+
7	GND

Here following the signals related to SATA interface:

SATA0_TX+/SATA0_TX-: Serial ATA Channel #0 Transmit differential pair.

SATA0_RX+/SATA0_RX-: Serial ATA Channel #0 Receive differential pair.

SATA1_TX+/SATA1_TX-: Serial ATA Channel #1 Transmit differential pair.

SATA1_RX+/SATA1_RX-: Serial ATA Channel #1 Receive differential pair.

SATA2_TX+/SATA2_TX-: Serial ATA Channel #2 Transmit differential pair.

SATA2_RX+/SATA2_RX-: Serial ATA Channel #2 Receive differential pair.

SATA3_TX+/SATA3_TX-: Serial ATA Channel #3 Transmit differential pair.

SATA3_RX+/SATA3_RX-: Serial ATA Channel #3 Receive differential pair.

3.3.8 Feature pin Header

Feature internal pin header – CN27			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V_ALW (with 1.5 resettable fuse)	2	+3.3V_RUN (with 1.5 resettable fuse)
3	SMB_CK	4	I2C_CK
5	SMB_DAT	6	I2C_DAT
7	GND	8	GND
9	THRMTRIP#	10	THRM#
11	BUF_SUS_S5#	12	BUF_SUS_S4#
13	BUF_SUS_S3#	14	WDT
15	PWR_BTN#	16	EXT_WAKE#
17	SLEEP#	18	TPM_PP
19	GND	20	GND

For further expandability of the system, on board there is an expansion connector, which carries out the signals related to I2C bus, SM Bus, Watchdog and Power Management signals. These signals allow implementing, through external expansion modules, further functionalities that are not already realised by the carrier board.

For this purpose, it is available a dual row, 20 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008220-R or equivalent, with the pinout shown in the table on the left.

All the signals available on this connector come out directly from the COM Express™ connector.

Signal description:

SMB_CK: SM Bus control clock line for System Management, bidirectional signal

SMB_DAT: SM Bus control data line for System Management, bidirectional signal

I2C_CK: General purpose I2C port clock output

I2C_DAT: General purpose I2C port data I/O line

THRMTRIP#: Active low output signal. This signal is used to communicate that, due to excessive overheating, the CPU has entered thermal shutdown in order to prevent physical damages

THRM#: Thermal Alarm Input from off-Module temperature sensor indicating an overheating situation, so that the CPU can begin thermal throttling. Active Low Input signal

BUF_SUS_S3#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Suspend to RAM (S3) state

BUF_SUS_S4#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Suspend to Disk (S4) state

BUF_SUS_S5#: this signal, in reality, doesn't come directly from COM Express™ module, it is biased using a Ultra High Speed CMOS buffer. Active Low Output Signal, +3.3V_ALW electrical level with 100kΩ pull down resistor, indicating that the system is in Soft Off (S5) state

WDT: Watchdog event indicator Output. When this signal goes high (active), it reports that internal Watchdog's timer expired without being triggered, neither via HW nor via SW. It is an active high signal

PWR_BTN#: Power Button event signal input, used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. Active low output signal. This signal can be directly driven by M2 pushbutton (par. 3.3.23) and upon its pressure, the pulse of this signal will let the switched voltage rails turn on or off

WAKE1#: General Purpose Input wake up signal used to report that a general Wake-up event has occurred, and consequently the module must turn itself on. Active Low Input signal

SLEEP#: Sleep Button event signal input, used to bring a system in sleep state or wake it up again. Active Low Input signal. This signal can be directly driven by M4 pushbutton (par. 3.3.23) and upon its pressure, the pulse of this signal will let the transition of the module from Working to Sleep status, or vice versa

TPM_PP: Trusted Platform Module (TPM) Physical Presence Active high Input Signal

3.3.9 External BIOS SPI Flash header

External BIOS Flash Header – CN28			
Pin	**Signal**	**Pin**	**Signal**
1	SPI_CS#	2	SPI_POWER
3	SPI_MISO	4	SPI_HOLD#
5	SPI_WP#	6	SPI_CLK
7	GND	8	SPI_MOSI

In case that an external Flash is needed, then on the carrier board it is provided access to this interface through a dual-row 8-pin SMT male pin-header, p. 1.27mm, type TOWNES P1035-2*04MGF-084-D or equivalent, with pinout shown in the table on the left.

Signal description:

SPI_CS#: Chip Select Signal for SPI device, Active Low Output Signal, SPI_POWER electrical level

SPI_MISO: Data in to COM Express™ Module from Carrier SPI device

SPI_WP#: this signal is tied, through a 10kΩ resistor, to SPI_POWER signal. This means that when the Flash is powered, the protection from writing is automatically removed.

SPI_POWER: Dedicated Power supply sourced from COM Express™ Module for SPI devices. +3.3V or +1.8V electrical level depending on the module.

SPI_HOLD#: this signal too is tied, through a 10kΩ resistor, to SPI_POWER signal. This means that when the Flash is powered, the Hold condition of serial communication is automatically removed.

SPI_CLK: Clock from COM Express™ Module to Carrier SPI device

SPI_MOSI: Data out from COM Express™ Module to Carrier SPI device

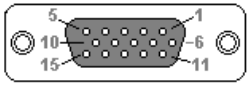
3.3.10 BIOS disable signals

According to COM Express™ Specifications rev. 3.0, there are two jumpers on board JP7 and JP8, which allow configuring the BIOS_DIS[0..1]# signals according to the table below.

JP8 position	JP7 position	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	BIOS Entry
Not inserted	Not inserted	Module	Module	High	Module	SPI0/SPI1
Not inserted	Inserted	Module	Module	High	Module	Carrier FWH
Inserted	Not inserted	Module	Carrier	SPI0	Carrier	SPI0/SPI1
Inserted	Inserted	Carrier	Module	SPI1	Module	SPI0/SPI1

3.3.11 VGA Connector

VGA DB15 connector - CN30			
Pin	Signal	Pin	Signal
1	RED	2	GREEN
3	BLUE	4	N.C.
5	GND	6	GND
7	GND	8	GND
9	+5V_VGA	10	GND
11	N.C.	12	CRT_I2C_DAT
13	HSYNC	14	VSYNC
15	CRT_I2C_CK		



For use of standard VGA monitors, all RGB signals coming from COM Express™ CPU module are carried out on a standard DB15 HD Female connector CN30,type NELTRON p/n 5511-15F-HR-02 or equivalent, raised (so that can be placed over one of the DP++ connectors). Pinout follows VGA VESA DDC2 standard; related pinout is reported in the table on the left.

RED: VGA Red Signal video output.

GREEN: VGA Green Signal video output.

BLUE: VGA Blue Signal video output.

HSYNC: VGA Horizontal Synchronization output signal.

VSYNC: VGA Vertical Synchronization output signal.

CRT_I2C_CLK: VGA's DDC Clock line for displays detection, +5V_VGA electrical level with 2k2Ω pull up resistor

CRT_I2C_DATA: VGA's DDC Clock line for displays detection, +5V_VGA electrical level with 2k2Ω pull up resistor

+5V_VGA: VGA power, directly obtained by +5V_RUN through a resettable fuse and a Schottky diode in series.

All of these signals are derived directly from COM Express™ module's VGA_xxxx corresponding signals, by placing ESD protections, EMI filters and voltage level shifters for DDC lines.

3.3.12 FuSa Header

FuSa Header – J1			
Pin	**Signal**	**FuSa Interface**	**Raw FuSa Interface**
1	+5V_ALW (with 1.5 resettable fuse)		
2	+12V_RUN (with 1.5 resettable fuse)		
3	GND		
4	GND		
5	RSVD#C17	FUSA_OKNOK0	FUSA_ERR0
6	RSVD#C18	FUSA_OKNOK1	FUSA_ERR1
7	RSVD#D17	FUSA_ALERT#	FUSA_ERR2
8	RSVD#D18	FUSA_SPIS_CS#	FUSA_SPI_CS#
9	RSVD#D24	FUSA_SPIS_SCLK	FUSA_SPI_SCLK
10	RSVD#D25	FUSA_SPIS_MISO	FUSA_SPI_MISO
11	RSVD#C27	FUSA_SPIS_MOSI	FUSA_SPI_MOSI
12	RSVD#C28	FUSA_CHXPMICEN_IN	FUSA_CHXPMICEN_IN
13	RSVD#D28	FUSA_CHXPMIC_EN	
14	RSVD#C35	FUSA_CHXRLYSWITCH	
15	RSVD#D35	FUSA_CHXOKNOK0	EXT_SI_ALERT#
16	RSVD#D38	FUSA_CHXOKNOK1	FUSA_GPP_U4
17	RSVD#C45	FUSA_SPIM_CS#	FUSA_I2C_CLK
18	RSVD#D45	FUSA_SPIM_SCLK	FUSA_I2C_DAT
19	RSVD#C48	FUSA_SPIM_MISO	FUSA_DIAGTEST_MODE
20	RSVD#D48	FUSA_SPIM_MOSI	FUSA_DIAGTEST_EN
21	RSVD#C63	FUSA_PROCHOT	FUSA_PROCHOT#
22	RSVD#C64	FUSA_THERMTRIP	FUSA_THERMTRIP#
23	RSVD#D63		FUSA_CATERR#

According to COM Express™ Specifications rev. 3.0, the COM Express™ card edge connector does provide additional reserved signals intended to be used for future use.

On CCOMe-C96 Carrier Board, these signals are carried out to a dual row, 28 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008228-R, with the pinout shown in the table on the left.

This connector is used to provide functional safety functions for FuSa applications through signals listed in left table.

Please be aware that FuSa functionality can be obtained only in case that it is supported by the COM Express™ module plugged onto the Carrier Board.

Please refer to specific COM Express™ module for a signal description related to this section.

24	RSVD#D64		FUSA_PCHHOT#
25	RSVD#C77	FUSA_POWERFAIL#	FUSA_POWERFAIL#
26	SYS_RESET#		
27	PS_ON#		
28	PWR_BTN#		

3.3.13 GPIO pin header / microSD Card Slot

GPIO pin header – CN31			
Pin	**Signal**	**Pin**	**Signal**
1	GPO0	2	+3.3V_ALW (with 1.5 resettable fuse)
3	GPO1	4	GPI0
5	GPO2	6	GPI1
7	GPO3	8	GPI2
9	GND	10	GPI3

JP10 position	GPIO/microSD selector
Not inserted	GPIO
Inserted	microSD

According to the release 3.0 of COM Express™ specifications, on the same pins are multiplexed the signals necessary for the implementation of 4-bit SD cards with four General Purpose Inputs plus four general Purpose Outputs. Effective support of GPI+GPO signals or SDIO interface depends on the module used. Please refer to the User Manual of the COM Express™ module used for a detail about the interface support.

The selection between SD Card interface and GPI/O interface is made using jumper JP10, according to the table on the left.

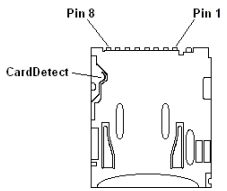
If supported by the COM Express™ module installed on CCOMe-C96, the GPIO interface, is available on CN31, which is a dual row, 10 pin, P2.54mm standard pin header, type ADIMPEX p/n LE008210-R, with the pinout shown in the table on the left. To redirect the signal coming directly from COM Express™ module to GPIO header, jumper JP10 doesn't have to be inserted.

GPO[0:3]: General purpose output signals

GPI[0:3]: General purpose input signals

µSD Card Slot – CN33	
Pin	**Signal**
1	SDIO_DAT2
2	SDIO_DAT3
3	SDIO_CMD
4	+3.3V_RUN
5	SDIO_CLK
6	GND
7	SDIO_DAT0
8	SDIO_DAT1
CardDetect	SD_CD#

The SD interface is carried to a standard µSD card slot (CN33), soldered on bottom side of the module, push-push type, H=1.68 mm, type JST DM3AT-SF-PEJM5 or equivalent. When this interface is available, this card slot is accessible with jumper JP10 inserted.



Signals description

SD_CD#: Card Detect Input. This signal is grounded when the card is inserted.

SD_CLK: SD Clock Line (output).

SD_CMD: Command/Response bidirectional line.

SDIO_DAT[0÷3]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode.

3.3.14 Front Panel Header

Switch / LED Header Interface - CN34			
Pin	**Signal**	**Pin**	**Signal**
1	HD_LED_P	2	FP PWR_P/SLP_N
3	HD_LED_N	4	FP PWR_N/SLP_P
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	+5V_RUN		

To allow the integration of a COM Express™ module based system inside a box PC-like, there is a connector on the carrier board that allows to remote signals for the Power Button (to be used to put the system in a Soft Off State, or awake from it), for the Reset Button, and the signal for optional LED signalling activity on SATA Channel and Power On states.

The pinout of this connector complies with Intel® Front Panel I/O connectivity Design Guide, Switch/LED Front Panel section, chapter 2.2.

Connector CN34 is an internal 9-pin standard male pin header, p 2.54 mm, 5+4 pin, h= 6mm, type NELTRON p/n 2213S-10G-E10 or equivalent.

Signals Description:

HD_LED_P: Hard Disk Activity LED signal's pull-up to +5V_RUN voltage (510Ω pull-up).

HD_LED_N: Hard Disk Activity LED output signal.

RST_SW_N: Reset Switch GND.

RST_SW_P: Reset switch input signal SYS_RESET#. This signal can be connected to an external momentary pushbutton (contacts normally open). When the pushbutton is pressed, the pulse of Reset signal will cause the reset of the board.

PWR_SW_P: Power switch input signal, open drain. This signal can be connected to an external momentary pushbutton (contacts normally open). Upon the pressure of this pushbutton, the pulse of this signal will let the switched voltage rails turn on or off.

PWR_SW_N: Power Switch GND.

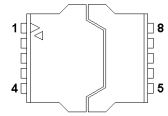
FP PWR_P/SLP_N: Power/Sleep messaging LED terminal 1 with 510Ω pull-up resistor to +5V_ALW voltage. Connect it to an extremity of a dual-colour power LED for power ON/OF, sleep and message waiting signalling. Please refer to Intel® Front Panel I/O connectivity Design Guide, chapter 2.2.4, for LED functionalities and signal meaning.

FP PWR_N/SLP_P: Power/Sleep messaging LED terminal 2 with 510Ω pull-up resistor to +5V_ALW voltage. Connect it to the other extremity of the dual-colour power LED above mentioned.

Please be aware that the power switch input signal and the reset switch input signal are also managed directly on the carrier board by the two pushbuttons M2 and M1 (respectively), so it is not mandatory to connect them externally using CN34.

3.3.15 External EEPROM I2C Flash socket

External EEPROM I2C Flash socket – CN35			
Pin	**Signal**	**Pin**	**Signal**
1	4.7kΩ pull-up +3.3V_ALW	5	I2C_DAT
2	4.7kΩ pull-up +3.3V_ALW	6	I2C_CLK
3	4.7kΩ pull-up +3.3V_ALW	7	I2C_Write Protect (GND)
4	GND	8	+3.3V_ALW



The I2C bus coming from COM Express™ module is carried directly to Feature pin Header (see par.3.3.8Errore. L'origine riferimento non è stata trovata.).

It is also used to manage an SO8 EEPROM Socket CN35, type LOTES p/n ASPI0001-P001A, for plugging I2C Flash in SO-8 format.

The I2C_Write Protect function is disabled for this board (signal tied to GND).

I2C_DAT: General purpose I2C port data I/O line

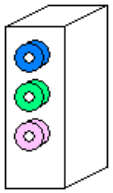
I2C_CLK: General purpose I2C port clock output

3.3.16 Audio Section

COM Express™ specifications include an HD Audio dedicated interface. For this reason, on the carrier board there is an HD Audio Codec, type Cirrus Logic p/n CS4207-CNZR.

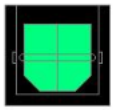
Triple Audio Jack – CN36	
Colour	**Signal**
Light Blue	Line IN (Left + Right)
Light Green	Front_OUT (Left + Right)
Pink	MIC1 IN (Left + Right)

Standard Stereo audio signals are carried on a standard HD Stereo triple jack connector, type LOTES ABA-JAK-028-K07 (light blue/light green/pink) or equivalent.



S/PDIF OUT connector – CN56	
Pin	**Signal**
1	GND
2	+5V_RUN
3	S/PDIF_OUT

Directly managed by Cirrus Logic CS4207-CNZR High Definition Audio Codec, there is also one S/PDIF optical connector, for the link to digital audio media. Connector is type SIMULA p/n OJ103B-T602 or equivalent.



HD Audio Front Panel Header – CN38			
Pin	**Signal**	**Pin**	**Signal**
1	Mic2_In_L	2	Audio_GND
3	Mic2_In_R	4	---
5	Line_Out_R	6	Sense1_Return
7	Audio_GND		
9	Line_Out_L	10	Sense2_Return

JP14 position	Mic1 / Mic2 selector
Not inserted	Mic2
Inserted	Mic1

Signals Description:

Mic2_In_L: Microphone Left Channel.

Mic2_In_R: Microphone Right Channel.

Sense1_return: Microphone Jack detection return signal.

Line_Out_L: Line Out Left Channel.

Line_Out_R: Line Out Right Channel.

Sense2_return: Line Out Jack detection return signal.

In order to give the maximum flexibility to CCOMe-C96 carrier board, it is also available a dedicated 9-pin 2.54mm pitch Pin header CN38, type NELTRON p/n 2213S-10G-E8, for external connection of a second Mic In and a Line Out. These additional audio inputs are managed by the same Cirrus Logic CS4207-CNZR Audio Codec.

Selection between Mic1 In available at pink jack of CN36 and Mic2 In available at HD Audio header CN38 is made by jumper JP14.

Pinout hereby shown is compliant to "Intel® Front Panel I/O connectivity Design Guide" specifications, par. 2.3.5 Table 7.

Using this dedicated connector CN38, it will be possible to connect any Azalia compliant panel audio jack to remote audio connectors in the preferred position.

3.3.17 eDP Connector

eDP connector – CN42			
Pin	**Signal**	**Pin**	**Signal**
1	N.C.	21	VDD_LCD
2	VDD_BKLT	22	VDD_LCD
3	VDD_BKLT	23	VDD_LCD
4	VDD_BKLT	24	GND
5	VDD_BKLT	25	eDP_AUX-
6	N.C.	26	eDP_AUX+
7	N.C.	27	GND
8	LCD_BKLT_CTRL	28	eDP_TX0+
9	LCD_BKLT_EN	29	eDP_TX0-
10	GND	30	GND
11	GND	31	eDP_TX1+
12	GND	32	eDP_TX1-
13	GND	33	GND
14	eDP_HPD	34	eDP_TX2+
15	GND	35	eDP_TX2-
16	GND	36	GND
17	GND	37	eDP_TX3+
18	GND	38	eDP_TX3-
19	N.C.	39	GND
20	VDD_LVDS	40	---

The CCOMe-C96 carrier board is also able to manage eDP Displays.

For the connection of this kind of displays, on-board there is a VESA® certified connectors for embedded Display Port interface, type STARCONN p/n 300E40-0110RA-G3 or equivalent (microcoaxial cable connector, 0.5mm pitch, 40 positions).

On this connector, VDD_BKLT and VDD_LCD are the voltage rails that can be used to supply the Backlight Unit and related LCD.

The eDP Interface is derived by placing an high-speed differential switch on shared LVDS/eDP interface coming from COM Express™ Connector. It is the same switch that makes available the LVDS interface on LVDS connector (please check par. 3.3.18).

The switching between eDP interface and LVDS is controlled via a jumper JP11, according to the table below.

Here following the signals involved in eDP management:

eDP_TX0+/eDP_TX0-: embedded DP differential data pair #0.

eDP_TX1+/eDP_TX1-: embedded DP differential data pair #1.

eDP_TX2+/eDP_TX2-: embedded DP differential data pair #2.

eDP_TX3+/eDP_TX3-: embedded DP differential data pair #3.

eDP_AUX+/eDP_AUX-: embedded DP auxiliary channel differential data pair.

eDP_HPD: embedded DP Hot Plug Detect. Active high signal, +3.3V_RUN electrical level

LCD_BKLT_EN: eDP Panel's Backlight Enable Signal. +3.3V_RUN electrical level Output.

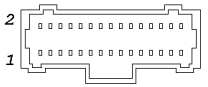
LCD_BKLT_CTRL: eDP Panel Backlight Brightness Control, PWM signal.

JP11 position	eDP/LVDS selector
Inserted	eDP enabled
Not inserted	LVDS enabled

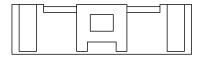
3.3.18 LVDS Connector

LVDS connector – CN44			
Pin	Signal	Pin	Signal
2	VDD_BKLT	1	VDD_LCD
4	VDD_BKLT	3	VDD_LCD
6	VDD_BKLT	5	VDD_LCD
8	GND	7	3.3V_RUN
10	LVDS0_D0+_CONN	9	GND
12	LVDS0_D0-_CONN	11	LVDS0_D1+_CONN
14	GND	13	LVDS0_D1-_CONN
16	LVDS0_D2+_CONN	15	GND
18	LVDS0_D2-_CONN	17	LVDS0_D3+_CONN
20	GND	19	LVDS0_D3-_CONN
22	LVDS0_CLK+_CONN	21	GND
24	LVDS0_CLK-_CONN	23	LVDS1_D0+_CONN
26	GND	25	LVDS1_D0-_CONN
28	LVDS1_D1+_CONN	27	GND
30	LVDS1_D1-_CONN	29	LVDS1_D2+_CONN
32	GND	31	LVDS1_D2-_CONN
34	LVDS1_D3+_CONN	33	GND
36	LVDS1_D3-_CONN	35	LVDS1_CLK+_CONN
38	GND	37	LVDS1_CLK-_CONN
40	GND	39	GND
42	LCD_BKLT_CTRL	41	LCD_BKLT_EN
44	LCD_VDD_EN	43	LCD_BKLT_AN_CTRL
46	---	45	---
48	---	47	---
50	LVDS_I2C_CLK	49	LVDS_I2C_DAT

CCOMe-C96 board allows to interface to Single/Dual Channel 18-/24-bit displays, using the LVDS channel coming directly from the COM Express™ module.



The LVDS interface will be available on a connector type HR A1014WV-S-2x25P or equivalent (2 x 25p, male, straight, P1, low profile, polarised), with the pin-out shown in the table on the left.



Mating connector: HR A1014H-2X25P with HR A1014-T female crimp terminals.

Alternative mating connector, MOLEX 501189-5010 with crimp terminals series 501334.

On the same connectors, are also implemented signals for direct driving of display's backlight: voltages (VDD_BKLT and VDD_LCD) and control signals (LCD enable signal, LCD_VDD_EN, Backlight enable signal, LCD_BKLTEN, and Backlight Brightness Control signal, LCD_BKLT_PWM and LCD_BKLT_AN_CTRL).

When building a cable for connection of LVDS displays, please take care of twist as tight as possible differential pairs' signal wires, in order to reduce EMI interferences. Shielded cables are also recommended.

1 3

JP13 position	LCD Power selector
1-2	+5V_RUN
2-3	+3.3V_RUN

JP12 position	Backlight Power selector
1-2	+12V_RUN
2-3	+5V_RUN

VDD_LCD: LCD Voltage rail. Its value can be set to +3.3V_RUN or +5V_RUN by using dedicated jumper JP13, which is a standard pin header, P2.54mm, 1x3 pin.

1 3

VDD_BKLT: Backlight Voltage rail. Its value can be set to +5V_RUN or +12V_RUN by using dedicated jumper JP12, same of JP13.

Signal Description:

LVDS0_D[0..3]+ / LVDS0_D[0..3]-: COM Express™ Module LVDS Channel#0 Differential pairs

LVDS0_CLK+ / LVDS0_CLK-: COM Express™ Module LVDS Channel#0 Differential clock

LVDS1_D[0..3]+ / LVDS1_D[0..3]-: COM Express™ Module LVDS Channel#1 Differential pairs

LVDS1_CLK+ / LVDS1_CLK-: COM Express™ Module LVDS Channel#1 Differential clock

LVDS_I2C_DAT: COM Express™ Module Display ID Data line for LVDS flat Panel detection.

LVDS_I2C_CLK: COM Express™ Module Display ID Clock line for LVDS flat Panel detection

LCD_VDD_EN: LVDS Panel power for LCD Enable Signal, controlled by the COM Express™ Module directly. +3.3V_RUN electrical level Output.

LCD_BKLT_EN: LVDS Panel power for Backlight Enable Signal, controlled by the COM Express™ Module directly. +3.3V_RUN electrical level Output.

LCD_BKLT_CTRL: LVDS Panel Backlight Brightness Control, PWM signal controlled by the COM Express™ Module directly

LCD_BKLT_AN_CTRL: LVDS Panel Backlight Brightness Analog Dimming Control, derived from LCD_BKLT_CTRL, for direct analogic control of backlights not supporting PWM.

LVDS External EDID Flash Header – CN45

Pin	Signal	Pin	Signal
1	4.7kΩ pull-up +3.3V_RUN	2	+3.3V_RUN
3	4.7kΩ pull-up +3.3V_RUN	4	DID_WP#
5	4.7kΩ pull-up +3.3V_RUN	6	LVDS_I2C_CLK
7	GND	8	LVDS_I2C_DAT

In order to allow the usage of LVDS panels with not-standard timings, on the carrier board there is a 8-pin header, type TOWNES p/n P1035-2*04MGF-084-D, for the external connection of I2C EEPROMs

LVDS_I2C_DAT: COM Express™ Module Display ID Data line

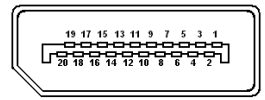
LVDS_I2C_CLK: COM Express™ Module Display ID Clock line

DID_WP#: I2C Write Protect Signal, active low output, +3.3V_RUN electrical level with 4k7Ω pull up resistor

3.3.19 DP++ Connectors

According to COM Express™ specifications, Type 6 pinout defines three Digital Display interfaces (DDI), that can be used to carry out DisplayPort and TMDS (HDMI/DVI) interface.

On MC96 Carrier board, these interfaces are carried to as many right-angle single DP connectors, supporting DP++ (so that it is possible to connect also HDMI and DVI displays by using external adapters).



DDI1,DDI2 and DDI3 are carried out directly on standard DisplayPort Connectors, CN52,CN53 and CN54, type WINNING p/n WDPE-20F3L1BU3 or equivalent, with the pinout shown in the following table.

Multimode DP#1 Connector – CN52

Pin	Signal	Pin	Signal
1	DDI1_PAIR0+	2	GND
3	DDI1_PAIR0-	4	DDI1_PAIR1+
5	GND	6	DDI1_PAIR1-
7	DDI1_PAIR2+	8	GND
9	DDI1_PAIR2-	10	DDI1_PAIR3+
11	GND	12	DDI1_PAIR3-
13	DDI1_DDC_AUX_SEL	14	DDI1_CEC
15	DDI1_CTRLCLK_AUX+	16	GND
17	DDI1_CTRLDATA_AUX-	18	DDI1_HPD
19	GND	20	+3.3V_RUN

Multimode DP#2 Connector – CN53

Pin	Signal	Pin	Signal
1	DDI2_PAIR0+	2	GND
3	DDI2_PAIR0-	4	DDI2_PAIR1+
5	GND	6	DDI2_PAIR1-
7	DDI2_PAIR2+	8	GND
9	DDI2_PAIR2-	10	DDI2_PAIR3+
11	GND	12	DDI2_PAIR3-
13	DDI2_DDC_AUX_SEL	14	DDI2_CEC
15	DDI2_CTRLCLK_AUX+	16	GND
17	DDI2_CTRLDATA_AUX-	18	DDI2_HPD
19	GND	20	+3.3V_RUN

Multimode DP#3 Connector – CN54

Pin	Signal	Pin	Signal
1	DDI3_PAIR0+	2	GND
3	DDI3_PAIR0-	4	DDI3_PAIR1+
5	GND	6	DDI3_PAIR1-
7	DDI3_PAIR2+	8	GND
9	DDI3_PAIR2-	10	DDI3_PAIR3+
11	GND	12	DDI3_PAIR3-
13	DDI3_DDC_AUX_SEL	14	DDI3_CEC
15	DDI3_CTRLCLK_AUX+	16	GND
17	DDI3_CTRLDATA_AUX-	18	DDI3_HPD
19	GND	20	+3.3V_RUN

Signal Description:

DDIx_PAIR0+/DDIx_PAIR0-: DDI Interface #x Differential Pair #0. Can be used as Display Port differential pair #0 or TMDS (HDMI) differential pair #2.

DDIx_PAIR1+/DDIx_PAIR1-: DDI Interface #x Differential Pair #1. Can be used as Display Port differential pair #1 or TMDS (HDMI) differential pair #1.

DDIx_PAIR2+/DDIx_PAIR2-: DDI Interface #x Differential Pair #2. Can be used as Display Port differential pair #2 or TMDS (HDMI) differential pair #0.

DDIx_PAIR3+/DDIx_PAIR3-: DDI Interface #x Differential Pair #3. Can be used as Display Port differential pair #3 or TMDS (HDMI) Clock differential pair.

DDIx_CTRLCLK_AUX+/DDIx_CTRLDATA_AUX-: DDI Interface #x, Auxiliary channel for Display Port (differential pair) or DDC Clock and Data Line for TMDS.

DDIx_HPD: DDI Interface #x Hot Plug Detect. This signal is tied to GND through a 100kΩ resistor.

DDIx_DDC_AUX_SEL: DDI Interface #x Cable Adapter Detect signal. When this signal is detected high, then on the connector there is the TMDS interface (it means that a DP-to-HDMI adapter is connected). This signal is tied to GND through a 1MOhm resistor.

DDIx_CEC: this signal is tied to GND through a 5.1MOhm resistor.

3.3.20 POST Code Display

For debugging purposes, it is available a display made by 4x 7-segment LED display, type Kingbright KCSC02-105 or equivalent.

The management of this display is done using a LC4064V-75TN44I CPLD, driven through the COM Express™ LPC Bus

3.3.21 JTAG Connector

JTAG Connector – CN16			
Pin	Signal	Pin	Signal
1	+3.3V_RUN	5	POST_TDO
2	GND	6	POST_TDI
3	POST_TCK	7	POST_TMS
4	N.C.		

For the programming of CPLD used to manage POST Code Display, it is available a JTAG connector CN16, which is a single row, 7 pin, P2.54mm standard pin header, type ADIMPEX p/n NPE08007-R.

POST_TCK: JTAG Test Clock Signal, 4k7Ω pull down resistor

POST_TDO: JTAG Test Data Out Signal

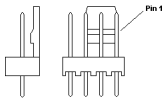
POST_TDI: JTAG Test Data In, +3.3V_RUN with 4k7Ω pull up resistor

POST_TMS: JTAG Test Mode Select, +3.3V_RUN with 4k7Ω pull up resistor

3.3.22 FAN Connector

FAN Connector – CN32	
Pin	Signal
1	GND
2	FAN_PWR
3	FAN_TACHO_IN
4	FAN_PWM

Onboard it is available a 4-pin connector, type MOLEX p/n 47053-3000 or equivalent, for the connection of tachometric FANs. Please be aware that the use of an external fan depends strongly on customer's application/installation. Fan Speed control must be supported by COM Express™ module through signals FAN_TACHIN and FAN_PWMOUT. Please refer to chapter 4.1 for considerations about thermal dissipation.



FAN_PWR: +12V_RUN derived power rail for FAN, managed by PWM signal FAN_PWMOUT coming from COM Express™ connector. FAN_PWR is fixed +12V_RUN in 4-wires Fan, while is pulse width modulated via FAN_PWMOUT for 3-wires Fan

FAN_TACHO_IN: tachometric input from the fan to the COM Express™ module

JP9 position	FAN driver mode selector
1-2	4-Wires Fan
2-3	3-Wires Fan

FAN_PWM: PWM output to the fan, +5V_RUN electrical level with 10kΩ pull up resistor. Only used in 4-wires Fan.

As stated above, by using a dedicate jumper JP9, it is possible to select if FAN_PWR is fixed to +12V_RUN, in order to support 4-wire tachometric fans, or must be controlled by the signal FAN_PWMOUT, coming directly from COM Express™ module, in order to support 3-wire tachometric fans.

3.3.23 Buttons

On the carrier board, there are four momentary pushbuttons (with contacts normally open) for the direct handling of COM Express™ power management signals.

The first pushbutton, M1, is placed on SYS_RESET# signal. Upon the pressure of this pushbutton, the COM Express™ module will perform a reset.

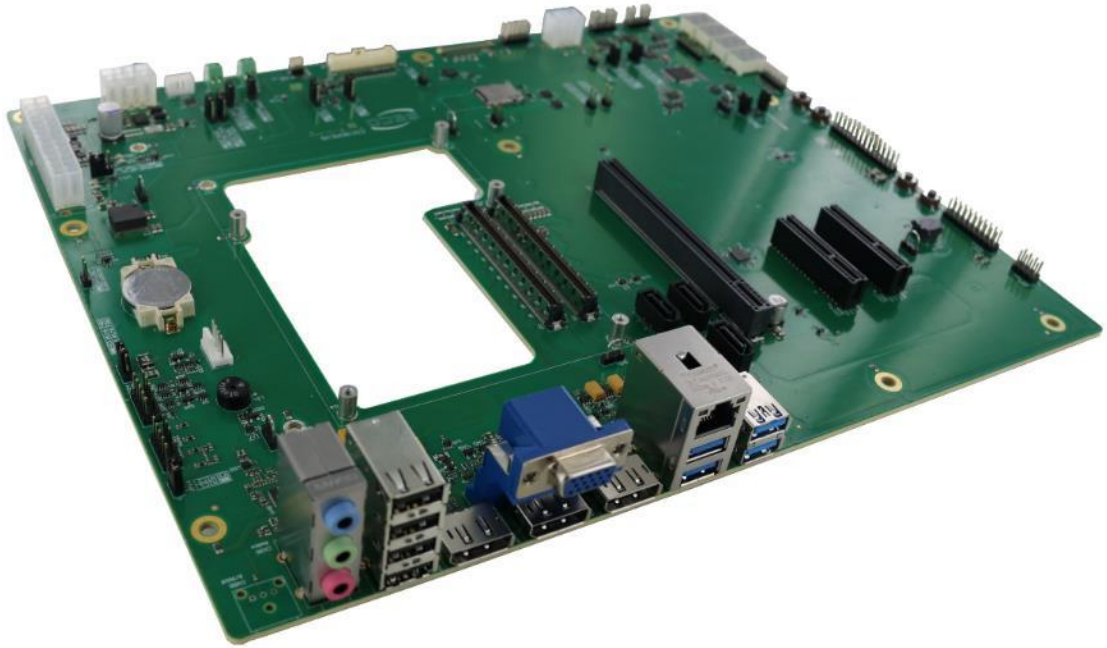
The second pushbutton, M2, is placed on POWER_BTN# signal. Upon the pressure of this pushbutton, the COM Express™ module will perform a power up / power down sequence.

The third pushbutton, M3, is placed on LID # signal. Such a signal can be used by the COM Express™ module to detect the opening / the closure of an external lid switch, like those used to detect opening / closure of the notebooks. Upon changes in LID # state, the OS could trigger the transition of the module from Working to Sleep status, or vice versa.

The fourth pushbutton, M4, is placed on SLEEP# signal. Upon the pressure of this pushbutton, the COM Express™ module will enter in a sleep state (if such states are supported by the module).

Chapter 4.
Appendices

- Thermal Design
- Accessories



4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like COM Express™ modules, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

COM Express™ specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the COM Express™ module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on.

Conversely, heatsinks in some situation can represent a cooling solution. Until the modules are used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink with fan could be sufficient for modules' cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat.

Indeed, when using CCOMe-C96 carrier board with any COM Express™ module, it is necessary to consider carefully the global heat generated by the system, and the scenario of utilisation.

Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide COM Express™ modules' specific heatspreaders and heatsinks (active and passive), but please remember that their use must be evaluated accurately inside the final system (electronics + mechanics), and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions, which also keeps the surface temperature of all carrier board's components in the temperature range specified for the specific carrier board configuration (industrial or commercial grade).

4.2 Accessories

The CCOMe-C96 Carrier Board will not be sold alone, but as a part of a more comprehensive Development kit, like those already available for Qseven Carrier boards and also for COM Express M965 Carrier board.

The full development kit is coded as COM EXP T6 DEV KIT and does contain:

- Carrier board for COM Express® Type 6 compliant modules CCOMe-C96
- GPIO Header adapter cable (Free wires on one extremity)
- 2 x DB-9 Serial cable adapter
- Front Panel Board with connecting cable (CV-837/30 and CV-836/30)
- SATA 7p Data cable
- DP cable
- HDMI cable
- DP-to-HDMI adapter
- eDP cable

A more detailed description can be found at related product page in Seco S.p.A website: COM EXP T6 DEV KIT (seco.com)